

CMOS Pixel Technologies R&D state of the art

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On behalf of the PICSEL team of IPHC



CENTRE NATIONAL
DE LA RECHERCHE
SCIENTIFIQUE



Outline

- Motivations for developing CMOS Pixel Sensors (CPS) beyond STAR-PXL
- Main characteristics of the real scale sensor FSBB-M fabricated in 2014
- Beam test based performance assessment of the FSBB-M sensor
- Summary and outlook

State-of-the-Art: STAR-PXL (The Sensor)

ULTIMATE main characteristics

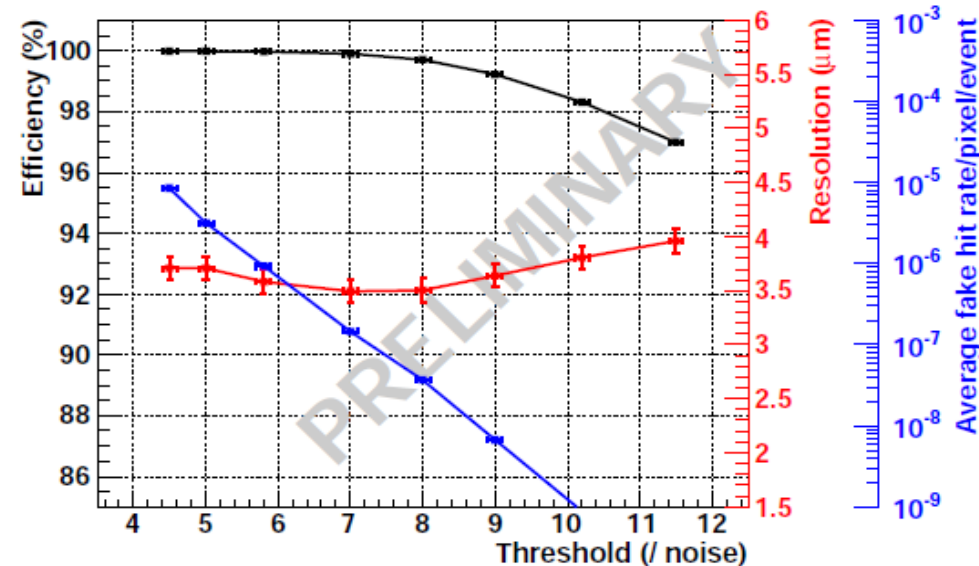
- CMOS sensor (0.35 μm AMS) high-resistive Epi-layer-15 μm
Sensor thinned to 50 μm (total thickness)
- Column || architecture with in-pixel CDS & amplification
- End-of-column discriminator & binary charge encoding, followed by \emptyset -suppression
- 960x928 (columns x rows): pitch 20.7 μm (19.9x19.2 mm²)
- $t_{\text{r.o.}} \lesssim 200\mu\text{s}$ ($\sim 5 \times 10^3$ frames/s) \Rightarrow suited to $> 10^6$ part./cm²/s
- 2 outputs @ 160 MHz
- Power consumption $\sim 150\text{mW}/\text{cm}^2$
- Running at room temp. ($T = 30\text{C}^\circ$)



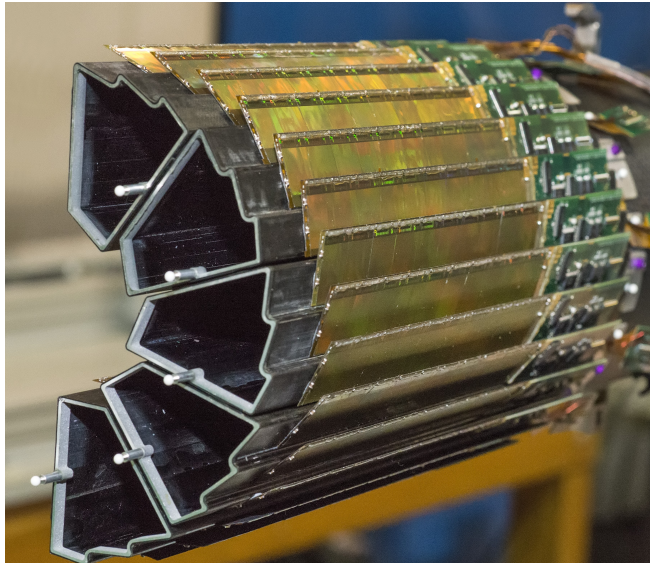
ULTIMATE Performances

- $\sigma_{\text{sp}} \gtrsim 3.5\mu\text{m}$
- Efficiency $\lesssim 99.9\%$
- Fake rate $\lesssim 10^{-5}$

MIMOSA 28 - epi 15 μm



State-of-the-Art: STAR-PXL (I)



STAR-PXL HALF-BARREL

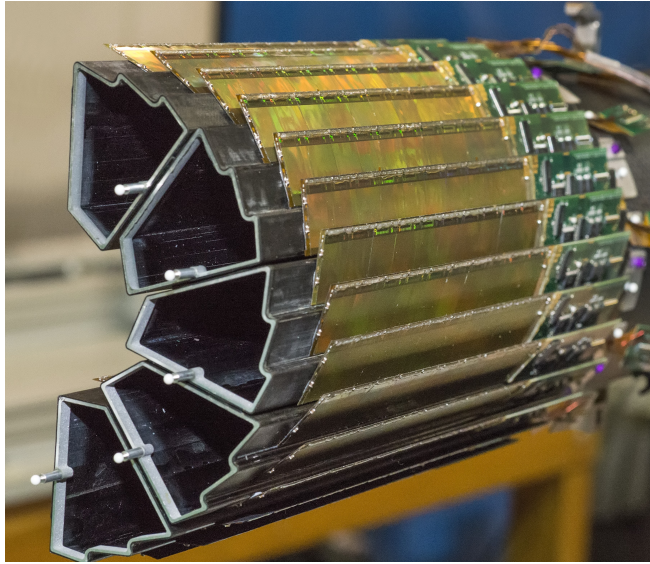
- 2 layers: 20 ladders ($0.37\% X_0$)
- 200 sensors
- 180×10^6 pixels
- Air flow cooling: $T < 35^\circ\text{C}$
- $\sigma_{\text{sp}} < 4\mu\text{m}$
- Rad. Load $150\text{kRad} + 3 \times 10^{12}$ n.e.q (Full life-time)
- $t_{\text{o.r.}} < 200\mu\text{s}$

1st CMOS Pixel Sensor in a collider experiment !

Data Taking from March-June 2014



State-of-the-Art: STAR-PXL (II)

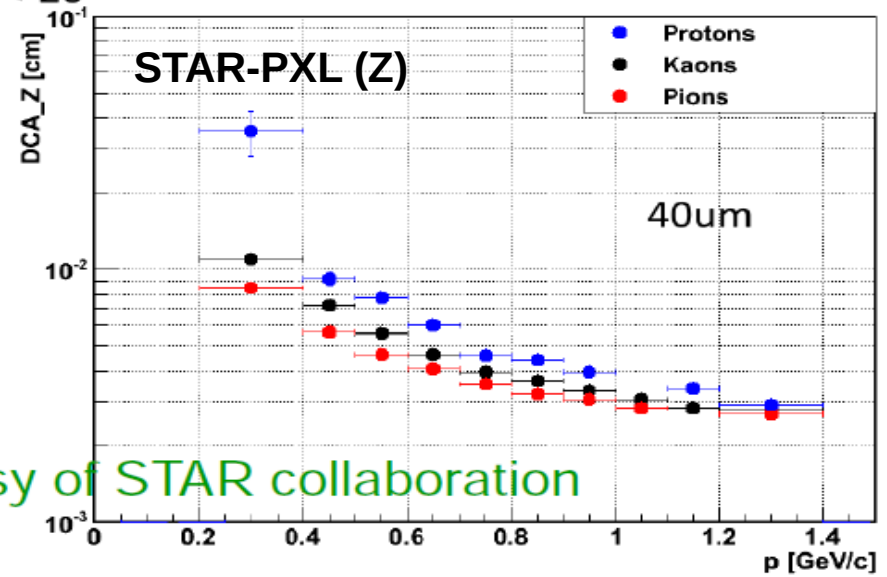
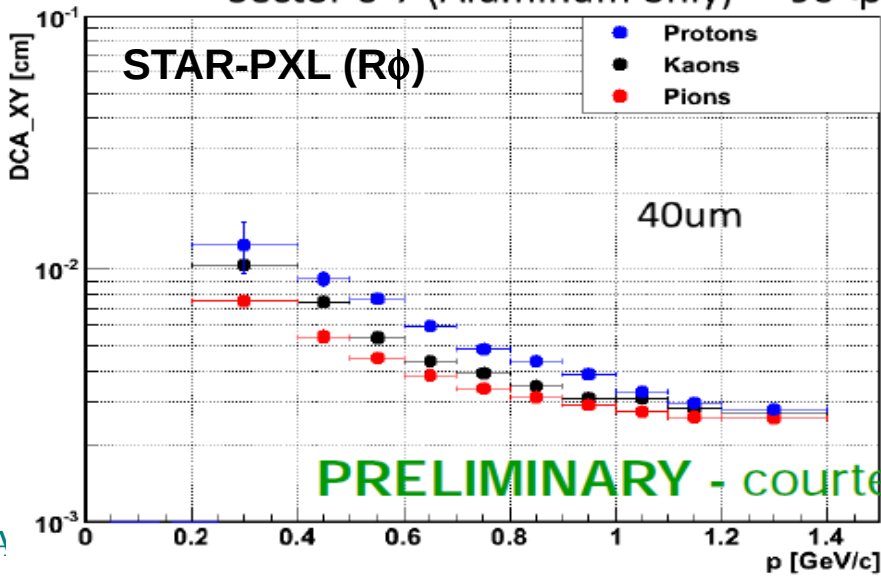


STAR-PXL HALF-BARREL

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1st CMOS Pixel Sensor in a collider experiment !

Sector 6-7 (Aluminum only) $-90 < \phi < -20$

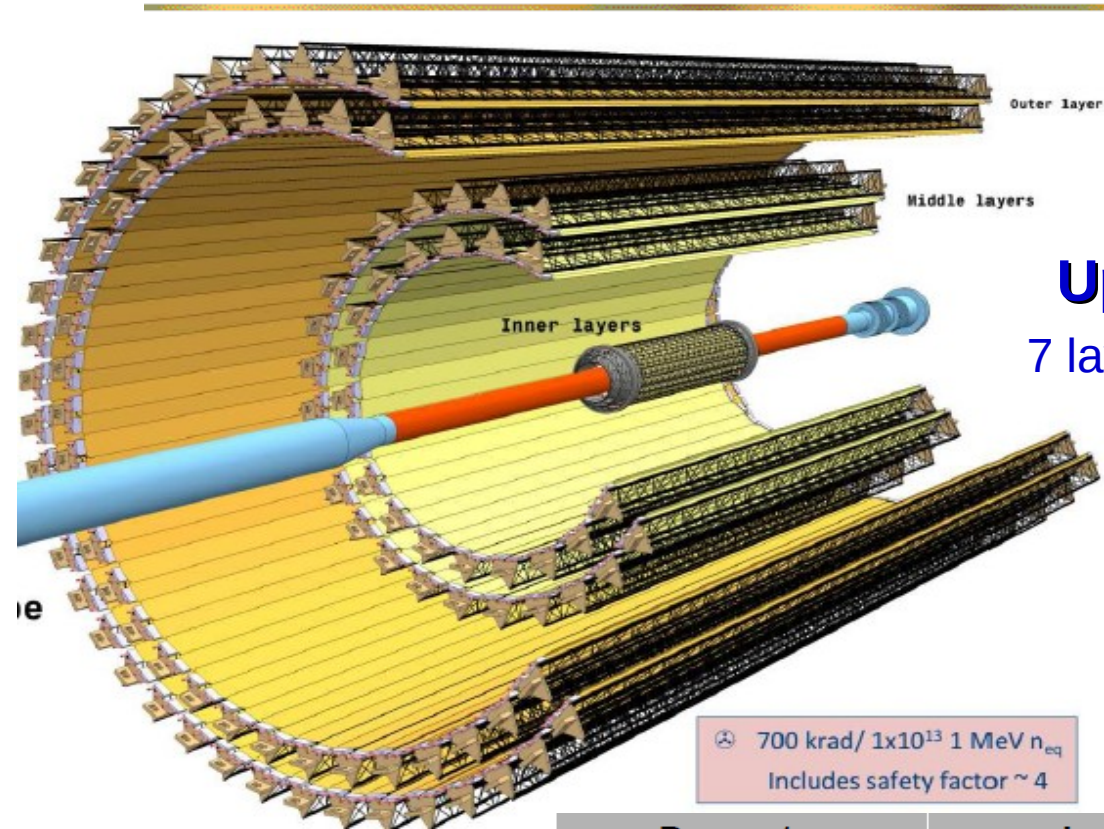


Next generation of High Precision
Tracking & Vertexing Devices



FASTER and **MORE RADIATION TOLERANT**
CMOS Pixel Sensors (CPS)

Forthcoming device: New ALICE Inner Tracking System (ITS)



ALICE

Upgrade of ALICE-ITS at LHC

7 layers > 10m² active area (>> 10⁴ CPS)

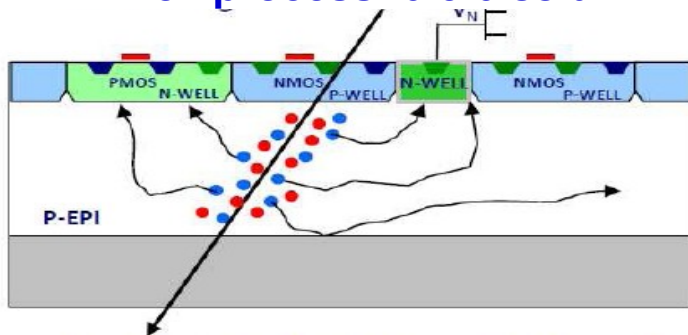
- $\sigma_{sp} \lesssim 5(10)\mu\text{m}$ inner (outer) layers
- $\sim 0.3\%$ X_0 / layer

⚠ 700 krad / 1×10^{13} 1 MeV n_{eq}
Includes safety factor ~ 4

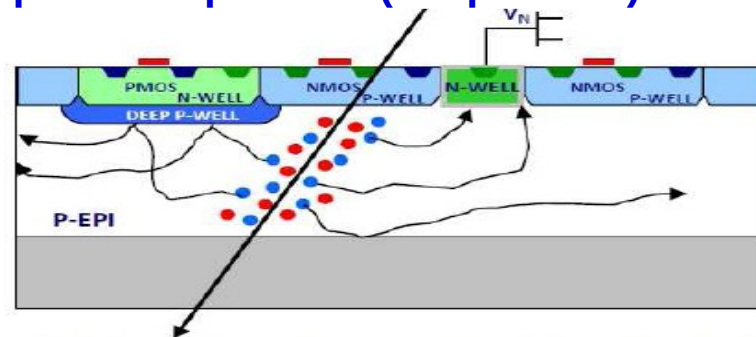
Parameter	Inner Barrel	Outer Barrel
Max thickness (μm)	50	50
σ_{sp} (μm)	5	10
Chip dims. (mm^2)	15x30	15x30
Max power (mW/cm^2)	300	100
Max t_{int} (μs)	30	30
Radiation load	250kRad + $2.5 \times 10^{12} n_{eq}/\text{cm}^2$	15kRad + $5 \times 10^{11} n_{eq}/\text{cm}^2$

CMOS Process Transition: STAR-PXL → ALICE-ITS

Twin well process: 0.6-0.35 μm

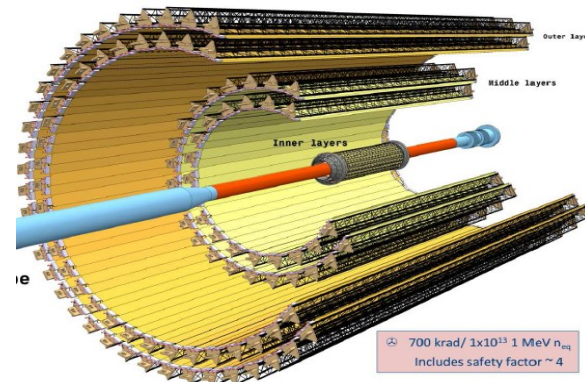
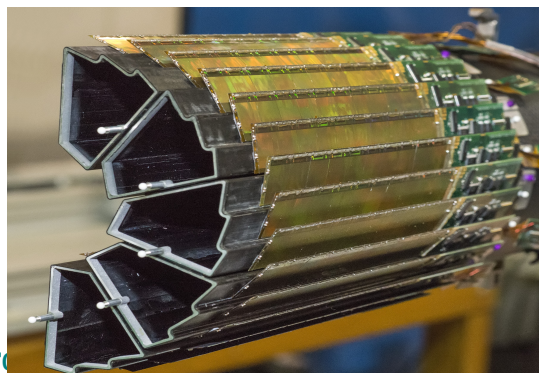
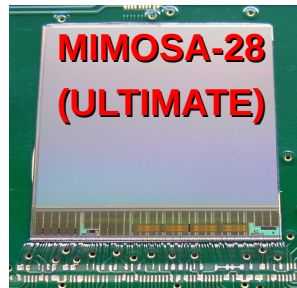


Quadrupole well process (deep P-well): 0.18 μm



- Use of PMOS in pixel array not allowed because any additional N-well hosting PMOS would compete for charge collection with sensing node
- Limits choice of readout architecture strategy
- Already demonstrate excellent performances
 - STAR-PXL: Mi-28 designed in AMS-0.35 μm process $\Rightarrow \epsilon_{\text{det}} > 99.5\%$, $\sigma_{\text{sp}} < 4\mu\text{m}$
 - 1st CPS detector at collider experiment

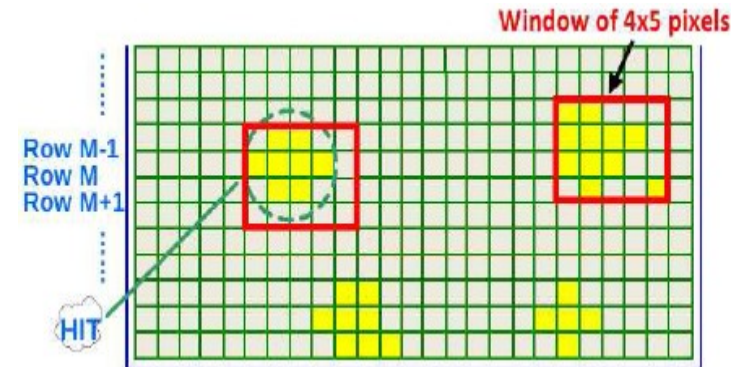
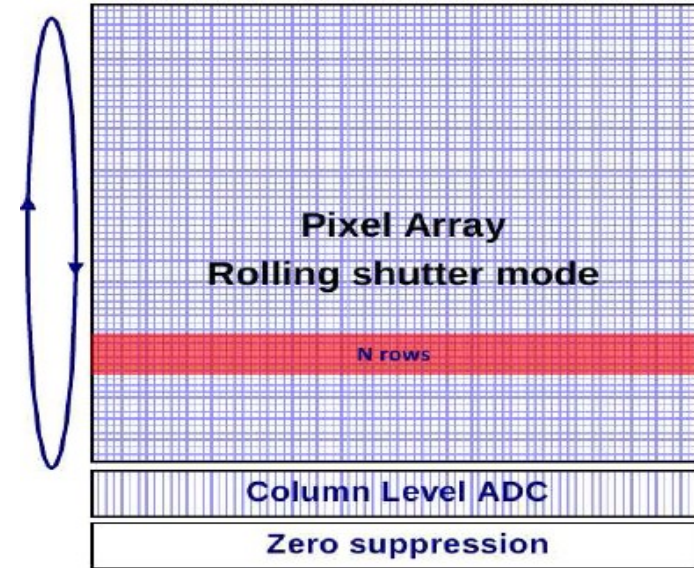
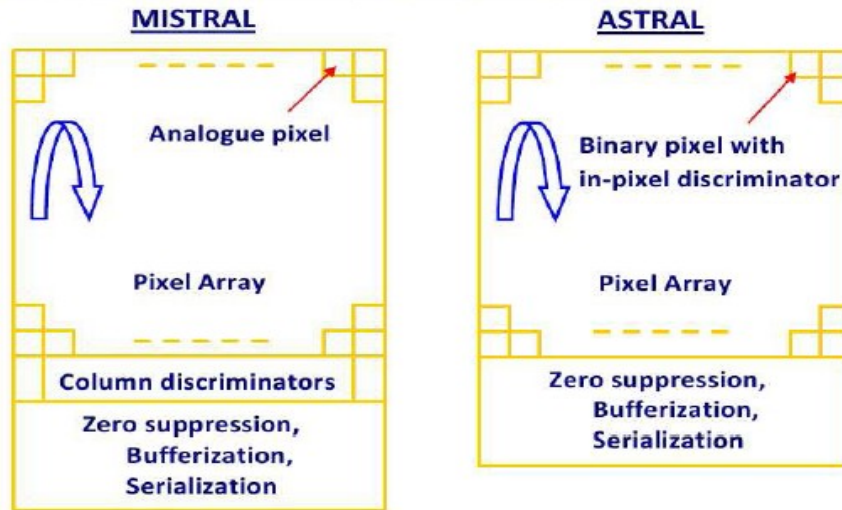
- N-well hosting PMOS transistors is shielded by deep P-well \Rightarrow both types of transistors can be used
- Widens choice of readout architecture strategies
 - Ex. ALICE-ITS upgrade: 2 sensors R&D in || using TOWER CIS 0.18 μm process (quadrupole well)
 - Synchronous Readout R&D: proven architecture \Rightarrow safety
 - Asynchronous Readout R&D: challenging



700 krad / 1×10^{13} 1 MeV n_{eq}
Includes safety factor ~ 4

Synchronous readout Architecture: Rolling Shutter Mode

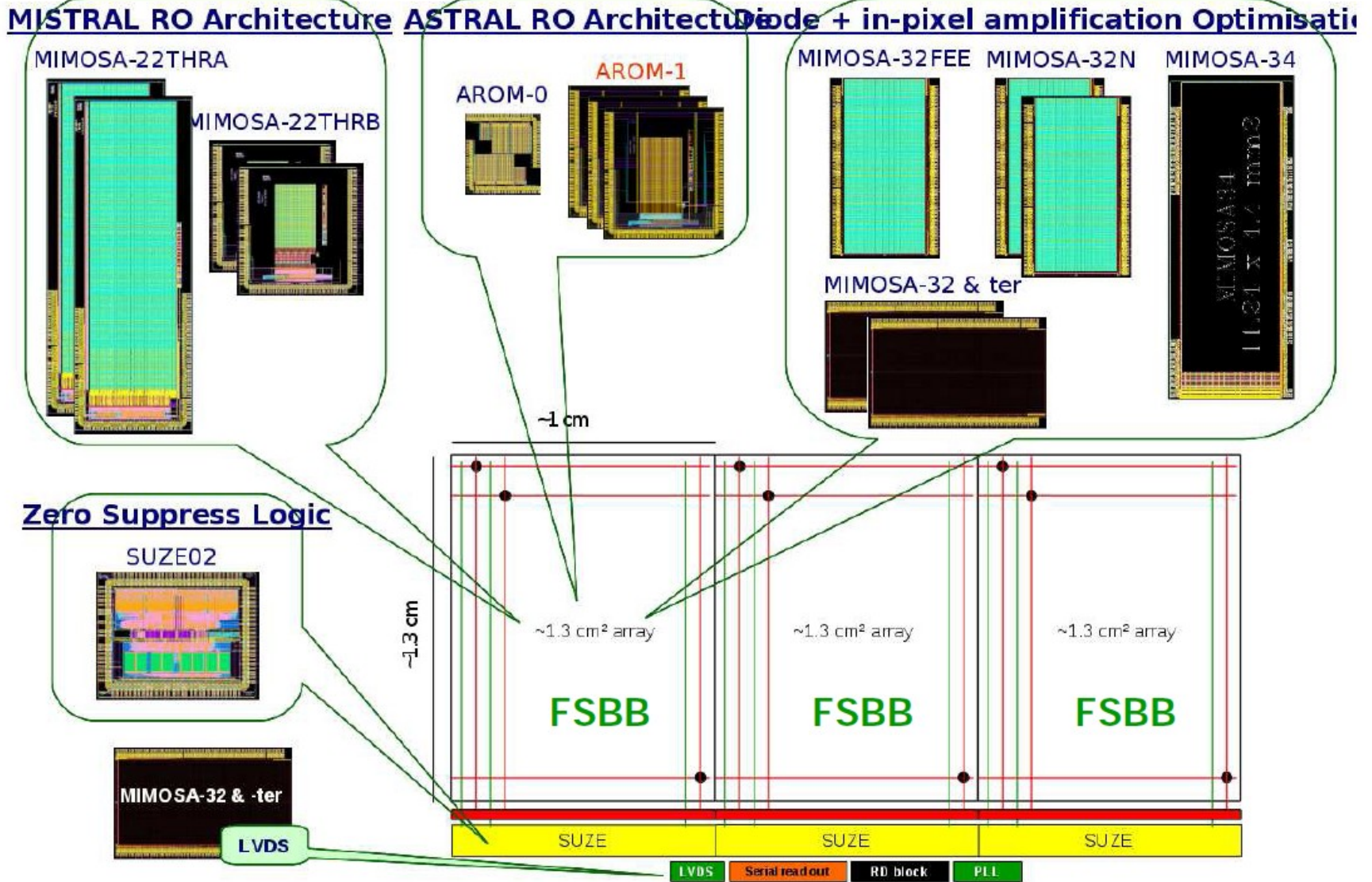
- Design addresses 3 issues
 - Increasing S/N at pixel-level
 - Analogue to Digital Conversion
 - At end of column \Rightarrow **MISTRAL**
 - Inside pixel \Rightarrow **ASTRAL**
 - Zero suppression (SUZE) at chip edge



- Power vs Speed
 - Power: only the selected rows ($N=1,2,3 \dots$) to be readout
 - Speed: N rows of pixels are readout in ||

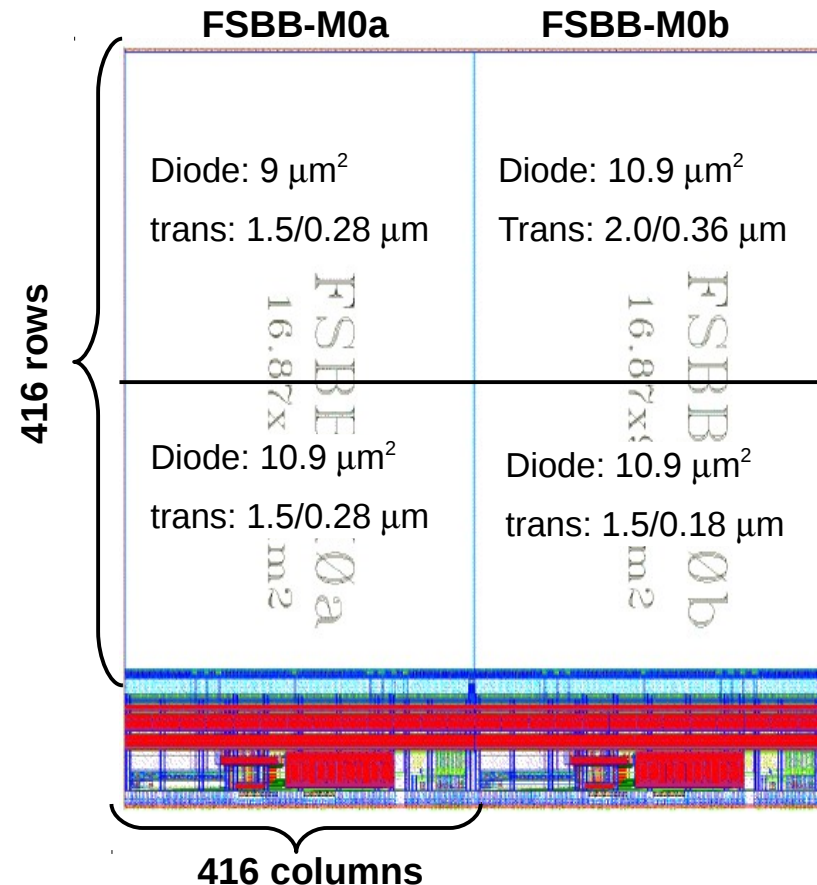
Integration-time (t_{int}) = frame readout time $\Rightarrow t_{int} = \frac{(\text{Row readout time}) \times (\text{No. of Rows})}{N}$

Prototypes Fabricated to Explore the Full Sensor Chain



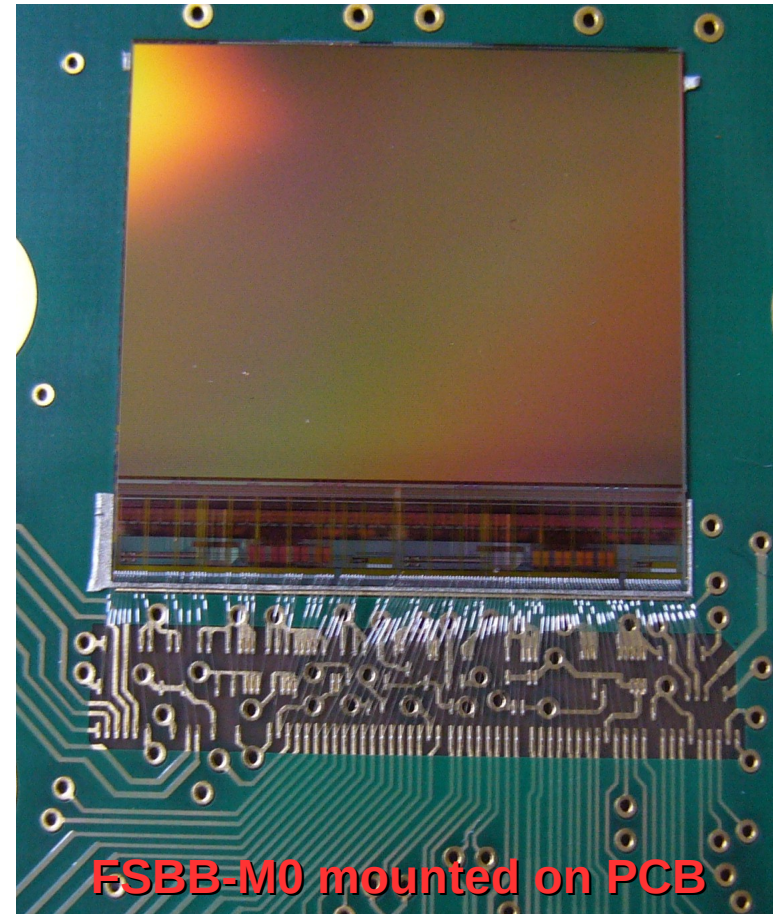
FSBB-M0 (\equiv MISTRAL) Fabricated in Spring 2014

- TJsc-0.18 CIS process, HR ($\sim 1\text{k}\Omega\text{cm}$) $18\mu\text{m}$ epitaxy, thinned to $50\mu\text{m}$
- Staggered pixel: $22 \times 33 \mu\text{m}^2$ including pre-amplification and clamping with 6 metal layers (ML)
- 416×416 of Columns x Row of pixels ended by discriminator (8-cols with analogue output)
- Double-row readout at 160MHz clock frequency $\Rightarrow t_{\text{int}} = 40\mu\text{s}$
- On-chip 3-stage sparsification: SUZE-02
- 4 Memories of 512×32 bits
- 2 output nodes at 320Mbits/s (used only one for TB)
- Integrated JTAG and regulators
- Sensitive area $\sim 1.2\text{cm}^2$
- Two versions fabricated (FSBB-M0 a & b)
 - FSBB-M0a: sensing node size variation
 - FSBB-M0b: input transistor of in-pixel pre-amplifier
- **Design not optimized in terms of**
 - Pixel dimensions
 - Power consumption
 - Readout speed
 - ITS layer, layout
 - In-pixels circuitry and discriminator
 - Epitaxy parameters



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Beam-Test: Experimental conditions and set-up

Beam conditions at CERN on Oct. 2014

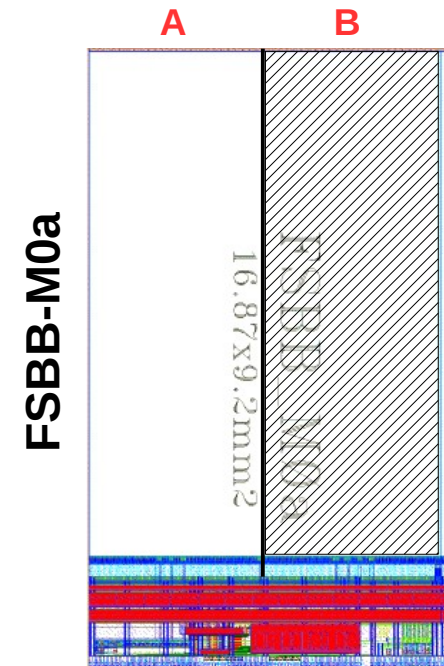
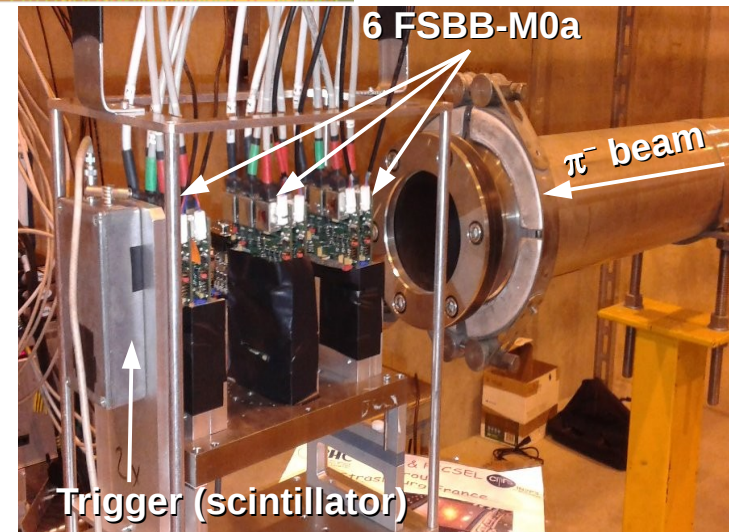
- SPS H6A area
- 120 GeV π^-
- Particle flux: trigger rate ~ 2.5 to 100 kHz / 5×10 mm²

Device used for the tests

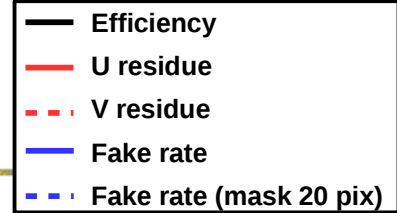
- 6 FSBB-M0a thinned to 50 μ m
- Most of the measurements with sub-array B (80k pixels), less cross-couplings than sub-array A

Data Collected (mainly on October 18-19th)

- 3.7×10^6 triggers collected with beam
- Reconstructed tracks for performances assessment
 - 11 μ m² diode: ~ 400 k
 - 9 μ m² diode: ~ 300 k
- 8.5×10^6 frames collected without beam for noise determination \Rightarrow fake rate studies
- All measurements performed at $T_{op} = 30^\circ\text{C}$

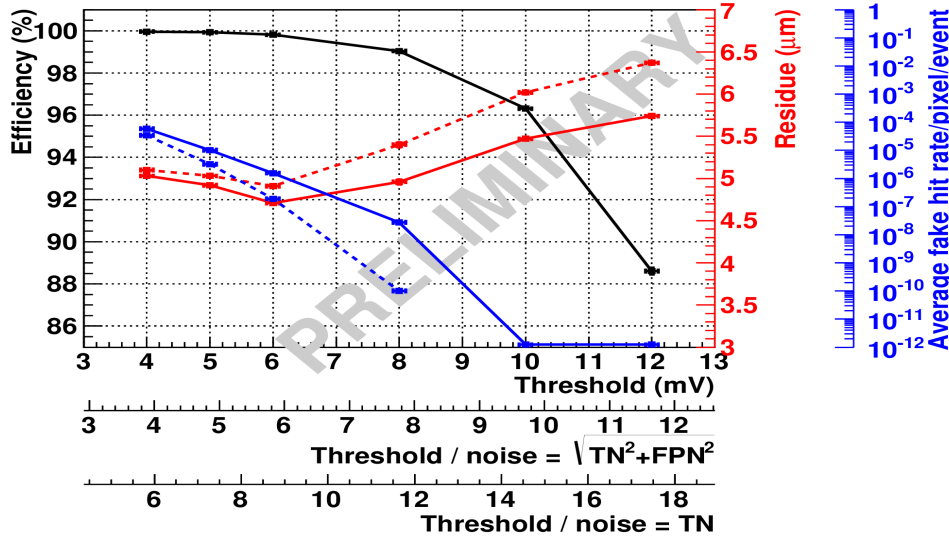


Beam-Test: Detection Performances

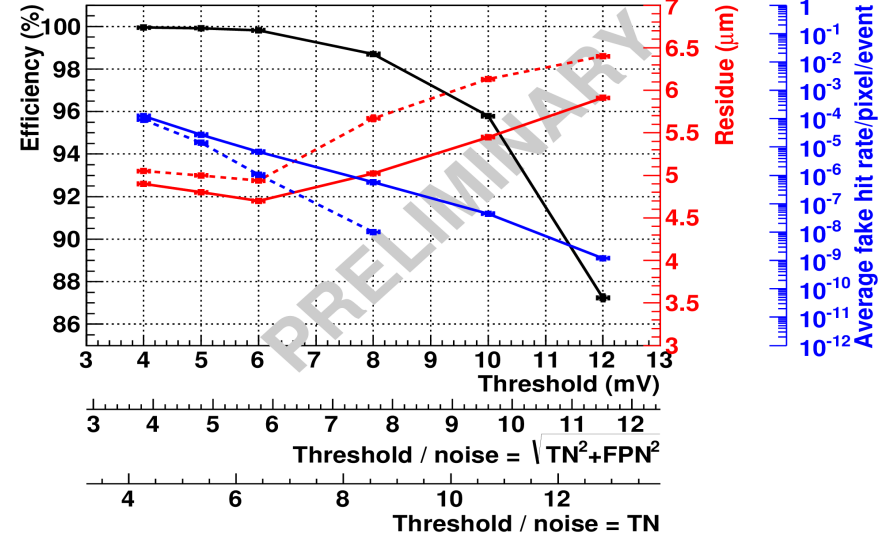


ϵ_{det} , fake rate, σ_{res} vs discriminator threshold (Noise averaged over 11 thinned sensors)

FSBB_M0a, Diode = 9 μm^2 , Transistor = 1.5/0.28



FSBB_M0a, Diode = 10.9 μm^2 , Transistor = 1.5/0.28



Diode size (μm^2)	$\epsilon_{det} \gtrsim 99.8\%$	$\epsilon_{det} \gtrsim 99.5\%$	$\epsilon_{det} \gtrsim 99.0\%$	fake $\lesssim 10^{-5}$
11.0	$\lesssim 6.0$ mV	$\lesssim 6.5$ mV	$\lesssim 8.0$ mV	$\gtrsim 6.0$ mV
9.0	$\lesssim 6.0$ mV	$\lesssim 7.0$ mV	$\lesssim 8.0$ mV	$\gtrsim 5.0$ mV

} Discriminator Thresholds

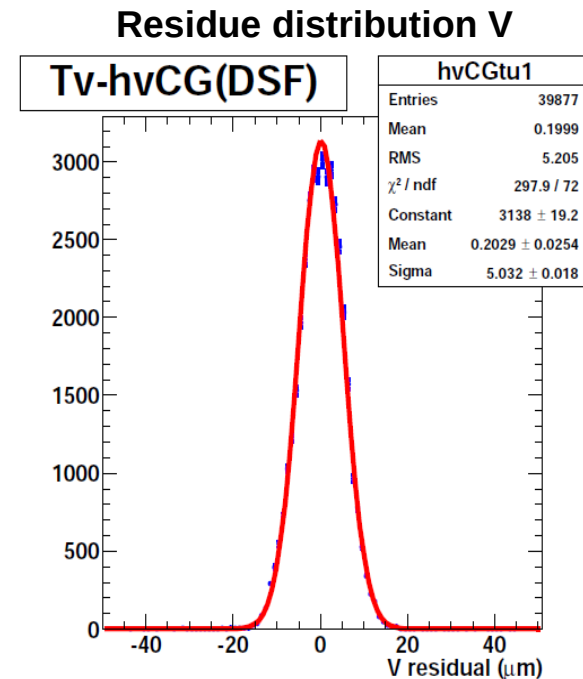
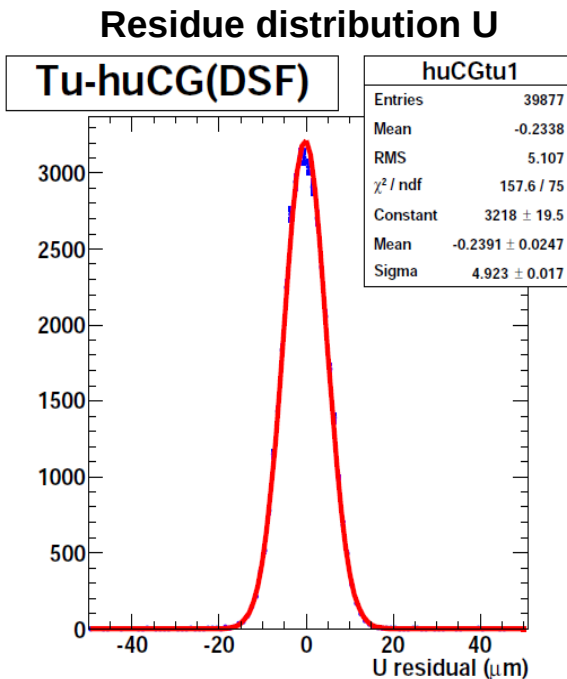
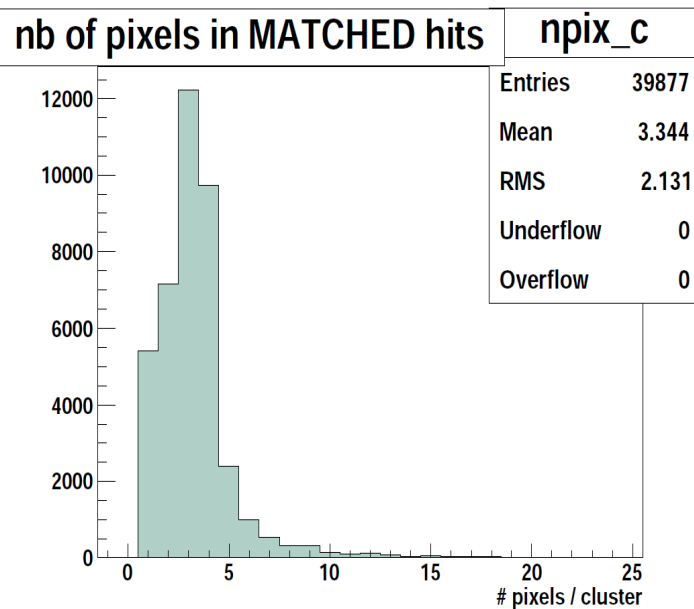
Residue on DUT: $\sigma_{res} \approx (4.7 \pm 0.1) \mu\text{m}$ (U) & $(4.9 \pm 0.1) \mu\text{m}$ (V) at 6mV for both diode sizes

Expected resolution: $\sigma_{sp} \approx 4.5 \mu\text{m}$ (tbc)

Beam-Test: Spatial resolution vs cluster multiplicity

- Multiplicity depends on where the track hits the sensor with respect to the collection diode
⇒ resolution is then a function of multiplicity

- 9 μm^2 diode:** threshold at 5mV



Beam-Test: Spatial resolution vs cluster multiplicity

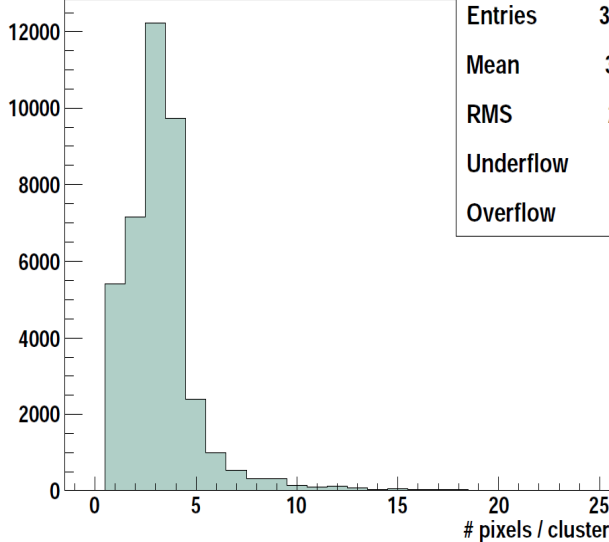
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Track position distribution vs associated hit multiplicity

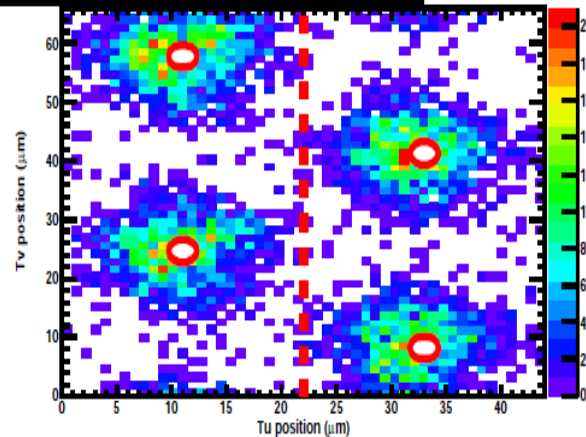
- 9 μm^2 diode:** threshold at 5mV

nb of pixels in MATCHED hits

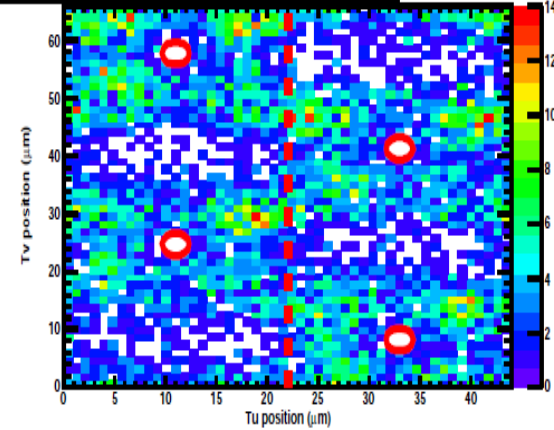
npix_c



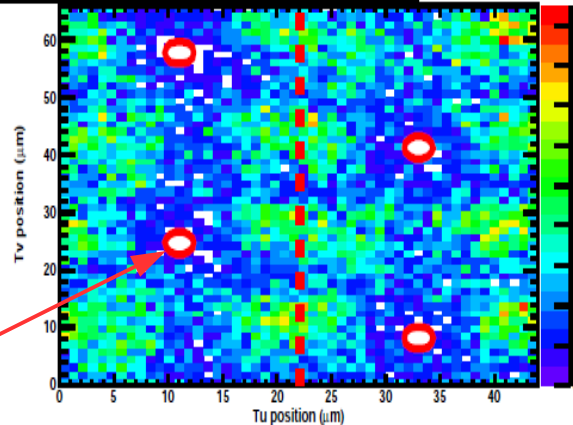
Tu vs Tv on matrix for Mult. = 1



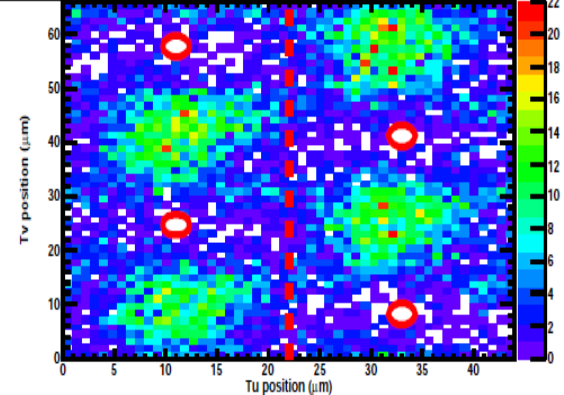
Tu vs Tv on matrix for Mult. = 2



Tu vs Tv on matrix for Mult. = 3



Tu vs Tv on matrix for Mult. = 4

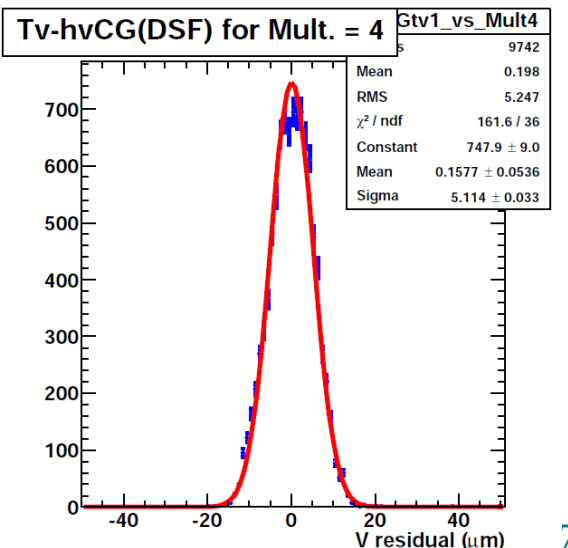
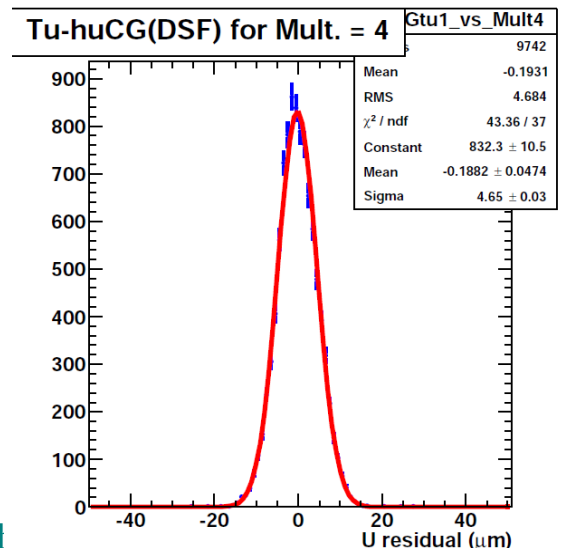
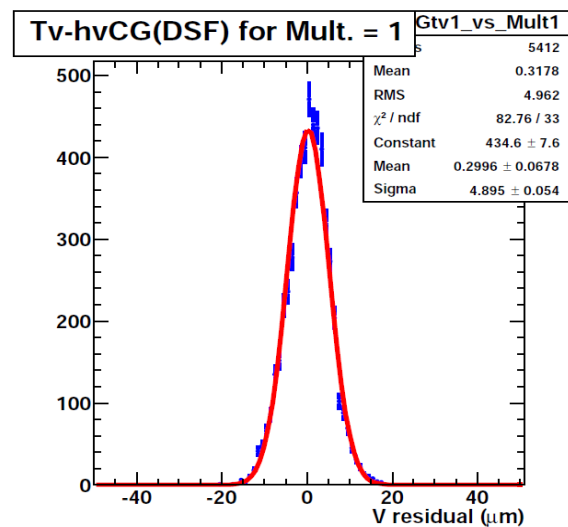
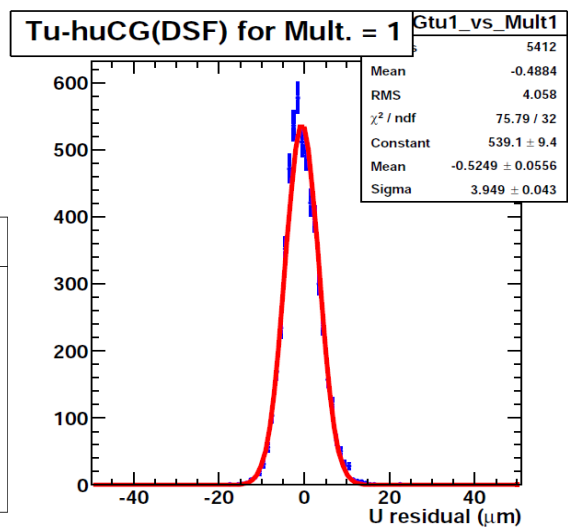
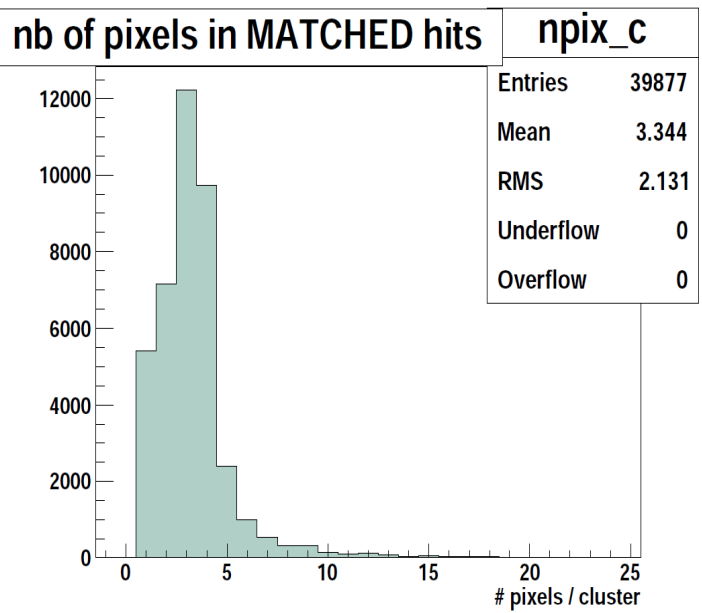


Collection diode position

Beam-Test: Spatial resolution vs cluster multiplicity

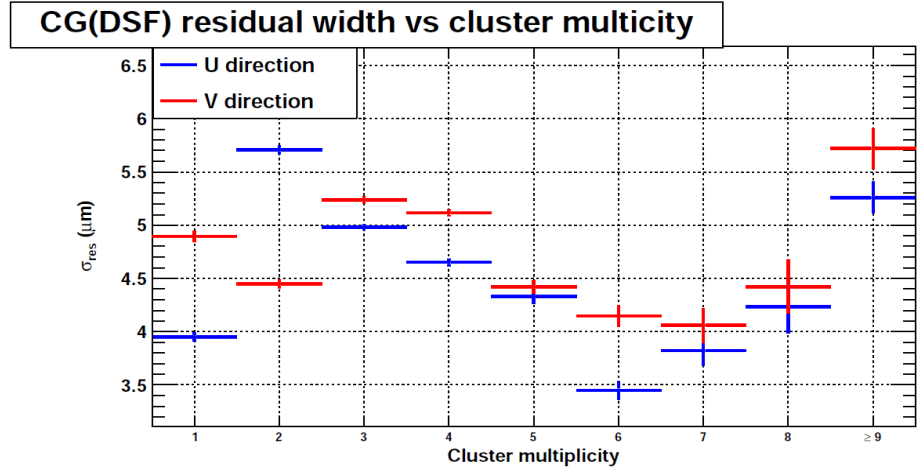
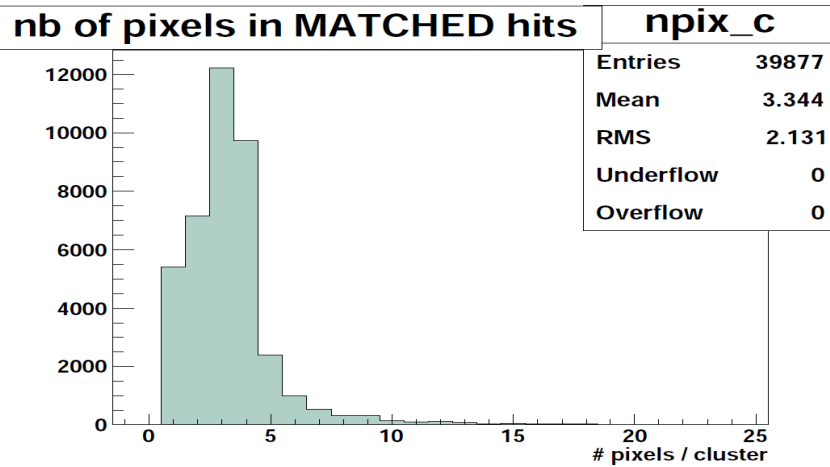
- Multiplicity depends on where the track hits the sensor with respect to the collection diode
 \Rightarrow resolution is then a function of multiplicity

9 μm^2 diode: threshold at 5mV

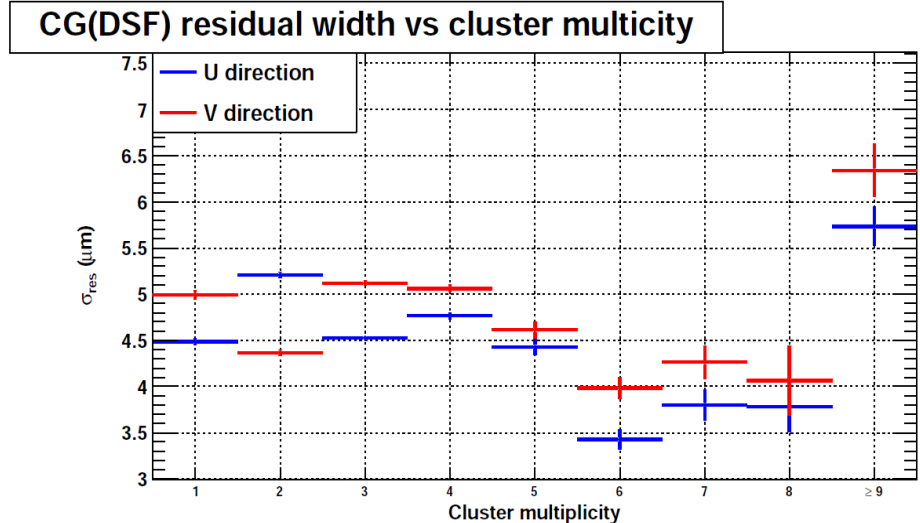
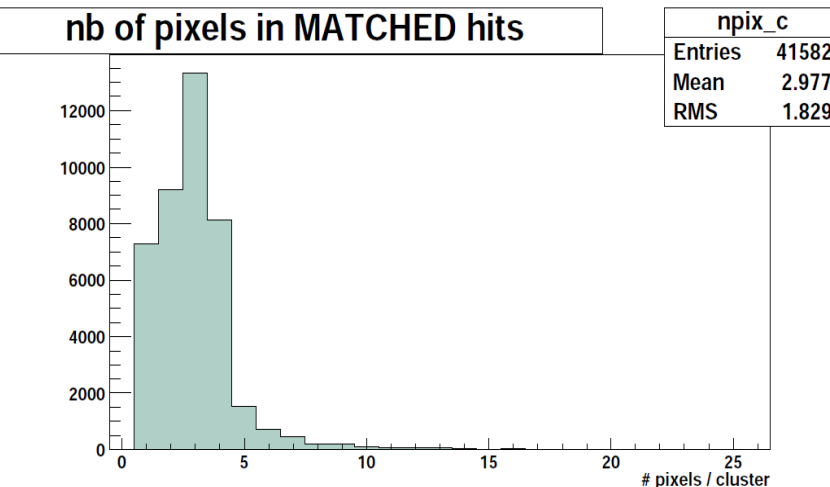


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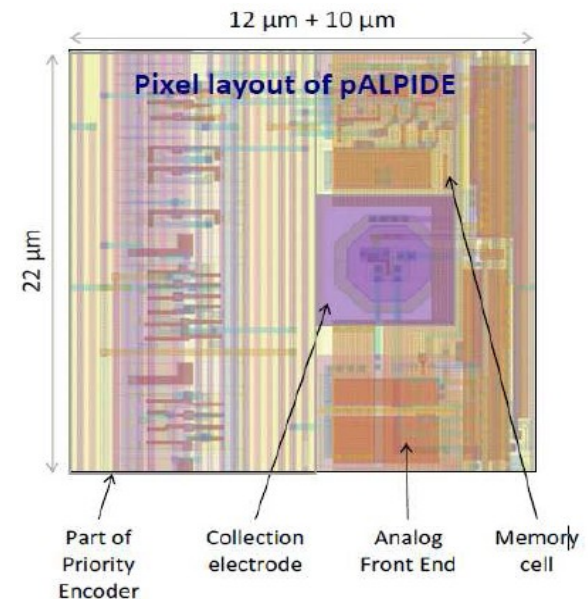
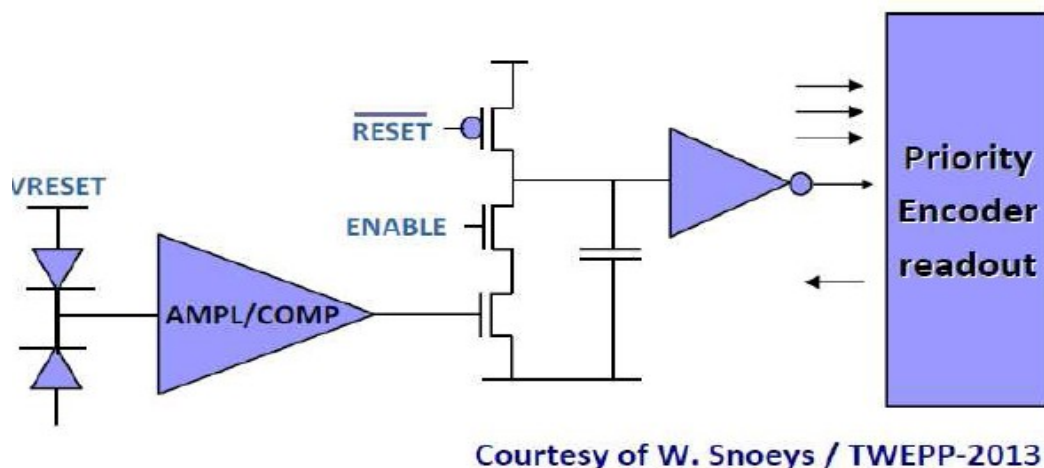
- 11 μm^2 diode:** threshold at 5mV



Asynchronous readout Architecture

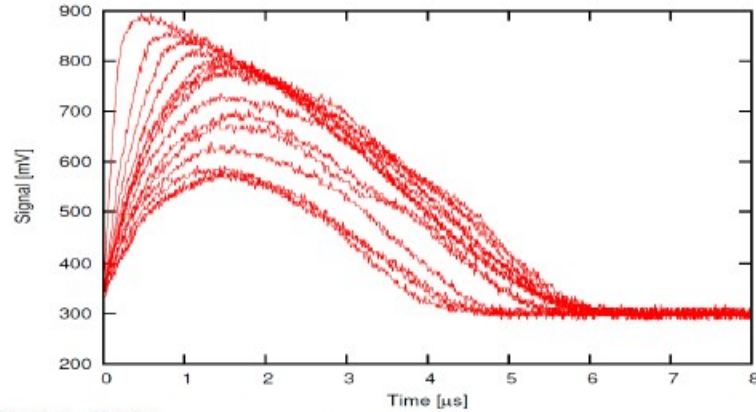
ALPIDE (Alice Pixel DEtector)

- Concept similar to hybrid pixel readout architecture
 - Tower CIS quadrupole well process: both N & P MOS can be used
- Continuously power active in each pixel
 - Low power consumption analogue front-end ($< 50\text{nW}/\text{pixel}$) based on single stage amplifier with shaping / current comparator
 - High gain ~ 100
 - Shaping time few μs
 - Dynamic memory cell, $\sim 80\text{fF}$ storage capacitor which is discharged by an NMOS controlled by the front-end
- Data driven readout of the pixel matrix, only zero-suppressed data transferred to periphery

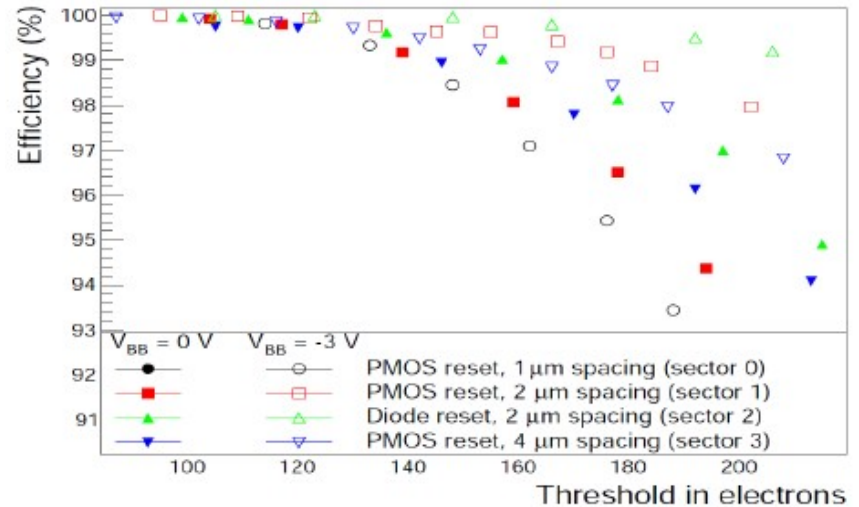
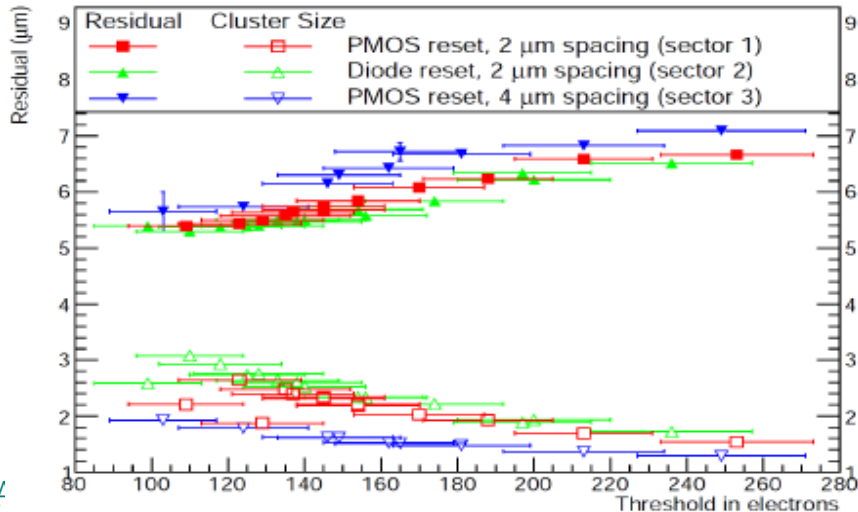
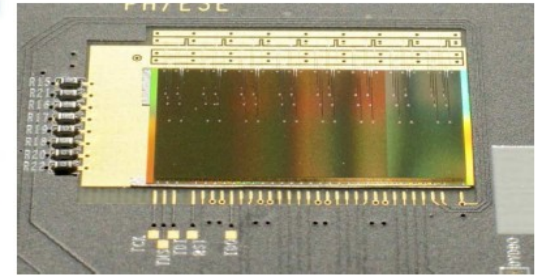
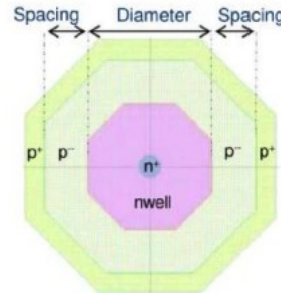


ALPIDE Architecture Validation

- 1st step: pALPIDE to validate fast pixel readout
 - 64x512 columns x rows ($22 \times 22 \mu\text{m}^2$)
 - Analog output of one pixel tested with ^{55}Fe source \Rightarrow expected time resolution



- 2nd step: full scale ALPIDE
 - Final sensor dimensions: $15 \times 30 \text{ mm}^2$
 - $\sim 500\text{k}$ pixels of $28 \times 28 \mu\text{m}^2$
 - 4 different sensing node geometries
 - Possibility of reverse biasing the substrate



Summary and outlook

1st FSBB (1.2cm² sensitive area) composing MISTRAL sensor (4.2cm² sensitive area) fabricated & successfully (but not completely) assessed on beam at T = 30°C

- $\epsilon_{\text{det}} \sim 99.8\%$ for fake rate $< 10^{-6}$
- $\sigma_{\text{sp}} < 5\mu\text{m}$ with 22x33 μm^2 pixels

Some layout shortcomings observed (e.g. x-couplings in peripheral circuitry)

- Corrections implemented in FSBB-M0bis, submitted to foundry

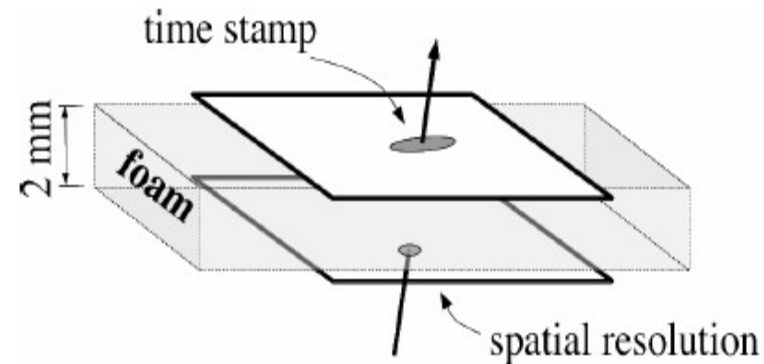
Next steps

- 2015: fabrication of full scale MISTRAL prototype ALICE-ITS outer layers

Potential of FSBB-M/MISTRAL architecture well suited for ILD-VXD. E.g.

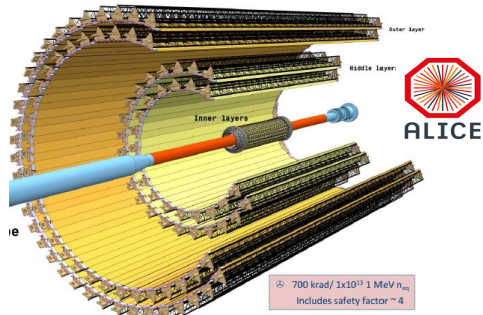
- 17x17 μm^2 pixels: $\sigma_{\text{sp}} < 3\mu\text{m}$ & $t_{\text{int}} \sim 30\text{-}40\mu\text{s}$ (tbc)
- 17x102 μm^2 pixels: $\sigma_{\text{sp}} < 6\mu\text{m}$ & $t_{\text{int}} \sim 5\mu\text{s}$ (tbc)

- **See A. Besson's talks for more on perspectives for ILD-VXD**



Back up Slides

Next Forthcoming device: CBM Micro-Vertex Detector (MVD)

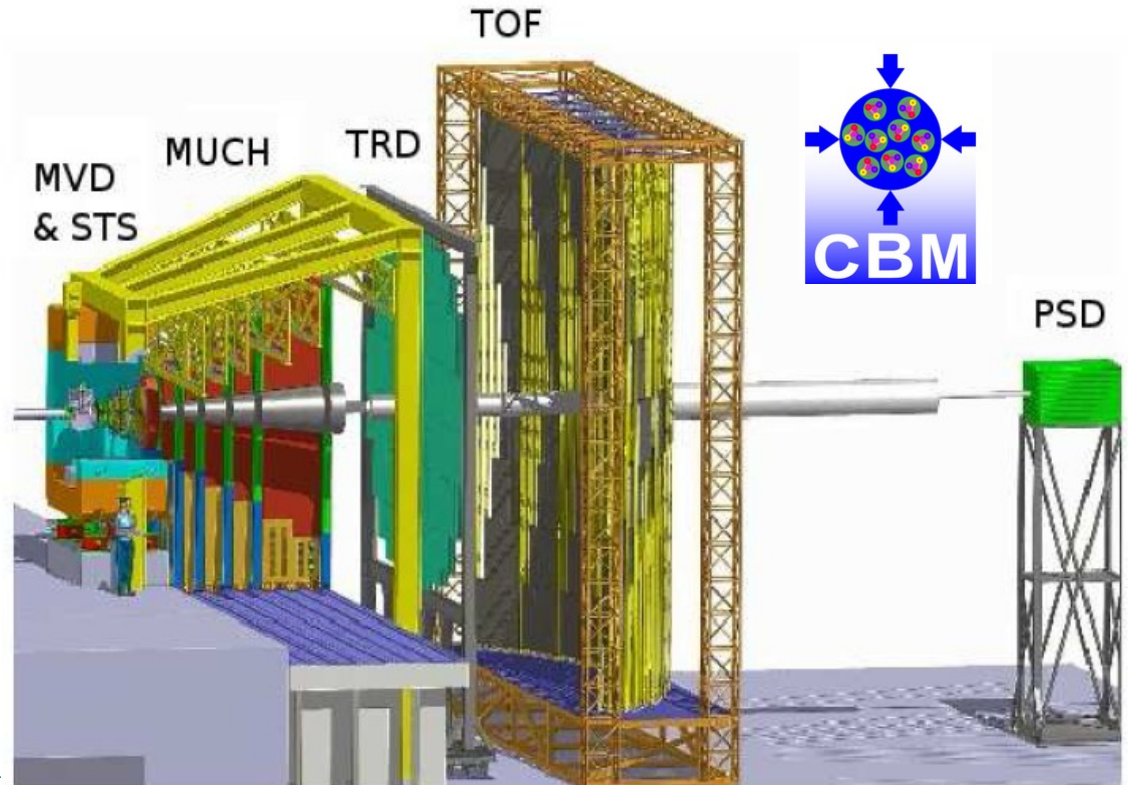
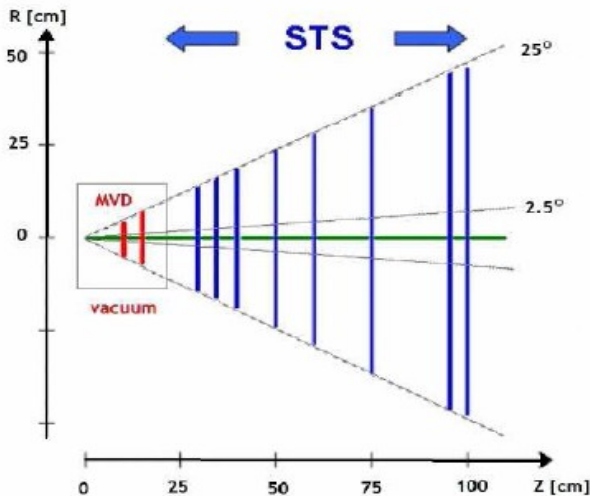


ALICE-ITS 2018/19

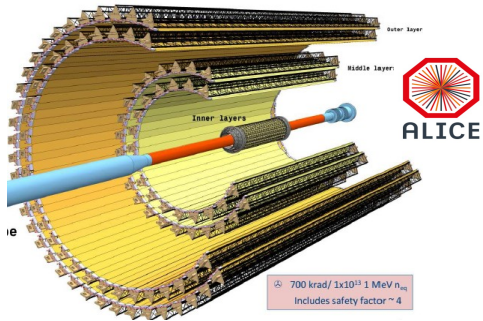
CBM-MVD at FAIR/GSI

3 double-sided stations in vacuum at $T < 0^\circ\text{C}$

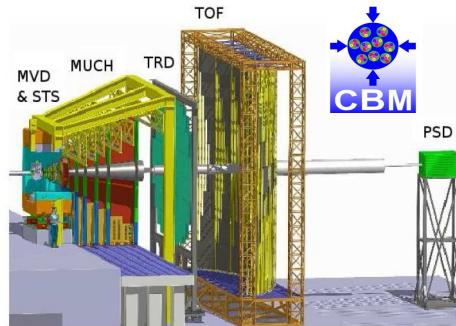
- $\sigma_{sp} \lesssim 5 \mu\text{m}$
- $\sim 0.5 \% X_0 / \text{station}$
- Radiation load: $\gtrsim 10^{13} n_{eq} / \text{cm}^2$



Device under Study: ILC Vertex Detector



ALICE-ITS 2018/19

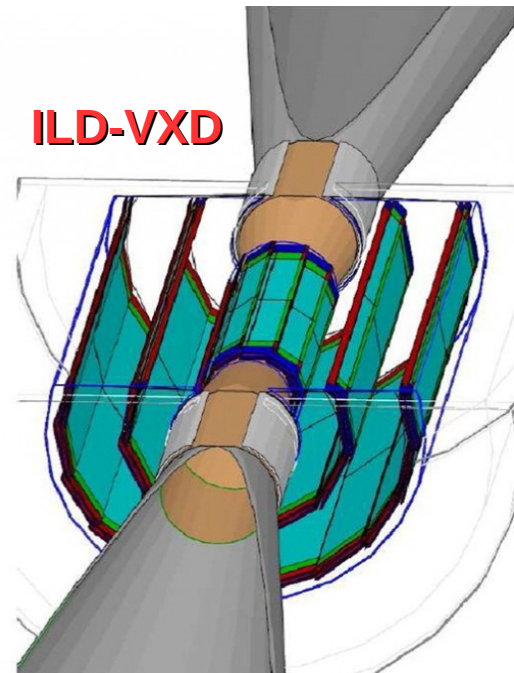
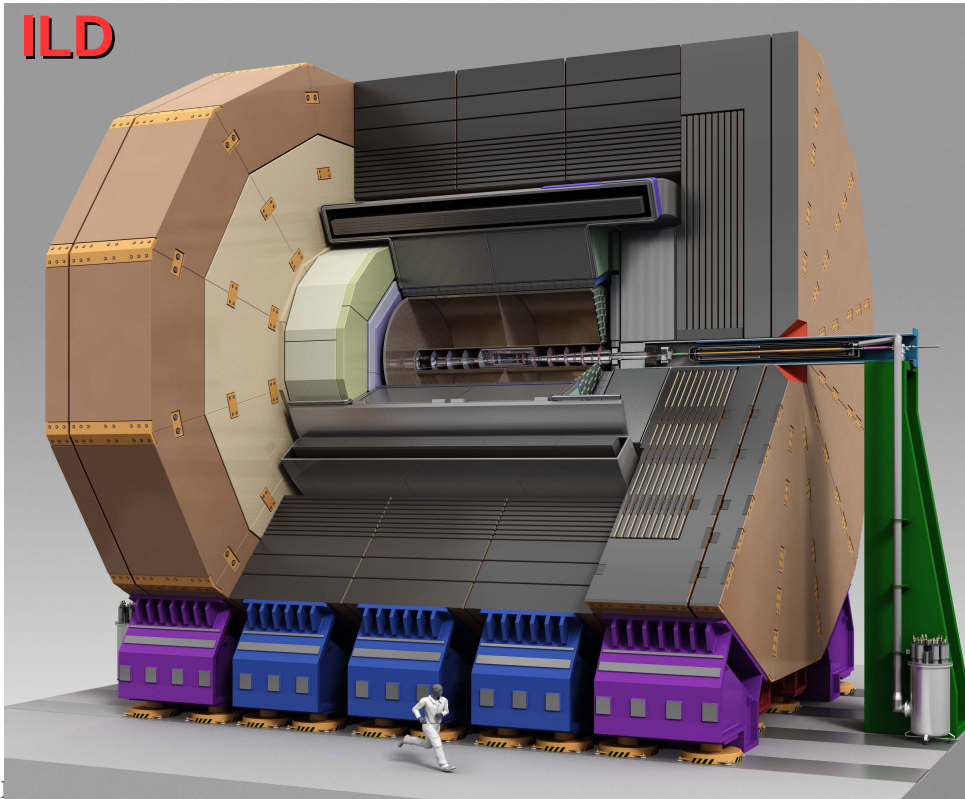


CBM-MVD > 2020

ILD-VXD at ILC

3 double-sided layers

- $\sigma_{sp} \lesssim 3 \mu\text{m}$
- $\sim 0.3 \% X_0 / \text{layer}$
- Radiation load: $O(100) \text{ kRad} + O(10^{11}) n_{eq}/\text{cm}^2 (1\text{yr})$



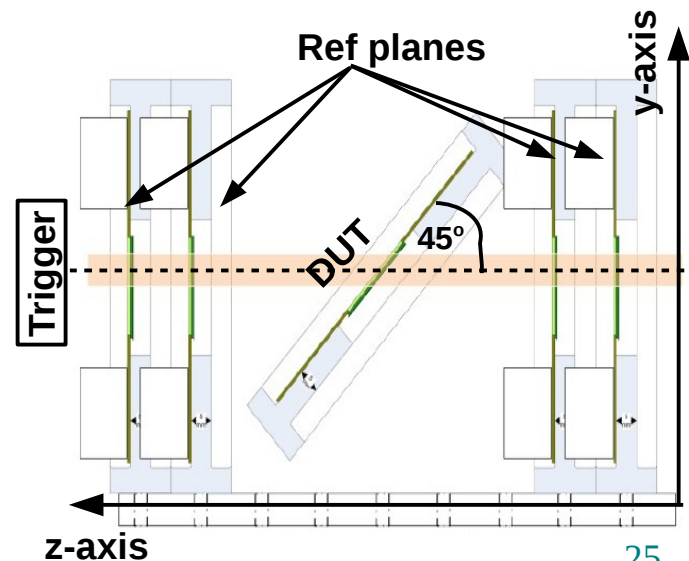
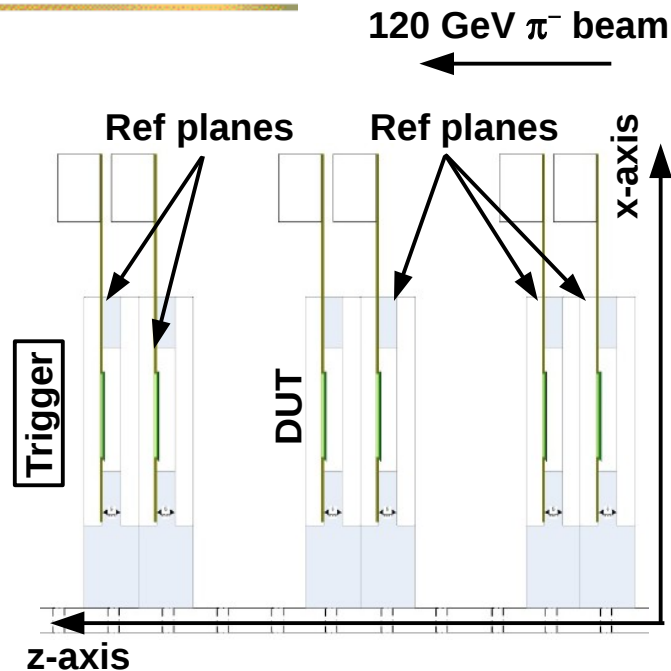
Beam-Test: Main goals and data collected

Main goals (mainly with sub-array B)

- Validate pixel geometry for $\sigma_{sp} \sim 5\mu\text{m}$
- Determine detection efficiency (ϵ_{det})
- Determine working range with
 - $\epsilon_{det} > 99\%$
 - Fake hit rate $< 10^{-5}$
- Study impact of present cross-coupling effects

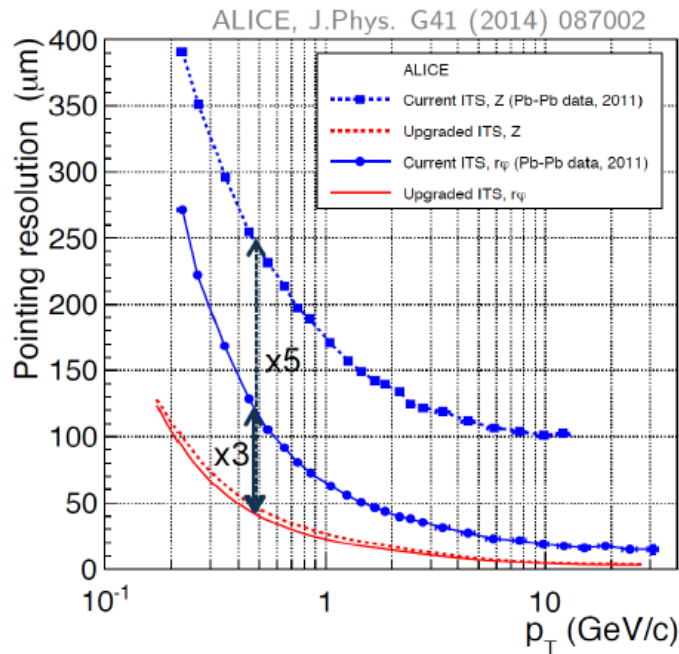
Running parameters varied

- Discriminator thresholds: 4 \rightarrow 12 mV
- Beam flux: 0.78 \rightarrow 11.6 hits/cm²/frame (average value)
- Incidence angle of beam particle on DUT: 0 or $\sim 45^\circ$ (ITS maximum pseudo-rapidity $\sim 55^\circ$)
- Comparison of sub-array A to sub-array B
- V_{REF} (discr.): external (cable on chip) vs internal (SDS)

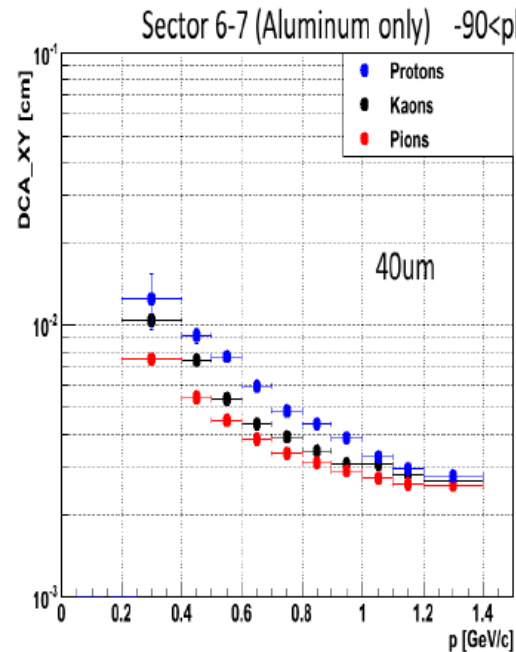


FSBB-M0 inspired from STAR-PXL Chip

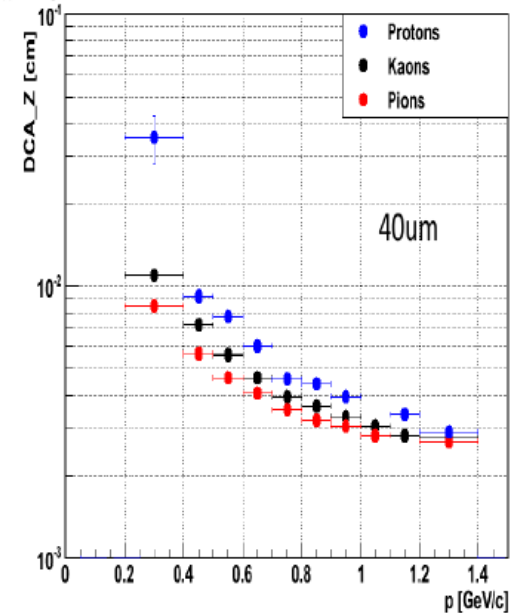
- **STAR-PXL PRELIMINARY results (courtesy of STAR collaboration) :**
 - Data collected with low luminosity (clean TPC environment)
 - Tracks traversing the ladders equipped with Al traces \mapsto resolution on DCA



ITS-TDR



STAR-PXL ($R\Phi$)



STAR-PXL (Z)

\Rightarrow 40/35 μm obtained for 700-800 MeV/c K^\pm/π^\pm in both directions

\mapsto very similar to ITS objectives

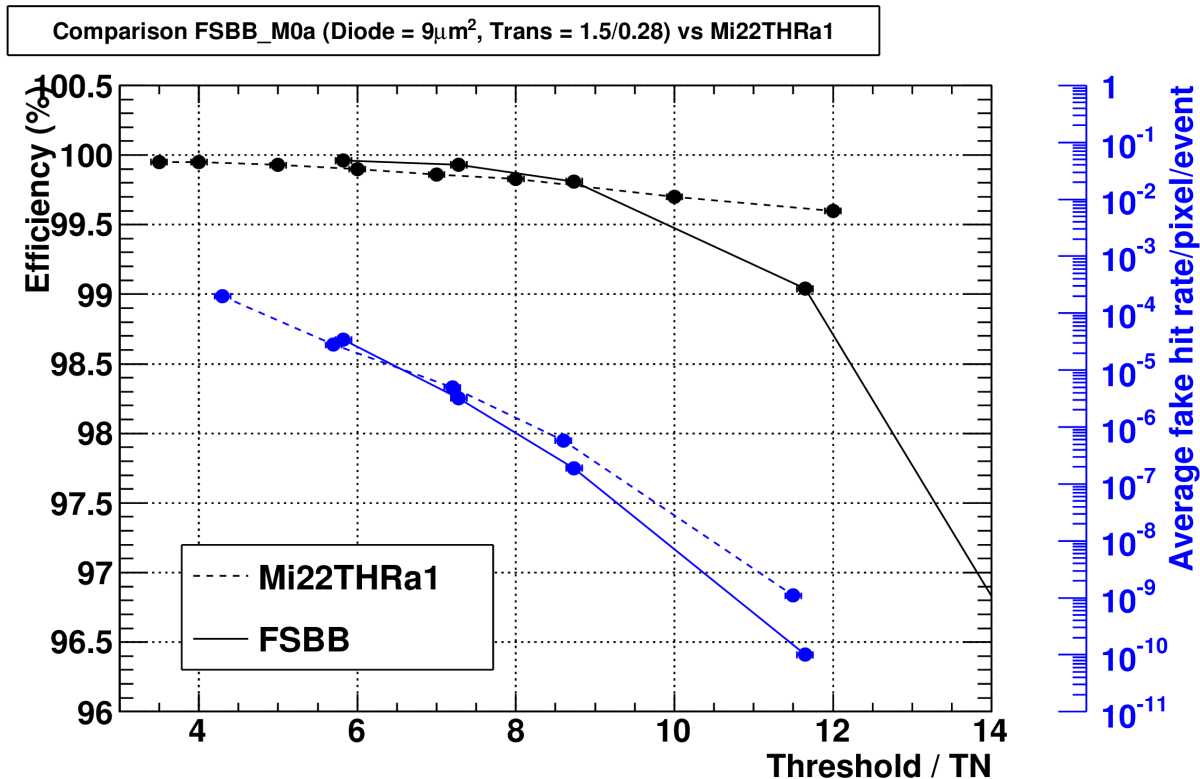
Comparison of Small Diode to MIMOSA-22THRa1

MIMOSA-22THRa1: 4.4 GeV e^- beam

- HR ($\sim 2\text{k}\Omega\text{cm}$) $20\mu\text{m}$ epitaxial layer
- 128 columns of 320 pixels
- No SDS, thresholds dispersion ignored
- Pixel dimensions: $22 \times 33\mu\text{m}^2$ ($11\mu\text{m}^2$ diode)
- Pixel amp input Trans: $L/W = 0.36/1\ \mu\text{m}$

FSBB-M0a (small diode): 120 GeV π^- beam

- HR ($\sim 1\text{k}\Omega\text{cm}$) $18\mu\text{m}$ epitaxial layer
- 2×208 columns of 416 pixels
- Discri. outputs processed with SDS
- Pixel dimensions: $22 \times 33\mu\text{m}^2$ ($9\mu\text{m}^2$ diode)
- Pixel amp. input Trans: $L/W = 0.27/1.5\ \mu\text{m}$
- **Noise increased by cross-coupling (mainly FPN)**



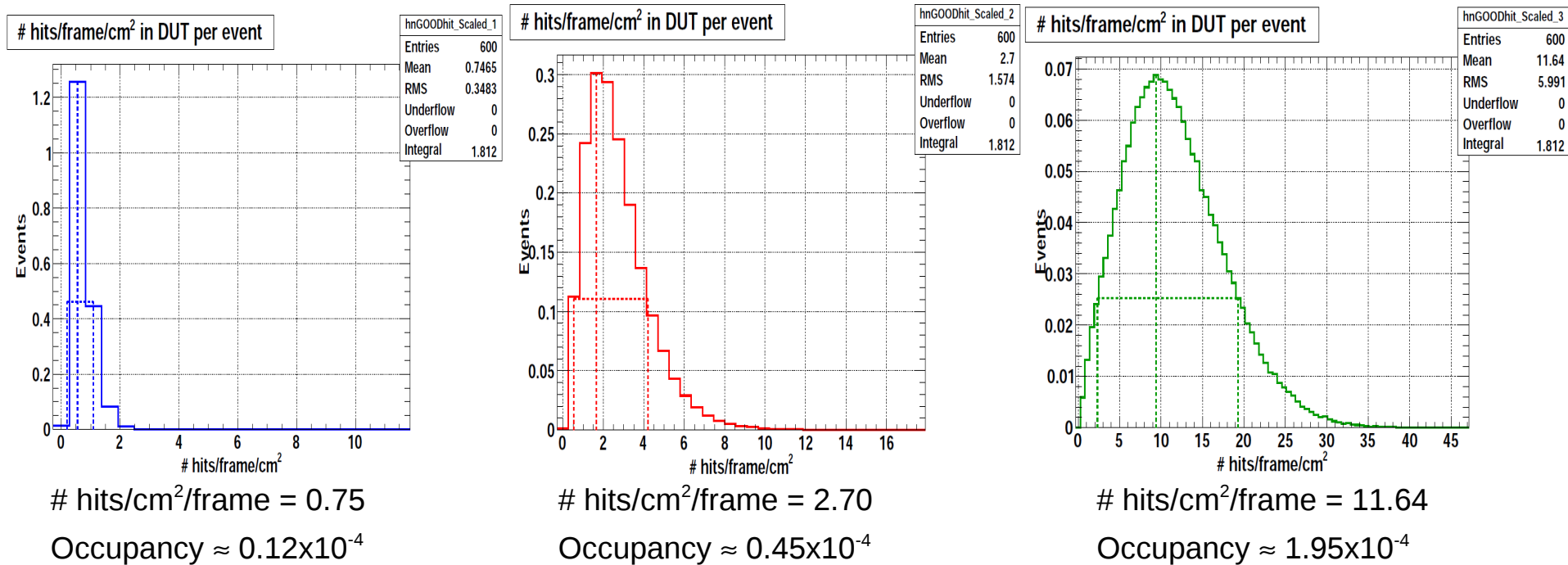
Beam-Test: Detection Performances vs Trigger Rate

- Data taken at different trigger rates: 2.5 (default value), 25 and 100 kHz
- Measurements performed with high threshold settings: 8mV

2.5 kHz

25 kHz

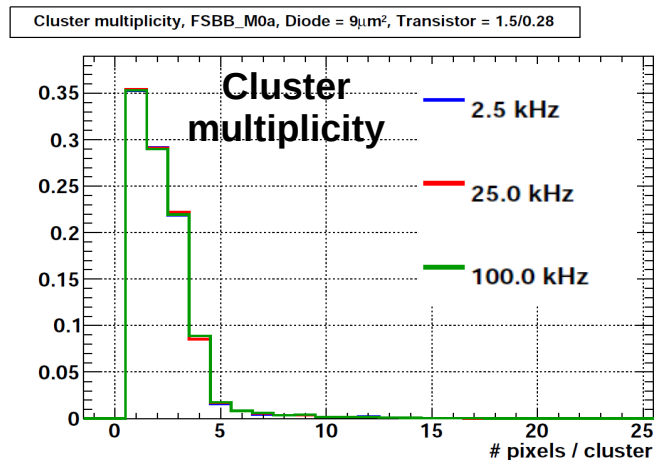
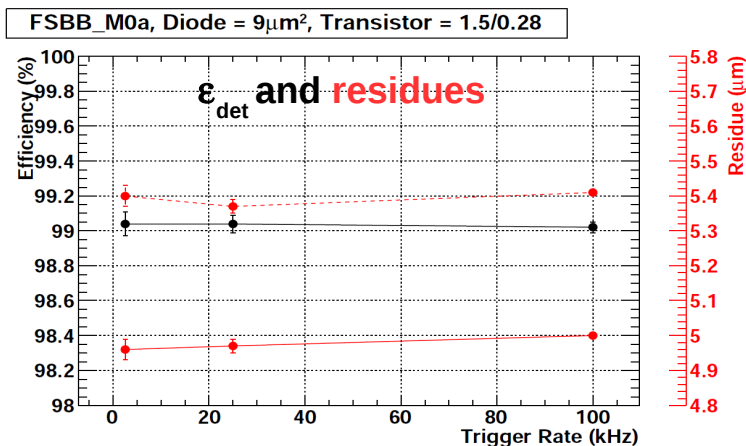
100 kHz



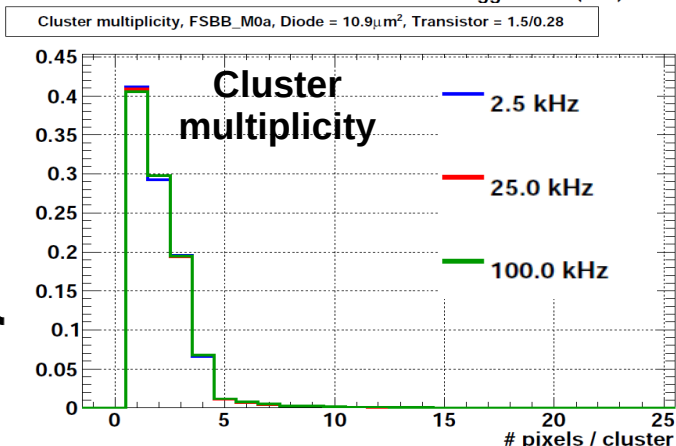
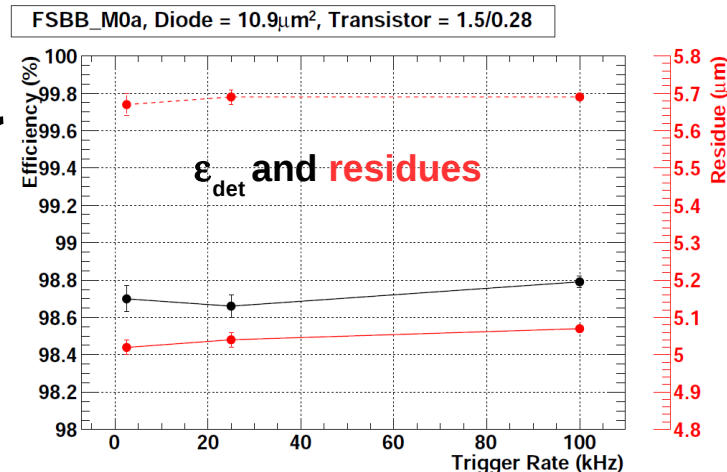
Beam-Test: Detection Performances vs Trigger Rate

- Data taken at different trigger rates: 2.5 (default value), 25 and 100 kHz
- Measurements performed with high threshold settings: 8mV

9 μm^2 Diode



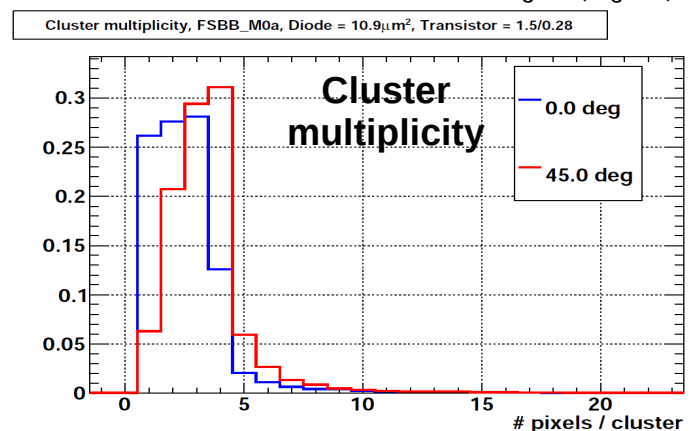
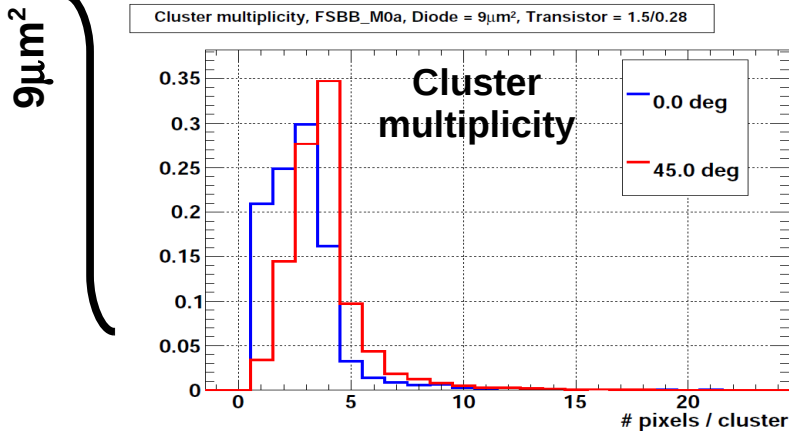
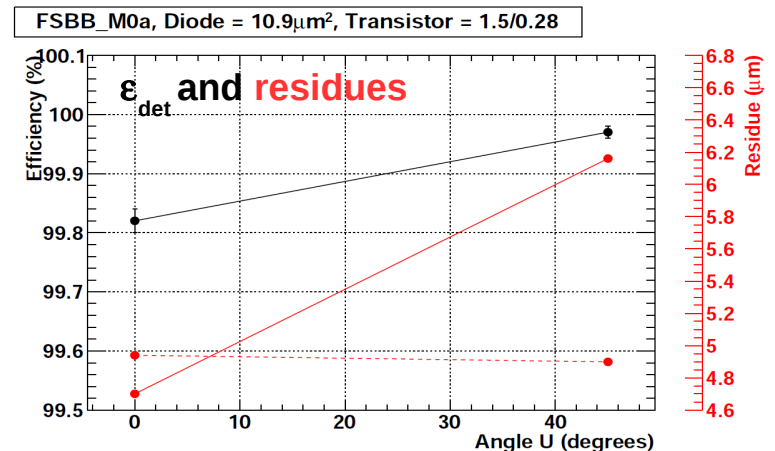
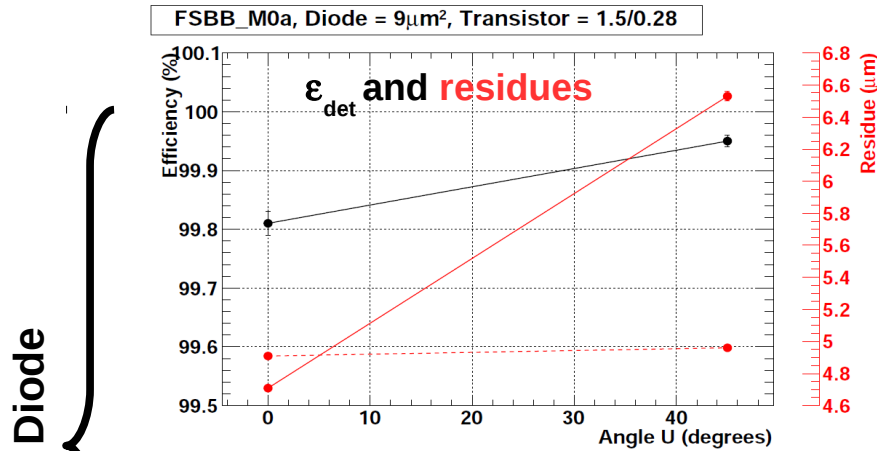
11 μm^2 Diode



- No sensitivity to hit rate observed** (deeper analysis under way)

Beam-Test: Detection Performances at High Incidence Angle

- Data taken with trigger rate of 2.5 kHz and 6mV threshold



- Increase in ϵ_{det} and multiplicity at high angles
- Increase in U-residue mainly due to the increase in multiplicity in this direction
- No change in V-residue as expected