CMOS pixel sensors (CPS): Prospects for a VTX detector @ ILC.

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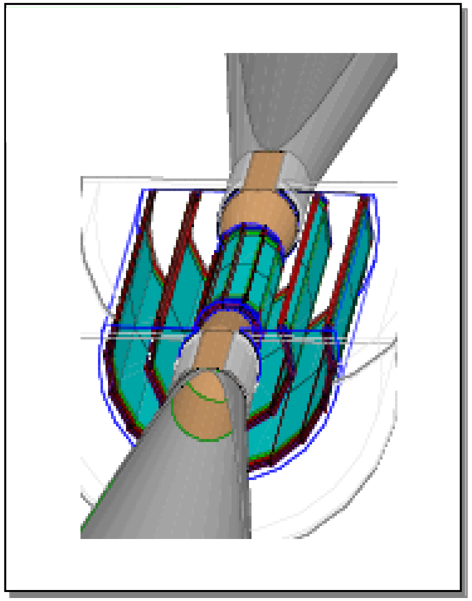
pour le groupe PICSEL (IPHC - Université de Strasbourg)

- Experimental conditions and performance goals
- CPS R&D roadmap for ILC-VTX

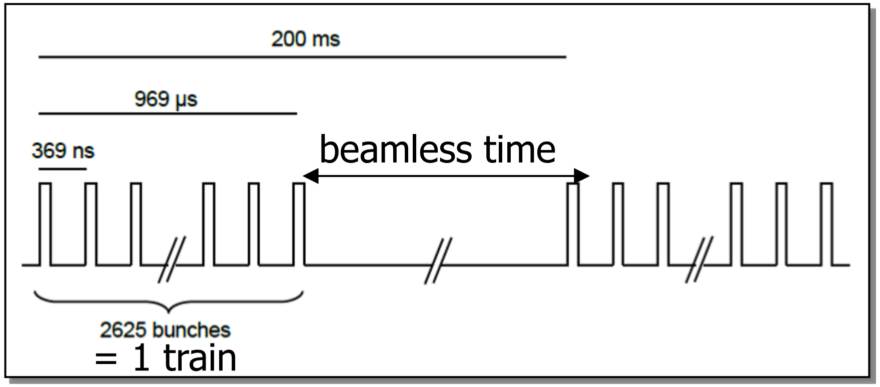


ILC Vertex detector :

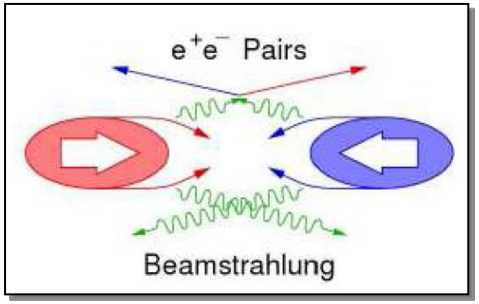
Experimental conditions and performance goals

ILC-VTX: reminder on experimental conditions

- Beam structure
  - 5 trains/s of ~2600 bunches
  - 1 bunch every ~ 300 ns
  - « Quiet time » of ~ 200 ms
  - Consequences
    - Read-out, No trigger
    - Cooling: Power pulsing



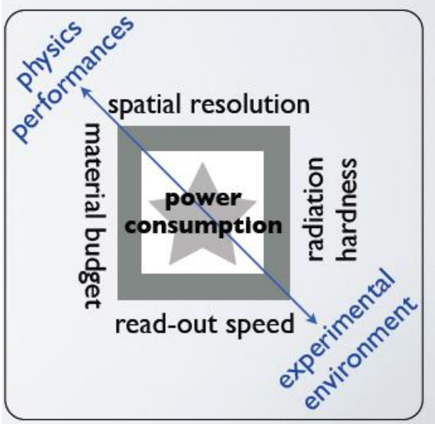
- Beam background :
  - Beamstrahlung: RMS energy loss:
    - δ_{BS} ~ 1% @ $\sqrt{s}$ = 250 GeV
  - Drives occupancy :
    - Read-out speed, Inner radius
    - Physics cross section: $e^+e^- \rightarrow$qqbar ~ 1 evt/s ⇨ negligible
  - Drives radiation level
    - Moderate (compared to LHC)
    - Vertex detector 1st layer: O(100) kRad/yr & O(10^{11}) n_{eq}(1MeV)/cm^2/yr



  - Typical value (first layer)
    - ~ 5 hits/cm^2/BX
    - High systematics !
  - Very sensitive to geometry and beam parameters
  - Safety factor needed !
    - at least x 5 !

- Possible read-out strategies:
  - Integrate a few bunches
  - Read-out between trains with time stamping
  - Read-out between trains without time stamping (very high granularity)

ILC vertex detector: squaring the circle



- Linear e+e- collider
  - Different approach compared to hybrid pixels & LHC
  - Experimental environment much less demanding (radiation tol. and speed)

⇨ favors technologies which allow to focus on resolution and material budget

- Vertex detector design and specifications
  - Physics performances $\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$
    - ➢ Spatial resolution: highly granular sensor: $\sigma_{R\phi} \sim 3\ \mu m$ (pitch ~ 17 μm)
    - ➢ multiple scattering : very low material budget O(0.15%X_0/layer)
    - ➢ b/c/τ tagging with high efficiency/purity, low momentum tracking, secondary vertex charge determination
  - Experimental environment constraints
    - ➢ Radiation hardness (ionising and non ion. rad.) ⇨O(100 kRad) & O(1x10^{11} $n_{eq\ (1MeV)}$) /year (layer 1)
    - ➢ Occupancy ⇦⇨Read-out speed ⇨ 1st layer: ~ 5 part/cm^2/BX ⇨ few % occupancy max
    - ➢ Power dissipation ⇦⇨ preferably air cooling ⇨ 600W/12W (Power cycling, ~3% duty cycle)
    - ➢ EM compliance (pick-up noise)
  - Read-out & electronics
    - ➢ Single Event Effect safety (Upset, latchup)
    - ➢ highly integrated read-out microcircuits
    - ➢ high data transfer rate (no trigger)
  - Other parameters
    - ➢ Costs, fabrication reliability and flexibility
    - ➢ Mechanical integration: low mass, rigidity, heat conductive
    - ➢ Geometry: short or long barrel ?
    - ➢ Alignment: micron level capabilities needed

⇨ reaching the specifications all together is the real challenge

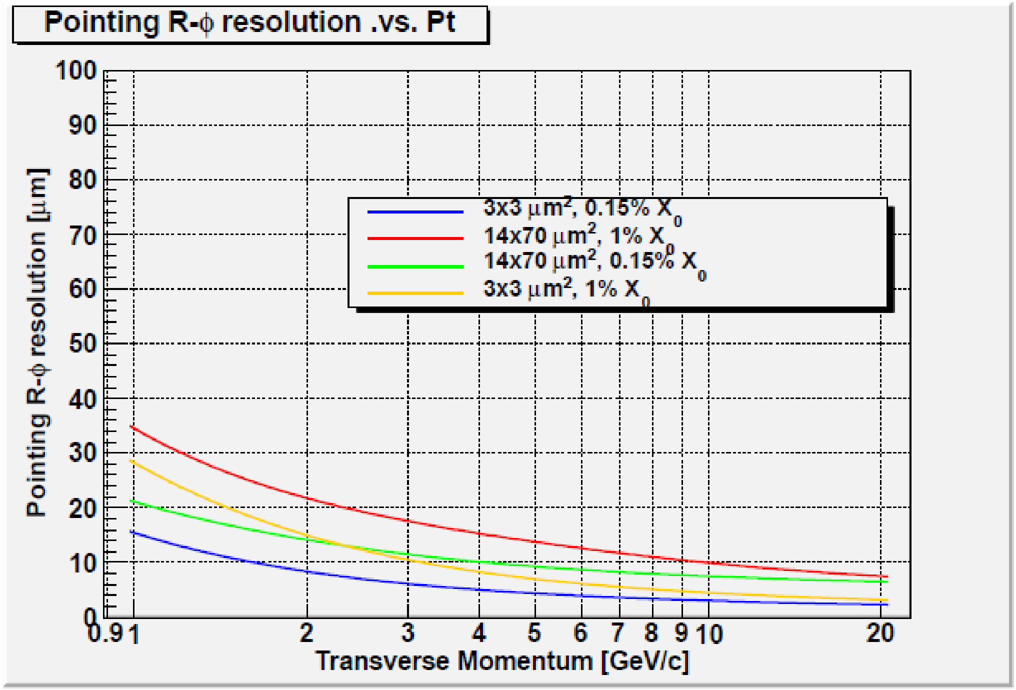
Expected Vertex performances: pointing resolution

- Compared pointing resolutions

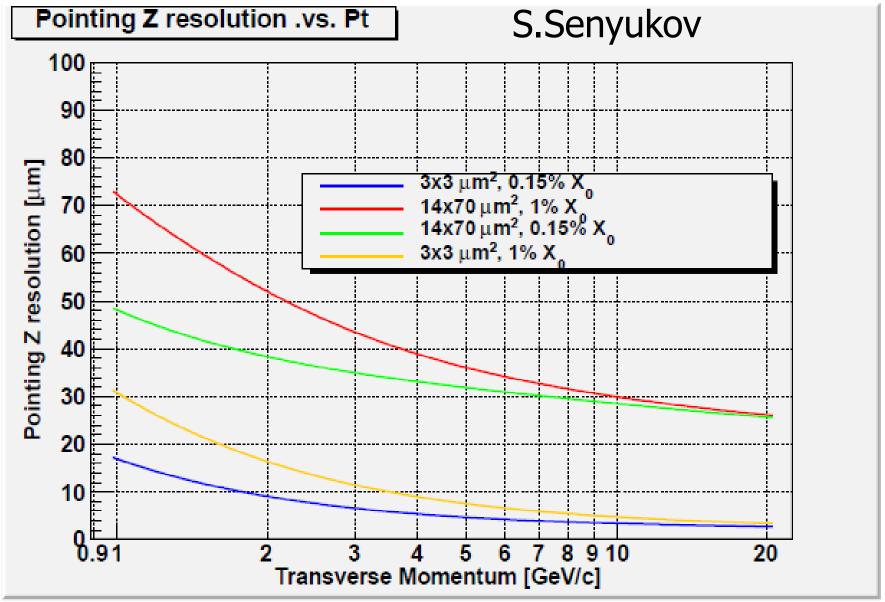
- LC VERTEXING GOAL : $\sigma_{R\phi,Z} \leq 5 \oplus 10 - 15/p \cdot sin^{3/2}\theta \ \mu m$

  ▷ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta$

__ ILC baseline
__ ILC mat.budget/layer 0.15%X_0 ⇨1%X_0
__ ATLAS-IBL
__ ATLAS-IBL with ILC mat.budget



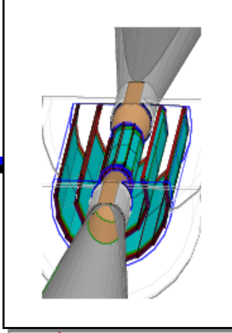
Pointing R-φ resolution .vs. Pt



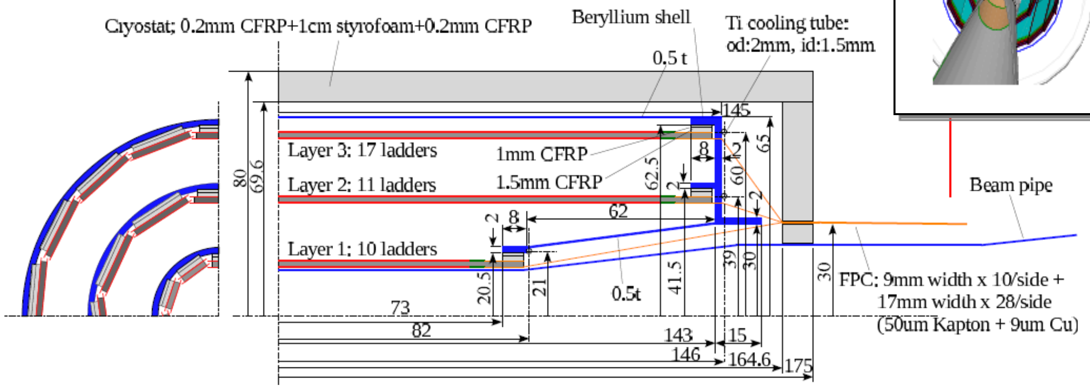
Pointing Z resolution .vs. Pt

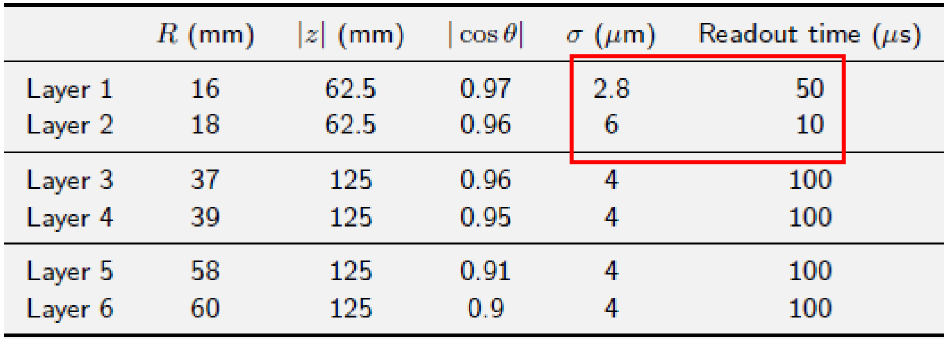
S.Senyukov

ILD: Vertex detector

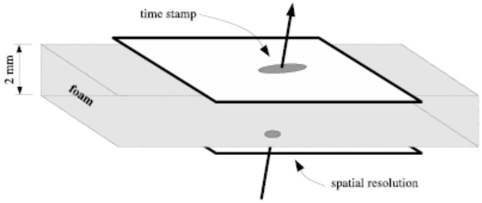


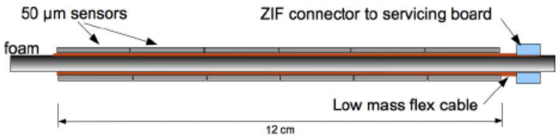
- Layout (DBD geometry):
  - Long Barrel approach
  - Radius: ~15 mm – 60mm
  - 3 x double sided ladders
    - Optimize material budget / alignment.
    - Stand alone tracking improvment
    - Background tagging capabilities
    - Other option: 5 single sided layers
  - Layers 1 / 2:
    - Priority to read-out speed & spatial resolution
    - Small pixels: 17 x 17 / 34-102 μm^2
    - Binary charge encoding
    - Read-out time ~ 50 / 25-5 μs
    - σ_{sp} ~ 3 / >~5 μm
  - layers 3 – 6
    - Optimized for power consumption
    - Large pixels (25/35 x 35 μm^2)
    - 3-4 bits charge encoding
    - Read-out time ~ 60 μs
    - σ_{sp} ~ 4 μm
- Occupancy @ √s = 500 GeV
  - Taking into account cluster multiplicity
  - L1 ⇨ ~ 10^{-2} / 50 μs
  - L2 ⇨ ~ 10^{-3} / 5 μs





	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6	10
Layer 3	37	125	0.96	4	100
Layer 4	39	125	0.95	4	100
Layer 5	58	125	0.91	4	100
Layer 6	60	125	0.9	4	100

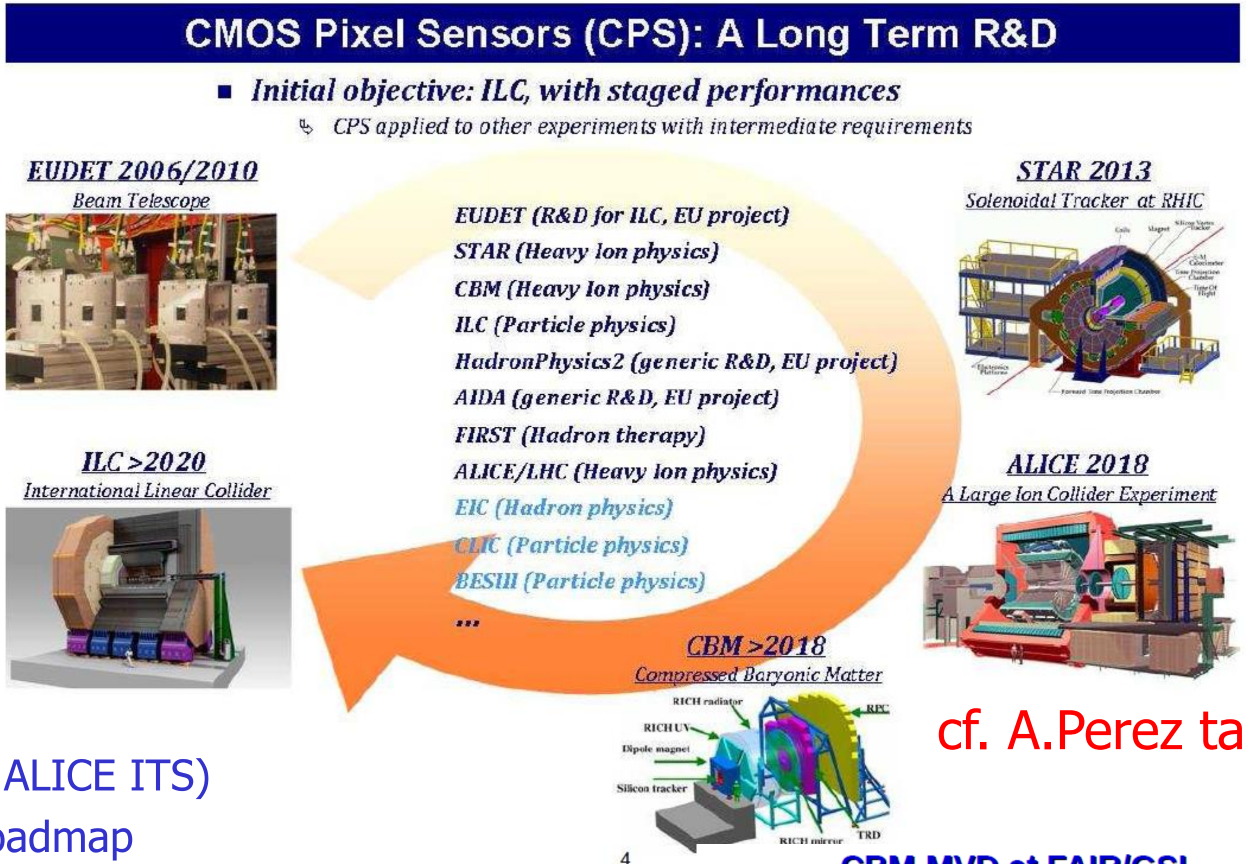




ILC Vertex detector :

- CPS R & D roadmap for ILC-VTX

CMOS Pixel Sensors roadmap



CMOS Pixel Sensors (CPS): A Long Term R&D

- *Initial objective: ILC, with staged performances*
  - ↳ *CPS applied to other experiments with intermediate requirements*

EUDET 2006/2010
Beam Telescope

STAR 2013
Solenoidal Tracker at RHIC

ILC >2020
International Linear Collider

ALICE 2018
A Large Ion Collider Experiment

CBM >2018
Compressed Baryonic Matter

EUDET (R&D for ILC, EU project)
STAR (Heavy Ion physics)
CBM (Heavy Ion physics)
ILC (Particle physics)
HadronPhysics2 (generic R&D, EU project)
AIDA (generic R&D, EU project)
FIRST (Hadron therapy)
ALICE/LHC (Heavy Ion physics)
EIC (Hadron physics)
CLIC (Particle physics)
BESIII (Particle physics)
...

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cf. A.Perez talk

- State of the art: (STAR and ALICE ITS)
- Pixel sensor development roadmap
  - Exploit fully the CPS potential
    - ➢ Granular, thin, integrated FEE, industrial and cheap
  - R&D performed in synergy with other applications
    - ➢ EUDET, STAR, ALICE, CBM, AIDA, etc.
  - Adress trade-off between resolution and speed
  - Adress double sided ladder development (alignment, mat.budget, power cycling, etc.)

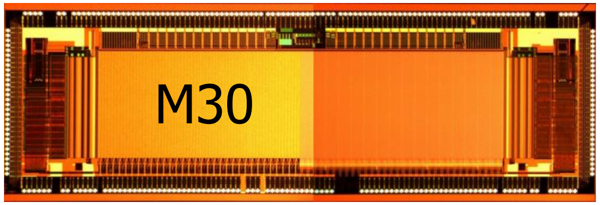
CBM-MVD at FAIR/GSI

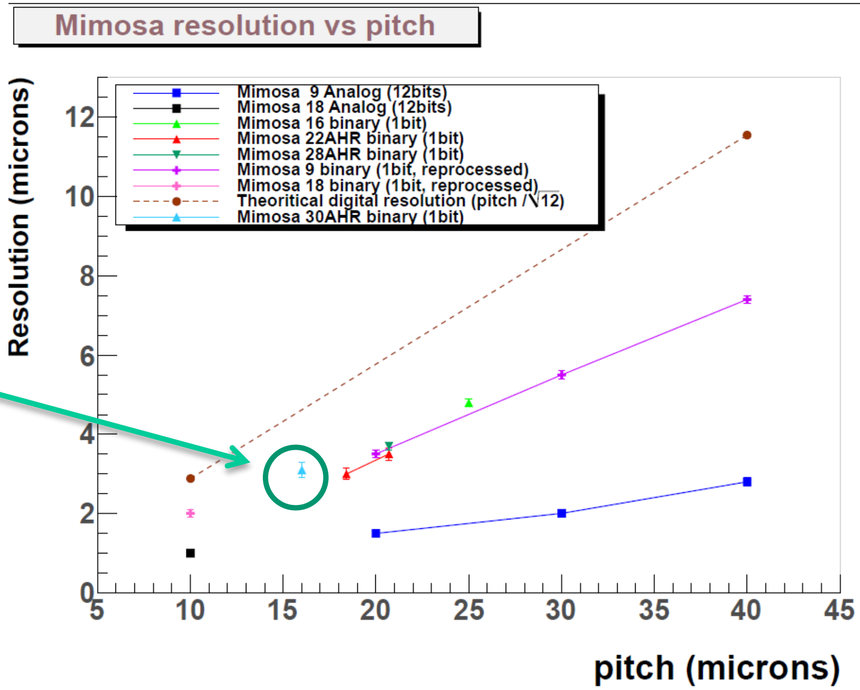
3 double-sided stations in vacuum at T < 0°C

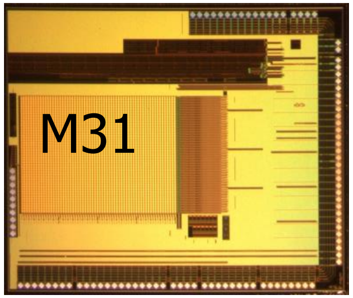
- $\sigma_{sp} \lesssim 5\ \mu m$
- ~ 0.5 % X_0 / station
- Radiation load $\gtrsim 10^{13} n_{eq}/cm^2$

Validation of the concept : 0.35 µm technology

- Inner most layer: Mimosa-30 fabricated
  - 0.35 µm process with high resistivity epitaxy
  - In pixels CDS, rolling shutter read-out, binary sparsified output
  - Column length ~ final sensor (~ 5 mm)
  - High resolution side (16 x 16 µm^2)
    - ➢ 128 col (discri) x 256 rows
    - ➢ Read-out time ~≤ 50 µs
    - ➢ Beam test: σ_{sp}~ 3 µm
  - Time stamping side (16 x 64 µm^2)
    - ➢ 128 col (discri) x 64 rows
    - ➢ Lab tests: Noise ~ 15 e- and discris ok for
    - ➢ Read-out time ~ 10 µs
- Outer most layer: Mimosa31 fabricated
    - ➢ 0.35 µm process
    - ➢ 35 x 35 µm^2 (power saving)
    - ➢ 48 col x 64 rows
    - ➢ Col. ended with 4 bits ADC
  - Read-out time ~ 10 µs (1/10 of full scale)
    - ➢ ⇨ 100 µs expected on full scale



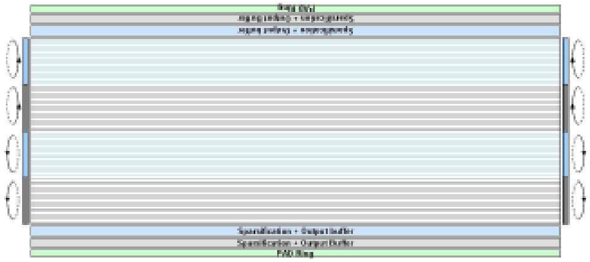




Improving read-out speed

- State of the art (fab. process: 0.35 µm)
  - STAR: O(100 ns) / row ⇨ ~ 60/30 µs (17/33 µm pitch)
- Motivations for faster read-out
  - Robustness w.r.t. predicted beam background @ √s = 0.5 TeV
  - Standalone tracking (e.g. low momentum tracks)
  - Compatibility with high luminosity and √s = 1 TeV
- Strategies to accelerate read-out (ALICE-ITS upgrade: MISTRAL/ASTRAL/ALPIDE)
  - Read-out from both side ⇨ x2 (moderate additional mat. budget)
  - Elongated pixels (17 µm ⇨33 µm or more) ⇨ x 2
  - Read-out simultaneously 2 or 4 rows ⇨ x2-4 (MISTRAL)
  - Subdivide arrays in 4 sub-arrays read-out in // ⇨x4
    - ➢ Achievable in 0.18 µm process (6-7 Metal layers)
  - In pixel discriminators ⇨ ASTRAL
  - Different read-out strategy: Asynchronous ⇨ ALPIDE

cf. A.Perez talk

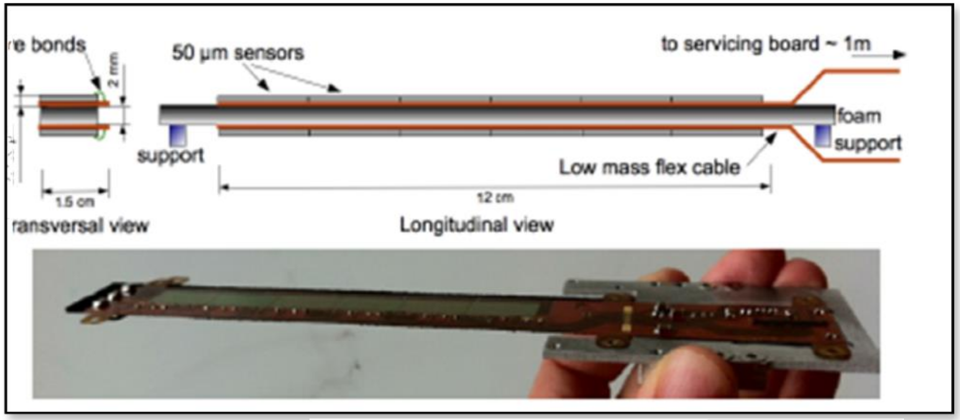


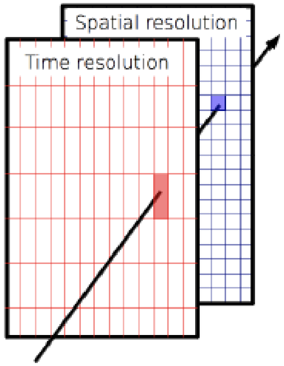
- Expected VTX performances
  - @ 1 TeV /0.5 TeV

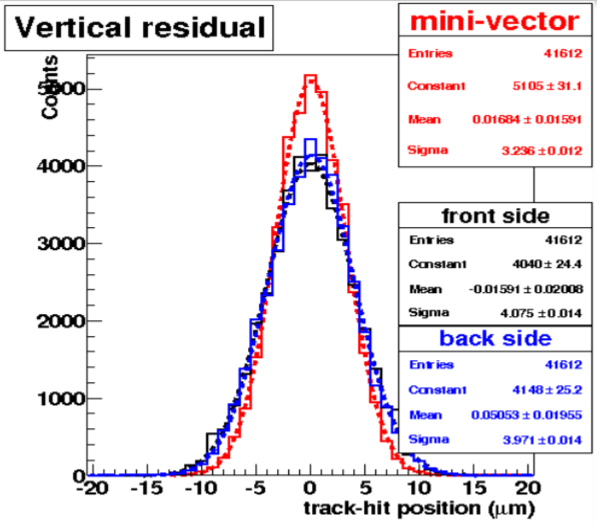
Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	**Occupancy [%]** 1 TeV (0.5 TeV)	**Power** inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs (8 μs)	4.5(0.9) / 0.5(0.1)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs (100 μs)	1.5(0.3) / 0.2(0.04)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs (100 μs)	0.3(0.06) / 0.05(0.01)	200/4 W

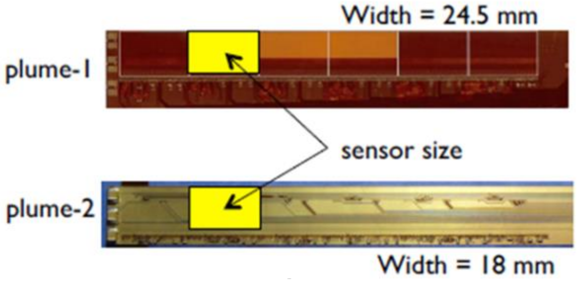
Sensor integration in Ultra Light Devices

- Double sided ladders expected benefits
  - Alignment & tracking (pointing)
  - Beam background rejection ?
  - Material budget, 1 mechanical support
  - Redundancy (efficiency)
  - Each layer optimized
    - read-out speed vs resolution
- PLUME coll. (Bristol, DESY, IPHC)
- Plume 01 prototype (<2012)
  - Fabricated
    - 2 x 6 Mimosa 26 chips
    - 2 mm low density SiC foam
    - Validated in test beam (2011)
    - Operated with air cooling
    - 0.6 % X_0
- Plume 02 prototype
  - Under construction (spring 2015)
  - Reduced mat. Budget
    - Reduced width (24.5 mm ⇨18mm)
    - Lighter (alu) flex cable, mechanical support
    - 0.6 % X_0 ⇨ ~ 0.35 % X_0 (cross-section)





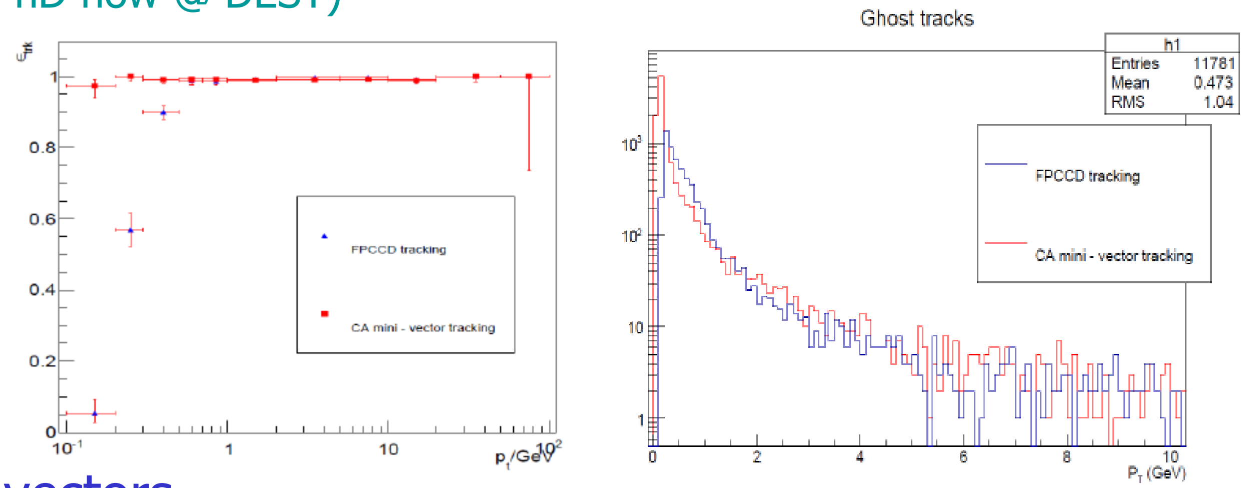




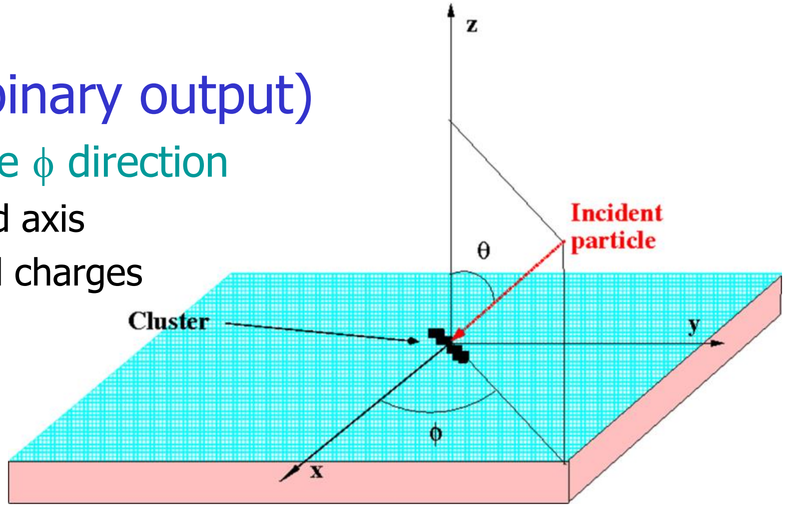
Vertexing, tracking, background and alignment studies

- Tracking with mini vectors
  - G.Voutsinas (former PhD now @ DESY)

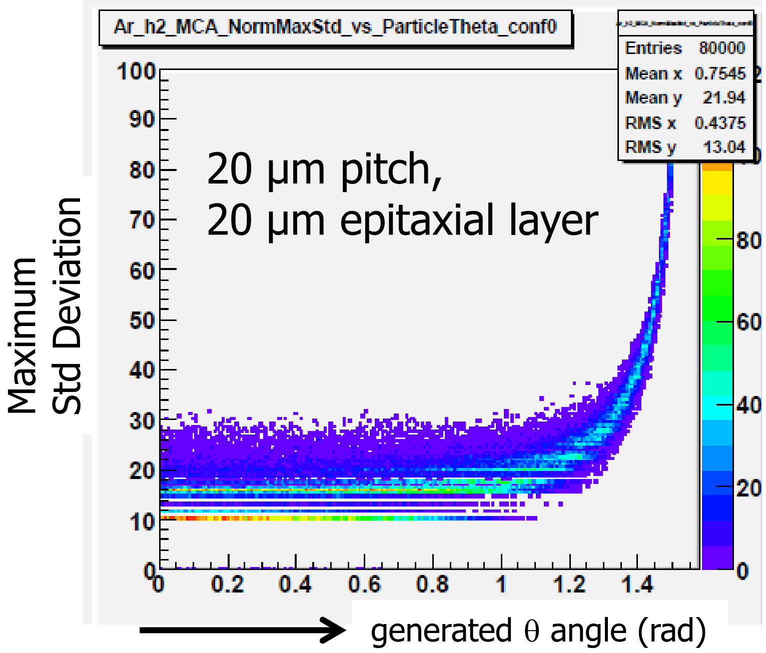
Sample: ttbar, √s = 500 GeV, fast CMOS VXD, pair bkg overlayed

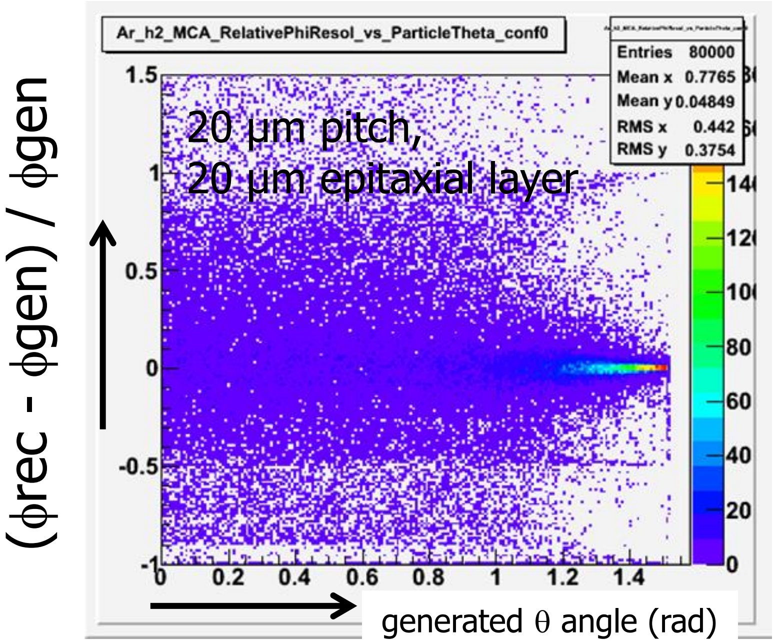


- Alignment with mini-vectors
  - L.Cousin: see his talk.
- Beam background identification (with pixel binary output)
  - When θ is large, clusters should be elongated in the ϕ direction
    - ➢ Main component analysis allows to find the elongated axis
    - ➢ Main Axis = Axis where the Variance of the projected charges is maximum
    - ➢ Variance related to θ (and also cluster multiplicity)
    - ➢ Main axis direction related to ϕ
    - ➢ Use CMOS digitzer based on test beam data.



Incident angle reconstruction (AMS 0.35 µm, High resistivity, preliminary)





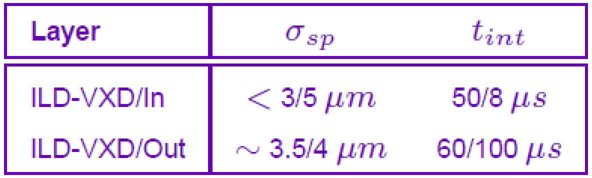
Minimal θ angle where standard deviation on theta_gen ~< 10º
(the systematic bias is small ~< 5%)

	Epi ~ 10 µm	Epi ~ 20 µm	Epi ~ 30 µm
θ Reconstruction (deg)	~ 80º	~ 70º	~ 65º
ϕ Reconstruction (deg)	~ 70º	~ 57º	~45º

Minimal θ angle where standard deviation on (ϕrec – ϕgen) / (ϕgen) ~< 5º

Summary and plans

- R & D in CPS: Well established architecture achieved
  - Successfully equipped STAR-PXL (0.35 μm process, ~ 360 Mpixels)
  - Extendable to ILC-VTX

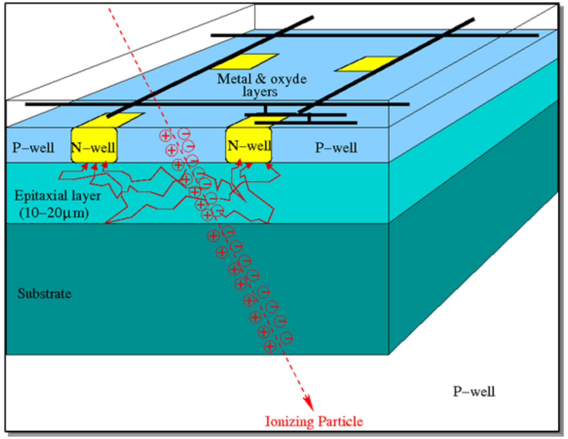


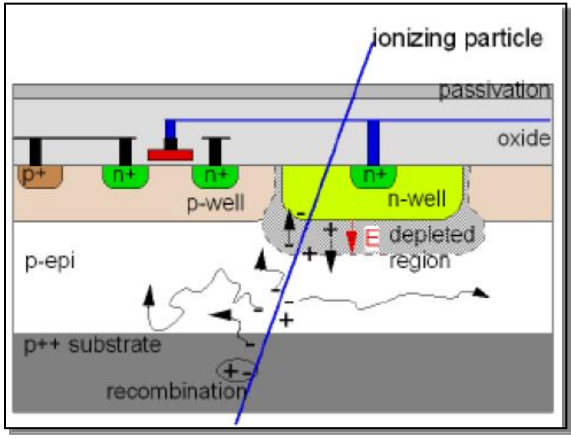
Layer	σ_{sp}	t_{int}
ILD-VXD/In	$<$ 3/5 μm	50/8 μs
ILD-VXD/Out	$\sim$ 3.5/4 μm	60/100 μs

- 0.18 μm fab. process benefits ⇨ should allow to go further
    - ➢ Standalone tracking, bunch tagging, High E/Lumi running, etc.
  - 6 Metal. Layers ⇨ higher μcircuits density, Deep P-well ⇨ PMOS & NMOS in pixels transistors
  - Access to high resistivity (few kΩ.cm), Access to sizeable epitaxy thickness.
  - Full Scale Building Block (FSBB) validated in test beam (A.Perez talk)
- 2 sided ladders: PLUME collab.
  - Concept validated ⇨On the way to achieve 0.35% X_0
  - Next:
    - ➢ 2 complementary sides
    - ➢ Validate power pulsing in mag. Field
    - ➢ Investigate possibilities to reach < 0.3 % X_0
- Beyond 2014 in 0.18 μm fab. process
  - Final ALICE-ITS sensor and CBM-MVD variant in 2015
  - Develop fast read-out in pixel fast shaping & discri. ⇨O(1 μs) ⇨ bunch tagging
  - Validate 3-bit charge encoding ADC concept (outer layers)
  - Investigate Fine pixels (delayed read-out)
  - Fabricate dedicated ILC sensors in 0.18 μm process -> ~2018

Back up

CMOS pixel sensor (CPS) for charged particle detection

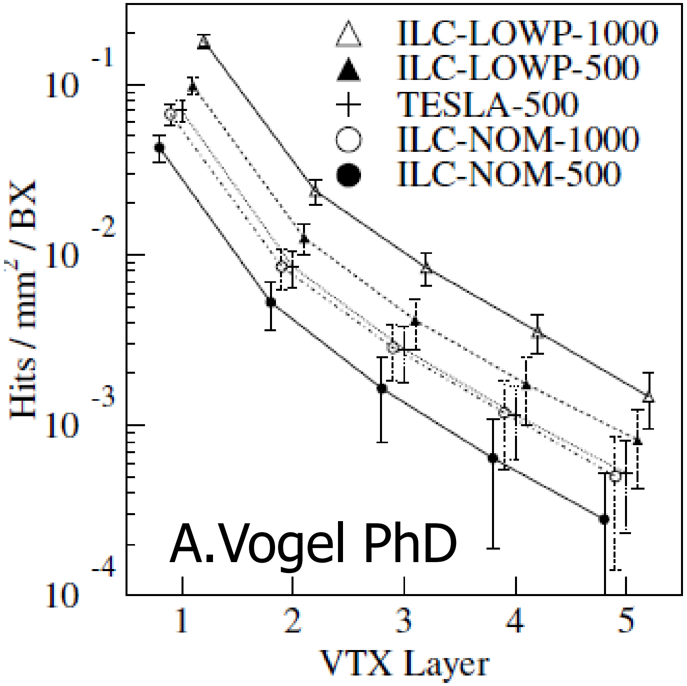


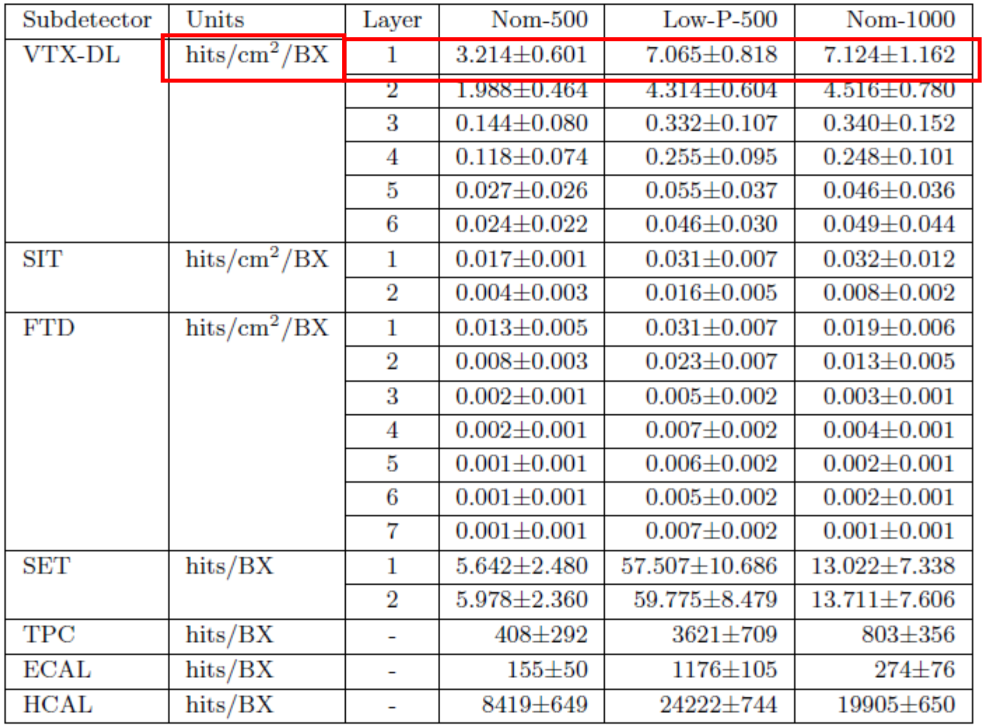


- Main features
  - Monolithic, p-type Si
    - Signal created in low doped thin epitaxial layer ~10-20 µm
    - ~ 80 e- /µm ⇨ total signal ~ O(1000 e-)
  - Thermal diffusion of e-
    - Limited depleted region
    - Interface highly P-doped region: reflection on boundaries
  - Charge collection: N-Well diodes
    - Charge sharing ⇨ resolution
  - Continuous charge collection
    - No dead time
- Main Avantages
  - Granularity
    - Pixel pitch down to 10 x 10 µm^2 ⇨spatial resolution down to ~ 1 µm)
  - Material budget
    - Sensing part ~ 10-20 µm ⇨ whole sensor routinely thinned down to 50 µm
  - Signal processing integrated in the sensor
    - Compacity, flexibility, data flux
  - Flexible running conditions
    - From ≤ 0°C up to 30-40°C if necessary
    - Low power dissipation (~ 150-250 mW/cm^2) ⇨ material budget
    - Radiation tolerance: >~100s kRad and O(10^{12} n_{eq}) ⇨f(T,pitch)
  - Industrial mass production
    - Advantages on costs, yields, fast evolution of the technology, Possible frequent submissions
- Main limitations
  - Industry adresses applications far from HEP experiments concerns
    - Different optimisations on the parameters on the technologies
  - Recently: new accessible processes:
    - Smaller feature size, adapted epitaxial layer
    - Open the door for new applications

Beam background in various detectors (ILD example)

- (A.Vogel, DBD, De Masi, etc.)
- 100 BX simulated
  - Pair induced background
  - Depends on √s
  - 20 % due to back scatterers
  - Statistical error only
    - ➢ systematics much higher

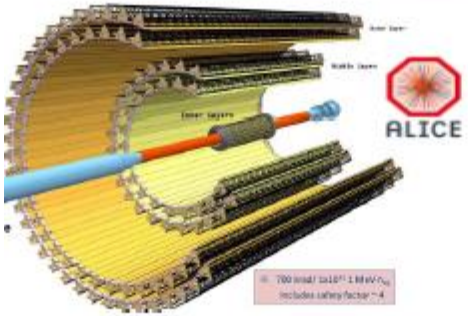




Subdetector	Units	Layer	Nom-500	Low-P-500	Nom-1000
VTX-DL	hits/cm^2/BX	1	3.214±0.601	7.065±0.818	7.124±1.162
		2	1.988±0.464	4.314±0.604	4.516±0.780
		3	0.144±0.080	0.332±0.107	0.340±0.152
		4	0.118±0.074	0.255±0.095	0.248±0.101
		5	0.027±0.026	0.055±0.037	0.046±0.036
		6	0.024±0.022	0.046±0.030	0.049±0.044
SIT	hits/cm^2/BX	1	0.017±0.001	0.031±0.007	0.032±0.012
		2	0.004±0.003	0.016±0.005	0.008±0.002
FTD	hits/cm^2/BX	1	0.013±0.005	0.031±0.007	0.019±0.006
		2	0.008±0.003	0.023±0.007	0.013±0.005
		3	0.002±0.001	0.005±0.002	0.003±0.001
		4	0.002±0.001	0.007±0.002	0.004±0.001
		5	0.001±0.001	0.006±0.002	0.002±0.001
		6	0.001±0.001	0.005±0.002	0.002±0.001
		7	0.001±0.001	0.007±0.002	0.001±0.001
SET	hits/BX	1	5.642±2.480	57.507±10.686	13.022±7.338
		2	5.978±2.360	59.775±8.479	13.711±7.606
TPC	hits/BX	-	408±292	3621±709	803±356
ECAL	hits/BX	-	155±50	1176±105	274±76
HCAL	hits/BX	-	8419±649	24222±744	19905±650

- typical value (first layer)
  - ➢ ~ 5 hits/cm^2/BX
- Very sensitive to geometry and beam parameters
- Safety factor needed !
  - ➢ at least x 5 !

Next Forthcoming device: CBM Micro-Vertex Detector (MVD)

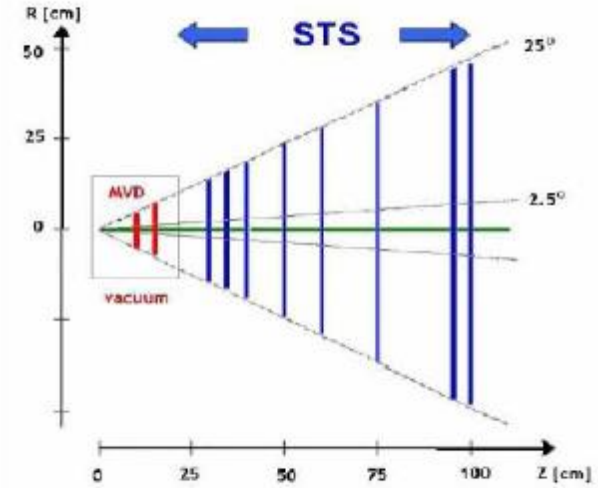


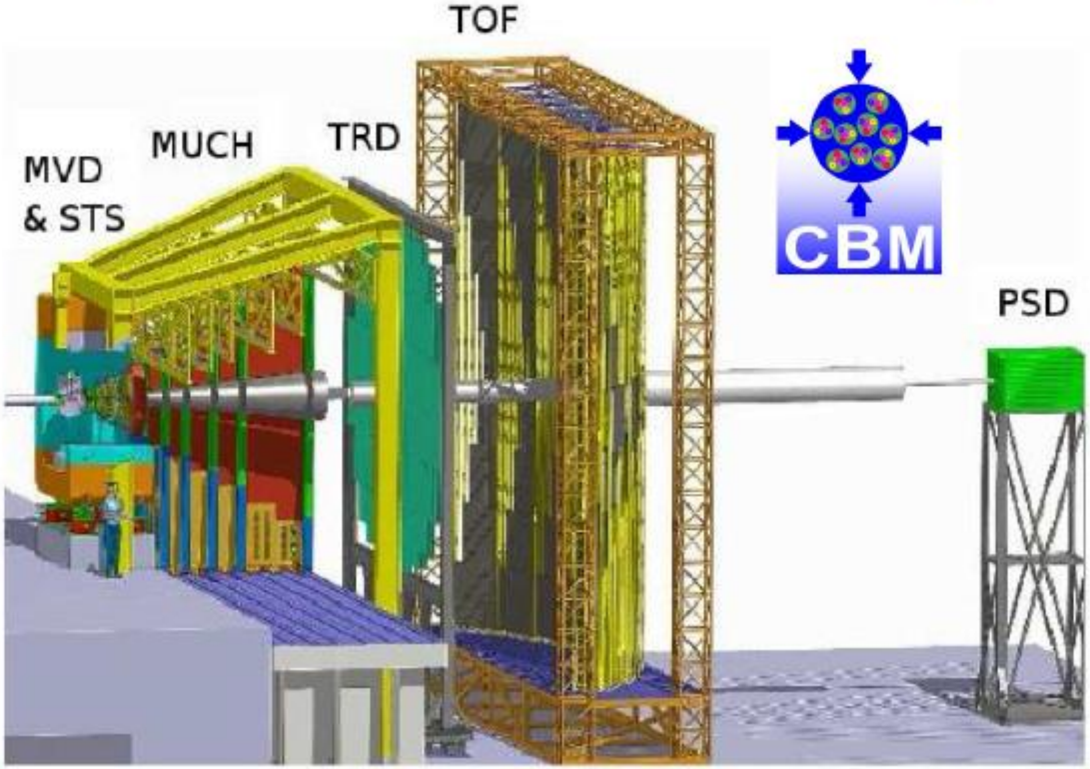
ALICE-ITS 2018/19

CBM-MVD at FAIR/GSI

3 double-sided stations in vacuum at T < 0°C

- $\sigma_{sp} \lesssim 5\ \mu m$
- ~ 0.5 % X_0 / station
- Radiation load $\gtrsim 10^{13} n_{eq}/cm^2$

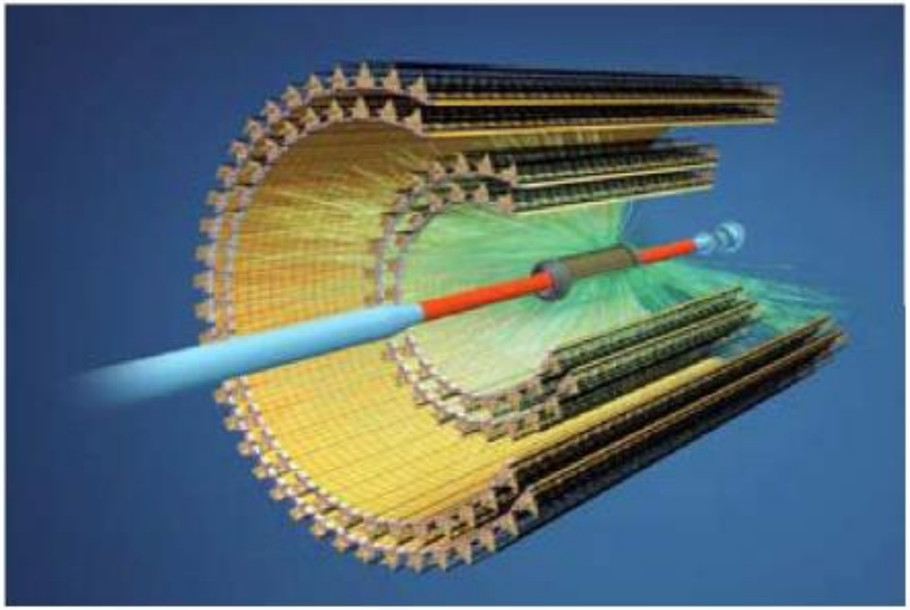




Next Challenge : ALICE-ITS Upgrade

Upgrade of ITS **entirely based on CMOS Pixel Sensors (CPS)** :

- Present geometry: 6 layers
  HPS x 2 / Si-drift x 2 / Si-strips x 2
- Future geometry : 7 layers $\mapsto$ $\mapsto$ $\mapsto$
  all with CPS ($\sim$ 25-30 · 10^3 chips)
  $\Rrightarrow$ 1st large tracker (10 m^2) using CPS
- ITS-TDR approved March 2014 :
  Pub. in J.Phys. G41 (2014) 087002



Requirements for ITS inner and outer barrels compared to specifications of STAR-PXL chip :

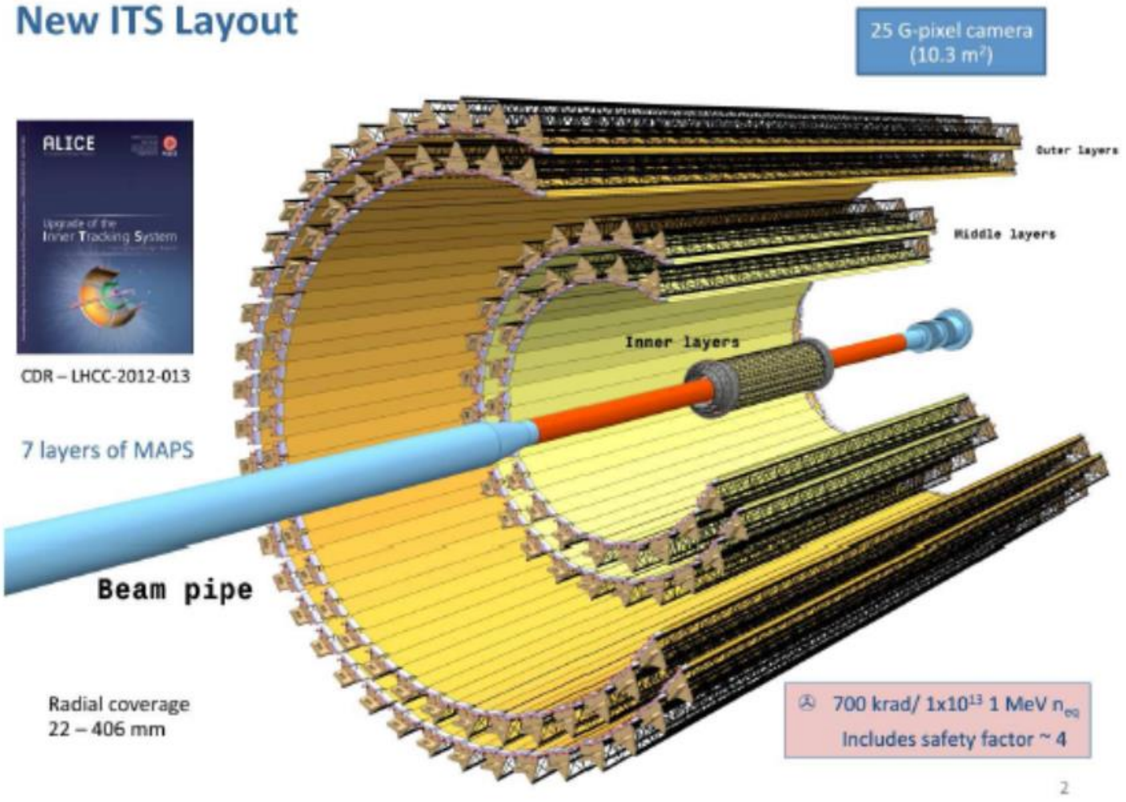
	σ_{sp}	$t_{r.o.}$	Dose	Fluency	T_{op}	Power	Active area
STAR-PXL	$< 4\ \mu m$	$< 200\ \mu s$	150 kRad	$3 \cdot 10^{12}\ n_{eq}/cm^2$	30-35°C	160 mW/cm^2	0.15 m^2
ITS-in	$\lesssim 5\ \mu m$	$\lesssim$ **30** μs	**700 kRad**	**$1 \cdot 10^{13}\ n_{eq}/cm^2$**	30°C	$< 300\ mW/cm^2$	0.17 m^2
ITS-out	$\lesssim 10\ \mu m$	$\lesssim$ **30** μs	15 kRad	$4 \cdot 10^{11}\ n_{eq}/cm^2$	30°C	$<$ **100 mW/cm^2**	$\sim$ **10 m^2**

$\Rrightarrow$ **0.35 μm CMOS process (STAR-PXL) not suited to read-out speed & radiation tolerance**

Next Progress Carrier : ALICE-ITS Upgrade

- Vx Det. (3 layers) + Tracker (4 layers, 10 m^2) : 5 μm, 20-30 μs, 700 kRad & $10^{13} n_{eq}/cm^2$ at 30°C
- 2 alternative sensors developped :
  - Baseline : **ASTRAL** (in-pixel discri.)
    - ↪ $\gtrsim$ 15 μs, 85 mW/cm^2
  - Back-up : **MISTRAL** (end-of-col. discri.)
    - ↪ $\gtrsim$ 30 μs, $<$ 200 mW/cm^2
- All main components validated in 2013 :
  - sensing node properties
  - in-pixel ampli+CDS
  - in-pixel discriminators
  - rolling-shutter with end-of-col. discri.
  - simultaneous 2-row read-out
  - sparse data scan
  - programmable chip steering (JTAG)
    - ↪ **outcome integrated in ITS-TDR**

New ITS Layout



25 G-pixel camera ($10.3 m^2$)

CDR – LHCC-2012-013

7 layers of MAPS

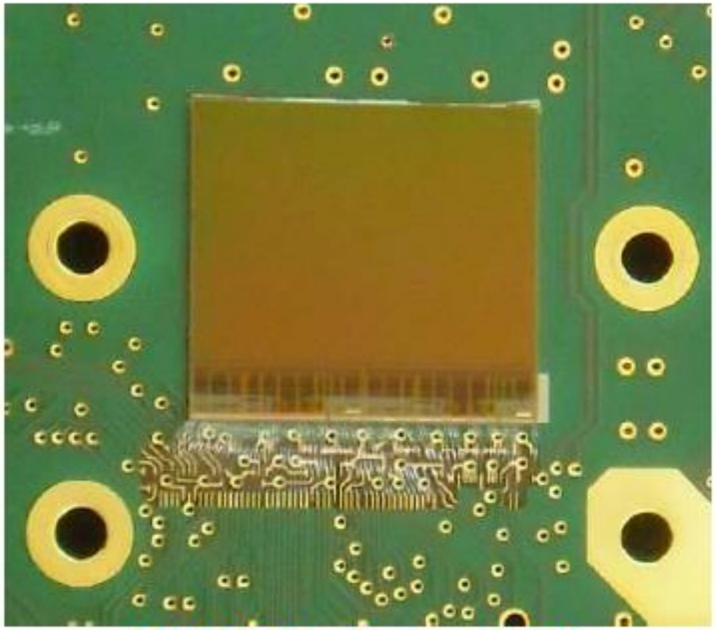
Radial coverage
22 – 406 mm

700 krad/ $1x10^{13}$ 1 MeV n_{eq}
Includes safety factor ~ 4

2

Upcoming Sensors (Partly) Based on the ALICE Development

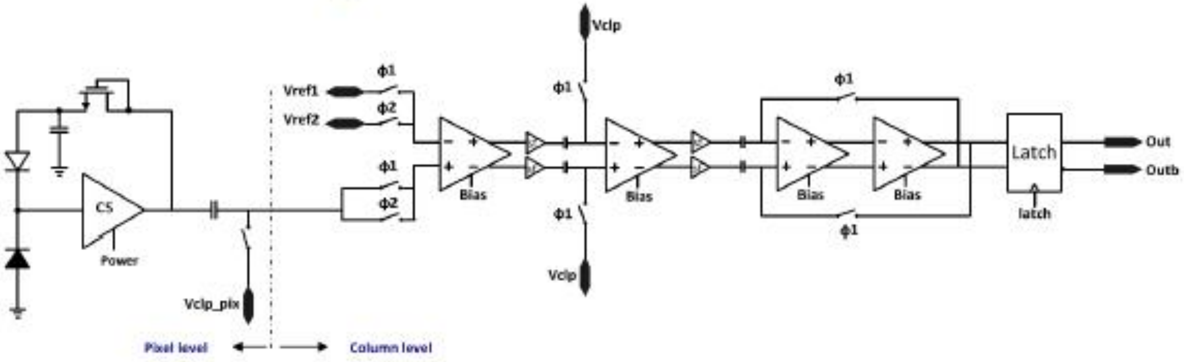
- **Spin-off of MISTRAL :**
  - best suited to reach $\lesssim 2.8\ \mu m$ resolution in L1
  - BUT pixels of 17 $\mu m \times$ 17 $\mu m \Rrightarrow\ \sim 50\ \mu s$ r.o. time
- **Spin-offs of ASTRAL :**
  - L2 : pixels of 17 $\mu m \times$ 102 $\mu m \Rrightarrow\ \sim 7\ \mu m \oplus 2.5\ \mu s$
  - L1 & L2 : pixels of 22 $\mu m \times$ 33 $\mu m \Rrightarrow$ 5 $\mu m \oplus 8\ \mu s$
    $\hookrightarrow$ mini-vectors $\equiv 3.5\ \mu m \oplus$ 4-8 μs
  - L3-L6 : pixels of $\lesssim 22\ \mu m \times$ 33 $\mu m \Rrightarrow$ 4-5 $\mu m \oplus 8\ \mu s$
- **Spin-offs of ALPIDE :**
  - L2 : pixels of 25 $\mu m \times$ 25 $\mu m \Rrightarrow$ 5 $\mu m \oplus < 5\ \mu s$
  - L2 : pixels of 15 $\mu m \times$ 125 $\mu m \Rrightarrow$ 8 $\mu m \oplus < 1\ \mu s$ reachable ?
- **Spin-offs of MIMOSA-31, MISTRAL & MIMADC :**
  - L3-L6 : pixels of 35 $\mu m \times$ 35 $\mu m \Rrightarrow$ 4 $\mu m \oplus$ 30-60 μs
  - L1-L2 : pixels of 25 $\mu m \times$ 25 $\mu m \Rrightarrow$ 3 $\mu m \oplus 20\ \mu s$ or 25 $\mu m \times$ 35 $\mu m \Rrightarrow$ 3.5 $\mu m \oplus 15\ \mu s$???
- **MIMOSA-33 :** Fine Pixels of 4 $\mu m \times$ 4 μm with delayed (analogue) read-out

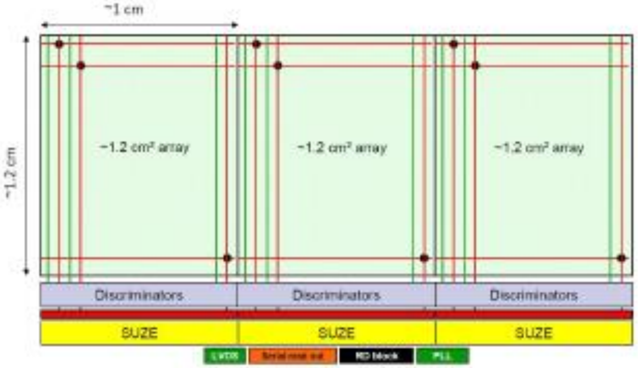


MISTRAL Proto. (2/3)

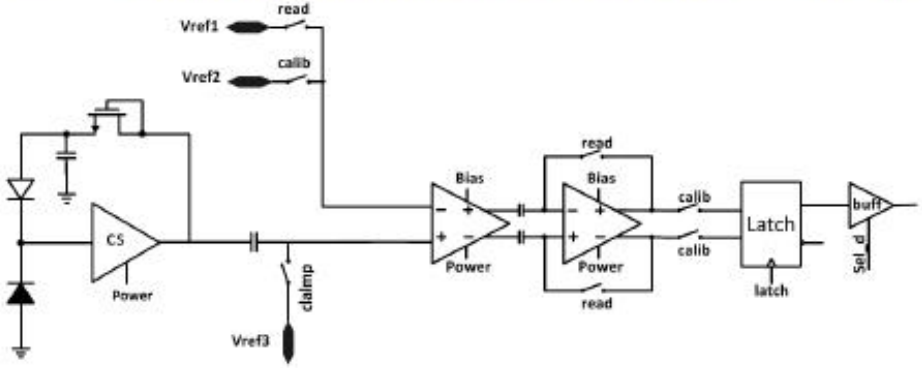
MISTRAL & ASTRAL : Schematics & Layouts

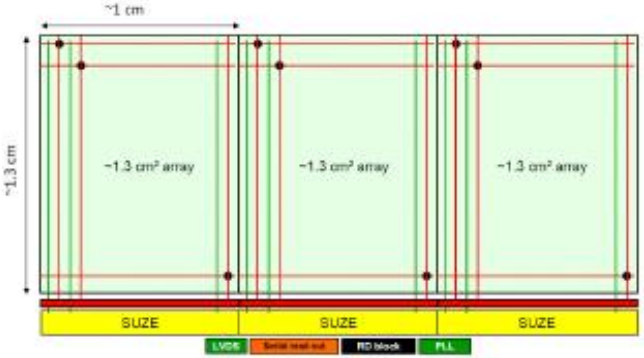
- **MISTRAL :** rolling shutter with 2-row read-out **& end-of column discriminators**





- **ASTRAL :** rolling shutter with 2-row read-out (≡ MISTRAL) **& in-pixel discriminators**

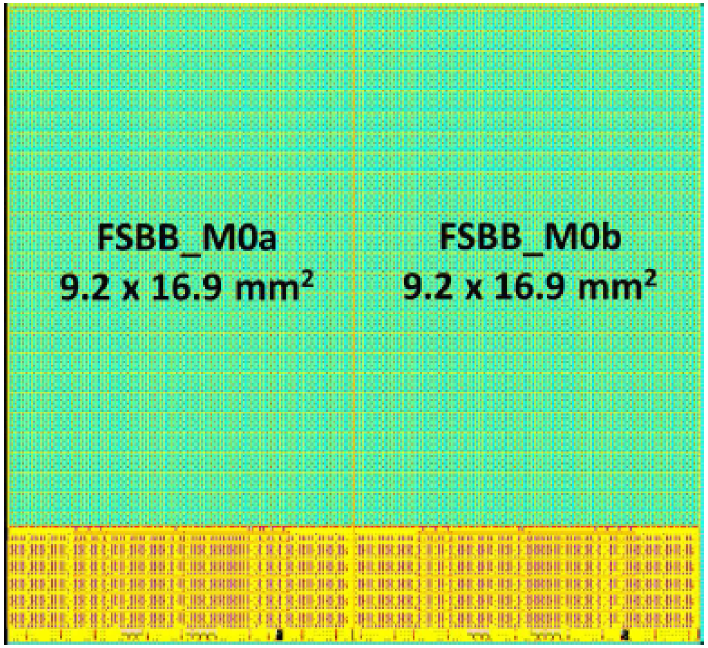




- **1st Full Scale Building Blocks (FSBB) fab. in Spring '14 ↦ FSBB-M0 tests ± completed**

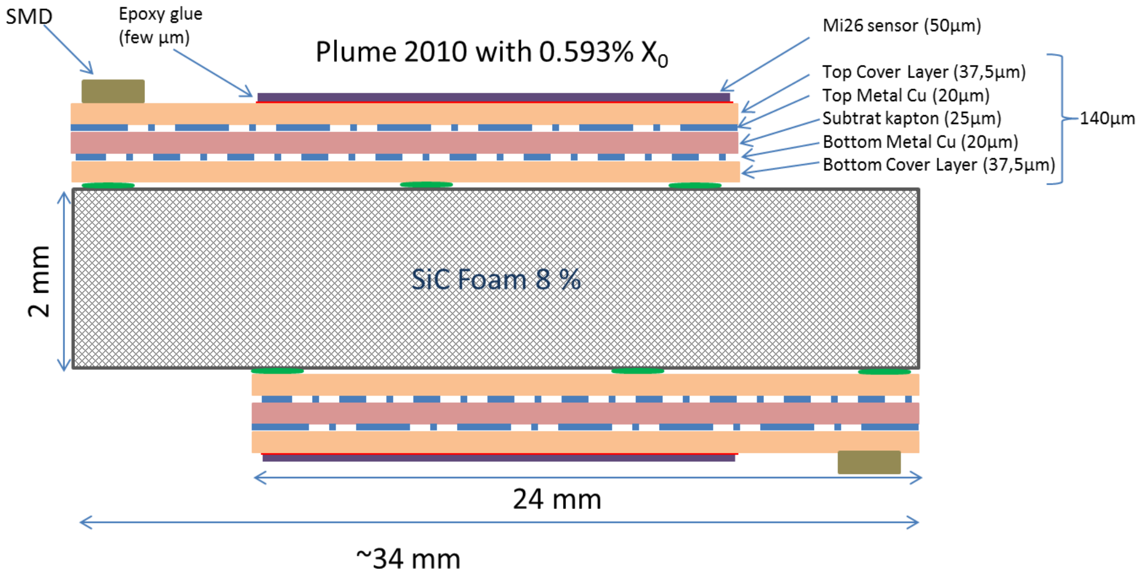
CPS for ITS Tracker : FSBB-M0a/b Overview

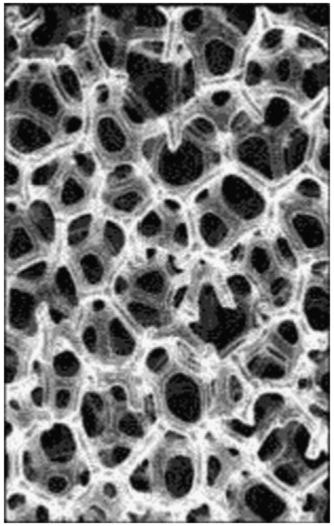
- **Main characteristics :**
  - pixels of $22\times33~\mu m^2$ including pre-amp. & CDS (clamping) using 6 ML
  - staggered sensing nodes
  - double-row rolling shutter read-out ($\equiv$ MIMOSA-22THRb)
  - 416 columns of 416 rows
  - $13.7\times9.2~\text{mm}^2$ active area
    - $\hookrightarrow$ becomes $13\times10~\text{mm}^2$ with $31\times24~\mu m^2$ pixels
  - 3 stages zero-suppression ($\equiv$ SUZE-02)
    - $\hookrightarrow$ windows of 4×5 pixels encoded on 32 bits
  - 4 output buffers of 512×32 bits each
  - 2 output nodes at 320 Mbits/s (160 MHz clock)
  - integrated JTAG, regulators, VDD, GND, ...
  - $t_{r.o.} \simeq$ 35–40 μs (tbc)
  - 2 slightly different sub-arrays in each sensor : optimisation of sensing node geometry & in-pixel circuitry

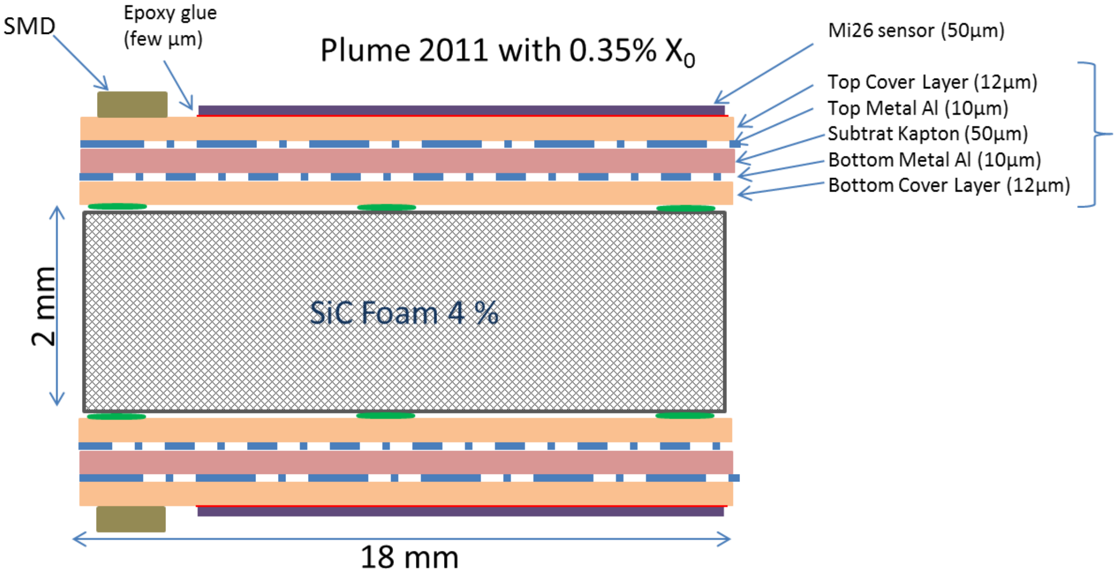


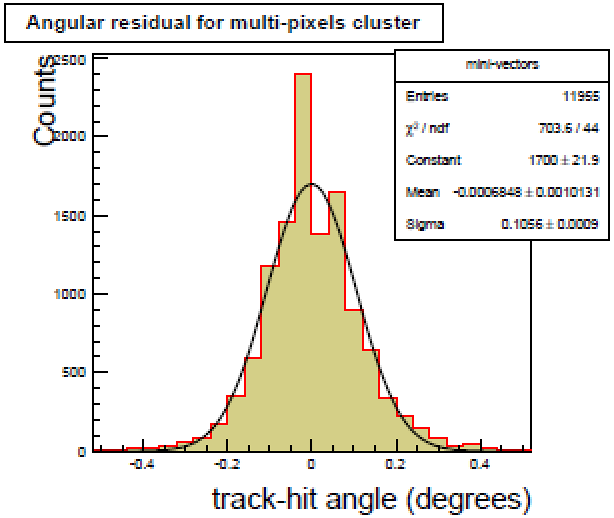
- **Design not final, e.g. in terms of :**
  - pixel dimensions
  - peripheral circuitry area
  - power consumption
  - pad implementation
  - SUZE-02 throughput vs power
  - trigger implementation (if any)

Sensor integration in Ultra Light Devices



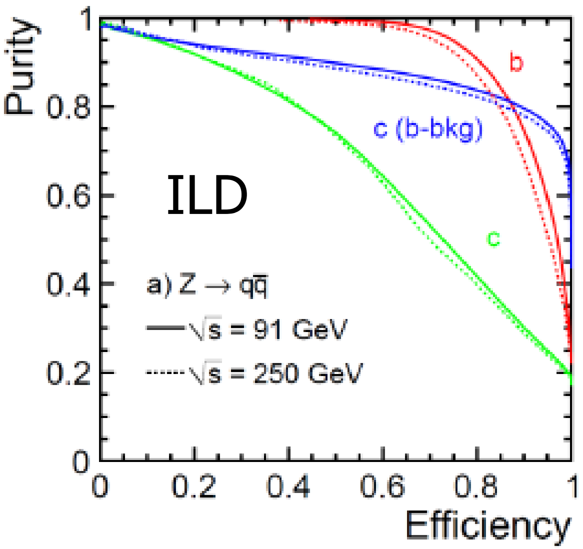


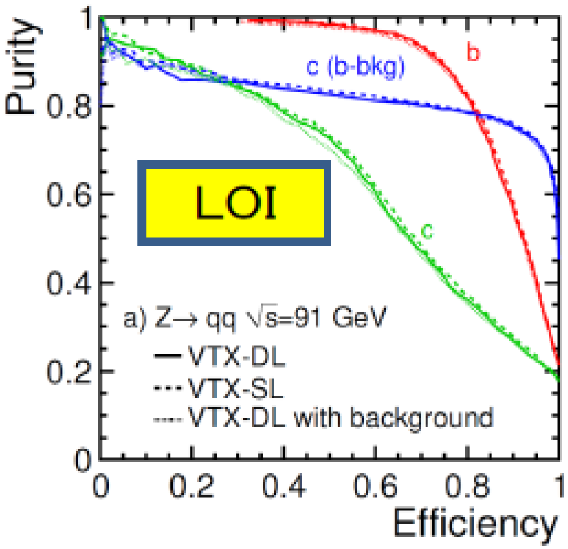


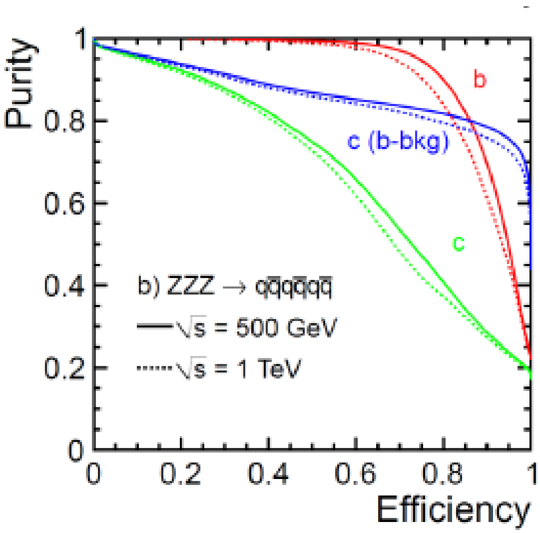


Expected Vertex performances : Flavor tagging

- ILD example
- Full simulation
- Multi-variable tagging algorithm (BDT)
  - LCFIplus
- Continuous improvements



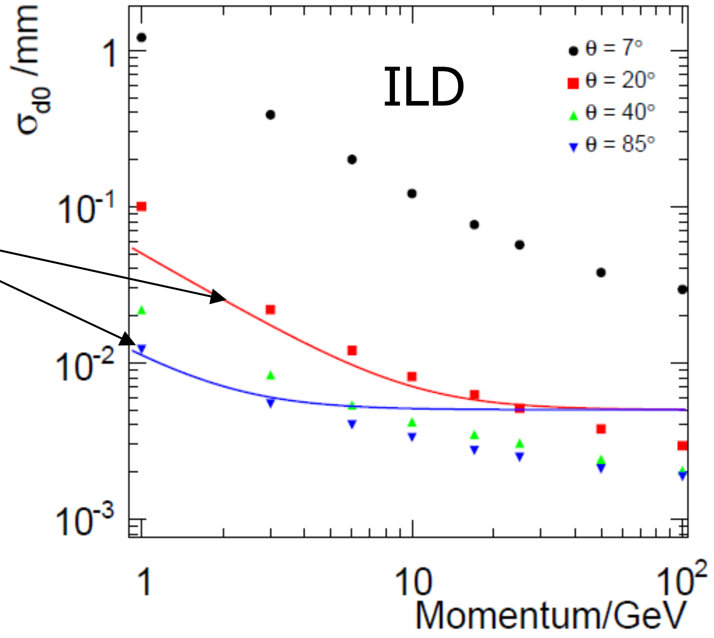


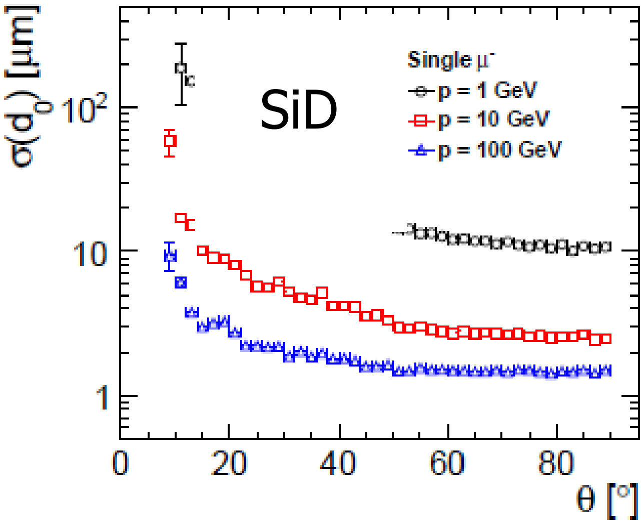


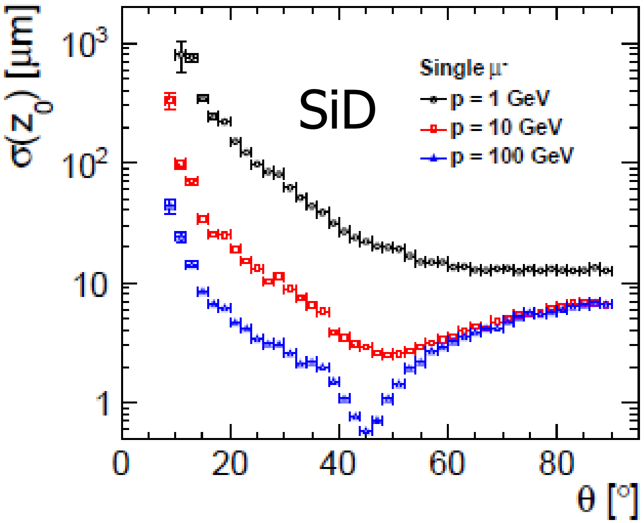
Expected Vertex performances : I.P. resolution

- Full simulation
  - single muons events

lines = $\sigma_{r\phi} = 5\ \mu\text{m} \oplus \frac{10}{p(\text{GeV})\sin^{3/2}\theta}\ \mu\text{m}$

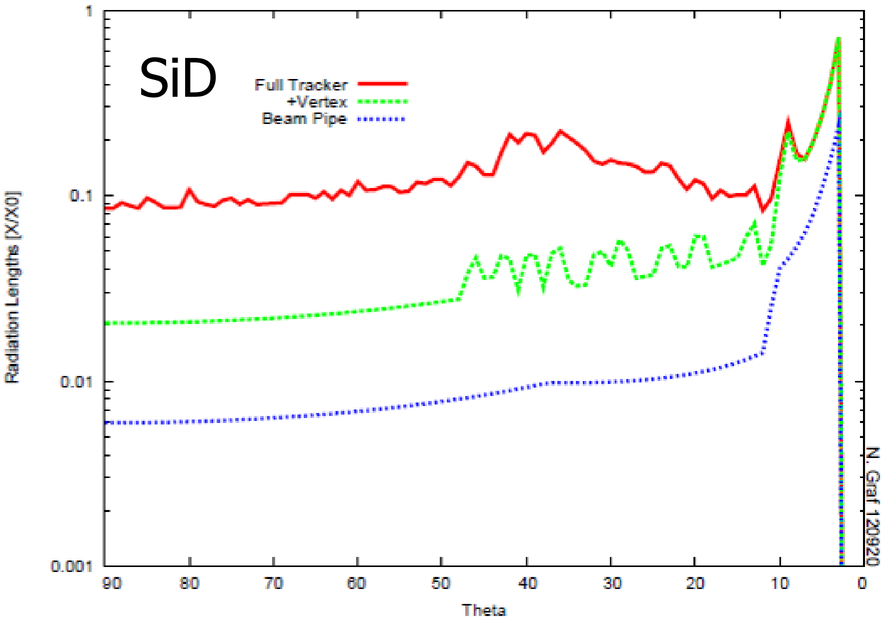


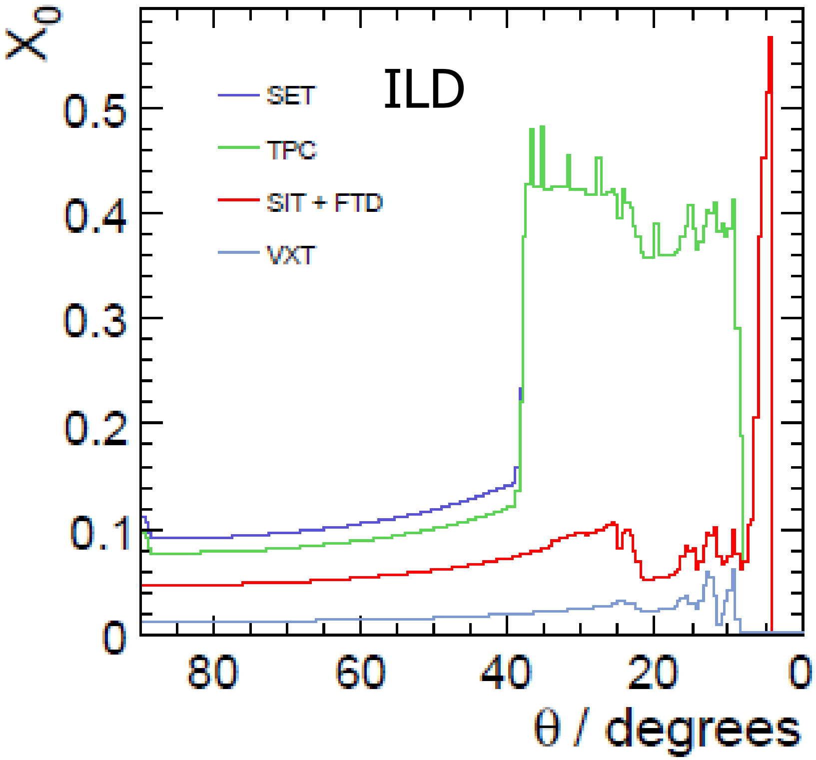




Tracking system: material budget

Radiation length vs polar angle

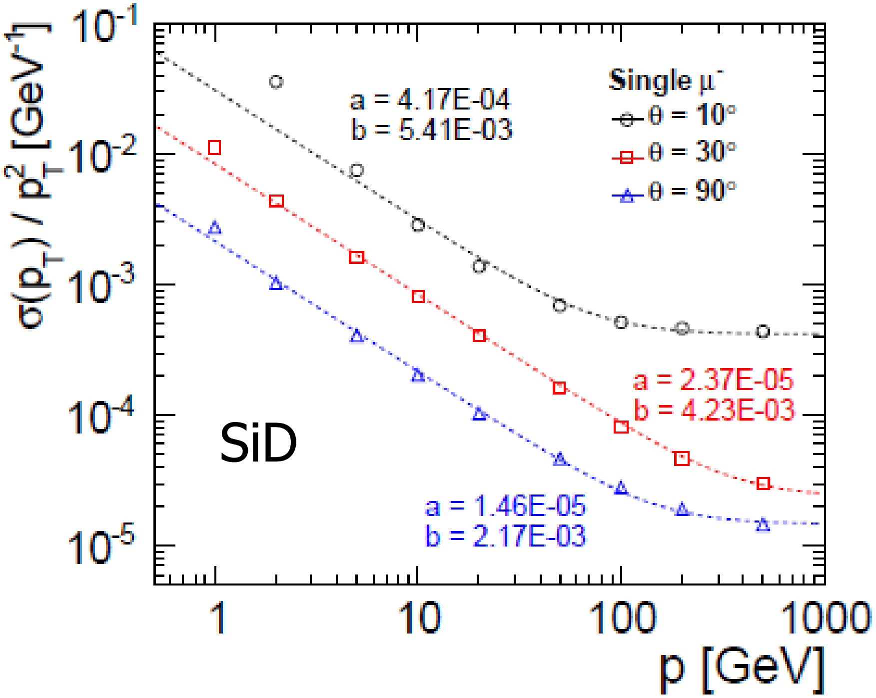




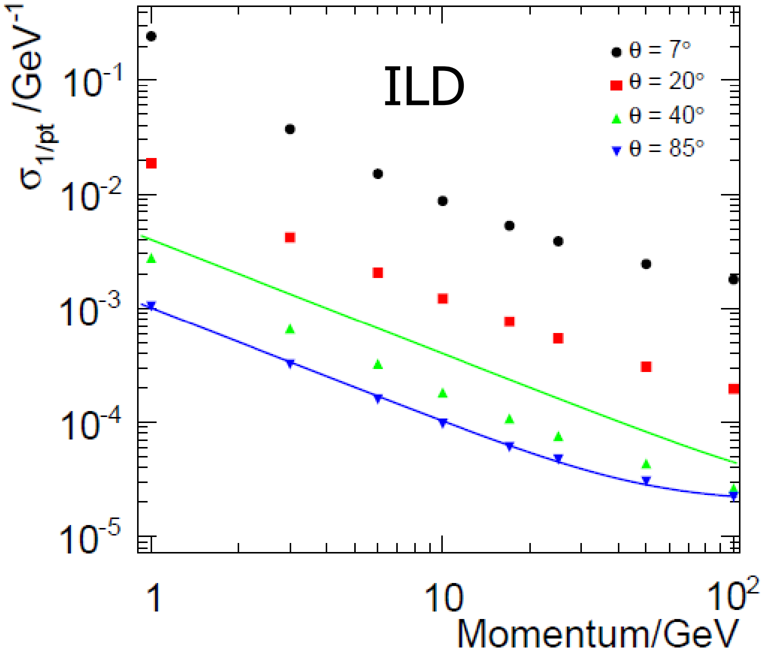
Goal: 0.1 X_0 for the complete tracker

Expected Tracking performances

Single muons events : Normalised pT resolution for different polar angles



$$\sigma_{1/p_T} = 2 \times 10^{-5} \oplus 1 \times 10^{-3}/(p_T \sin\theta)$$



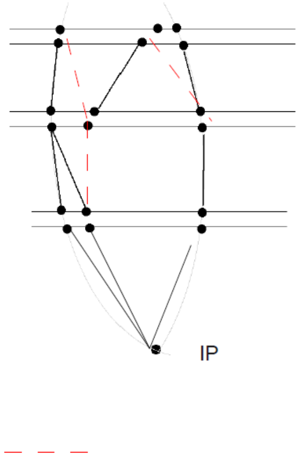
- SiD:
  - better @ high pT
  - robustness in high density tracks environment

- ILD:
  - better @ low pT
  - dE/dx capabilities (TPC)

see *Vertexing software and methods for the ILC* talk by G.Voutsinas

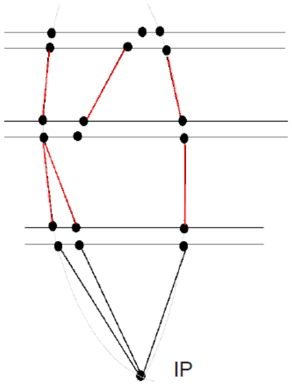
Tracking with mini vectors at ILD (Voutsinas)

Cellular Automaton – first pass



Connection filtered out by MV φ angle crit.

- First pass of cellular automaton
  - Every cell starts with state 0
  - Connect only cells having the same state
  - If a cell is connected with another, its state is raised by 1 (red segments)

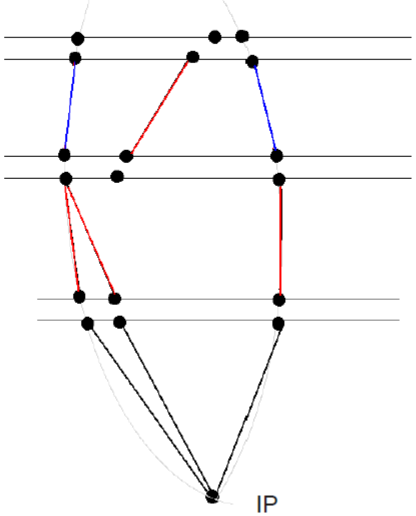


Cellular Automaton – second pass

- Second pass of cellular automaton
  - State 2
  - State 1
  - State 0
- CA continues up to the point no other changes occur in cell's states
- Consider segments where

state = layer number

as good



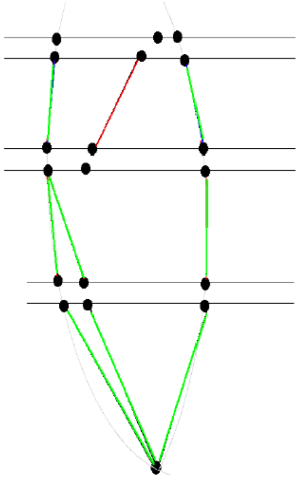
Cellular Automaton – collect tracks

- Second pass of cellular automaton
  - State 2
  - State 1
  - State 0
- CA continues up to the point no other changes occur in cell's states
- Consider segments where

state = layer number

as good

- Form track candidates



- Exploits the double sided ladder structure of VXD
- Up to now, has been applied in various CMOS VXD configurations (see table)
- Mini – vector formation

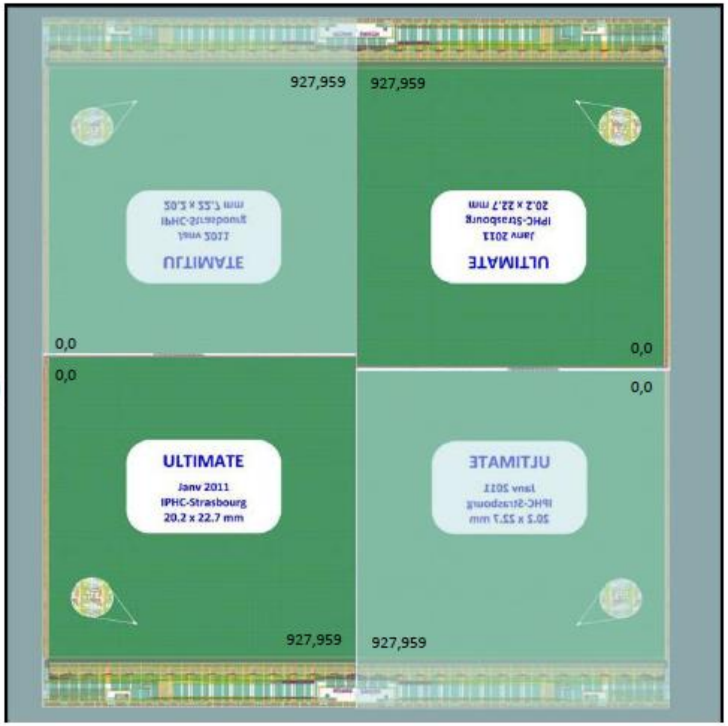
  1) Hits in adjacent layers (dist 2mm) with max distance 5mm

  2) Or δθ between hits in adjacent layers (cut can go up to 0.1^0)
- Divide VXD into θ, φ sectors
  - Try to connect mini – vectors in neighbouring sectors using a cellular automaton algorithm
- Cellular automaton is already there for the FTD tracking
- Very flexible
  - Appealing to be used for pattern recognition in other detectors
  - See R. Glattauer Diploma thesis

LAT final plane

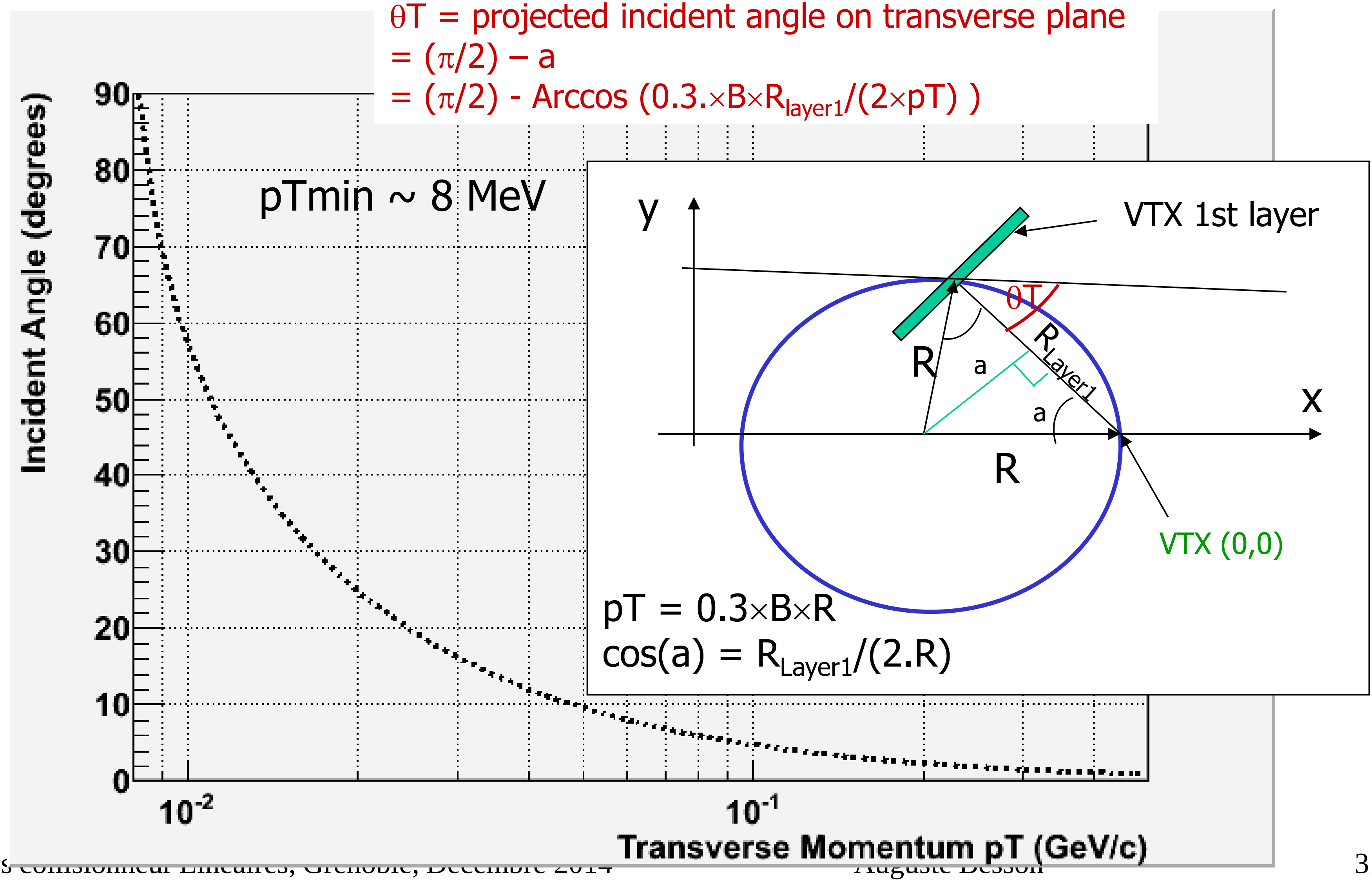
- **LAT motivations**
  - Big surface and thin reference planes
- **Assembly**
  - Stretched 50μm Mylar foil ($X_0^{Mylar} \sim 3 \times X_0^{Si}$)
  - Layout: 2 staggered sensors on each side
  - UV cured gluing
  - Sensor bonding
- **Basic numbers**
  - 3.6 M-pixels over 15.3 cm^2
  - $\lesssim$ 200μs integration time
  - Insensitive areas ~100μm
- **Production**
  - 2 SALAT planes fully operational (Mod-3 and 4)
  - One crack on sensor of Mod-3 during gluing
  - Even if sensor still operational decided to switch it off

Read out orientation



Beam background

- θT angle (no boost taken into account) vs pT

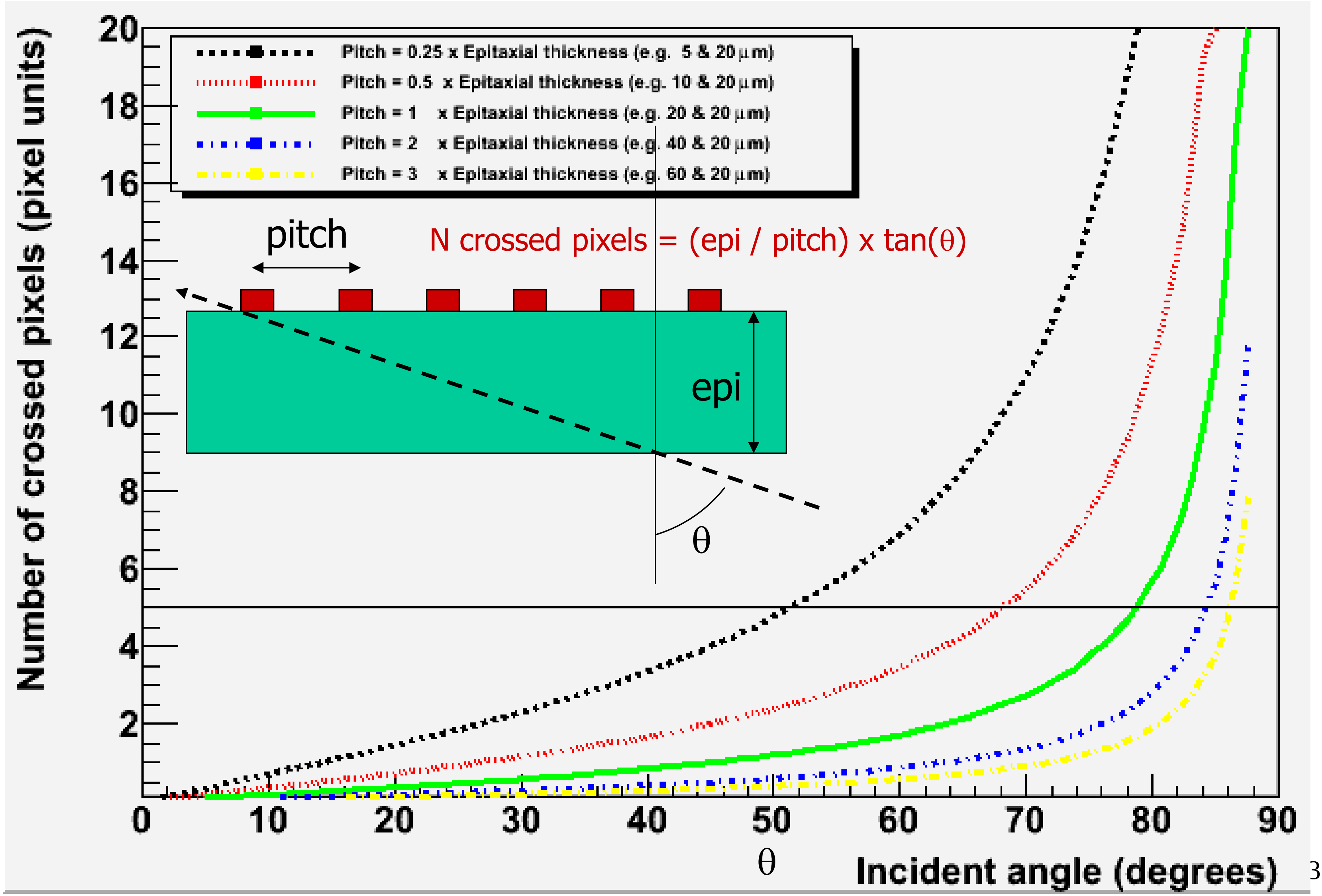


θT = projected incident angle on transverse plane
$= (\pi/2) - a$
$= (\pi/2) - \text{Arccos}\,(0.3\times B\times R_{\text{layer1}}/(2\times pT))$

pTmin ~ 8 MeV

$pT = 0.3\times B\times R$
$\cos(a) = R_{\text{Layer1}}/(2.R)$

Crucial parameter: pitch / epitaxial layer thickness



Beam background distribution (R. De Masi et al.)

- 1st layer.