ExCELSiOR
NANOSCIENCES CHARACTERIZATION CENTER

Pilotage et Acquisition d'un laser femto-seconde

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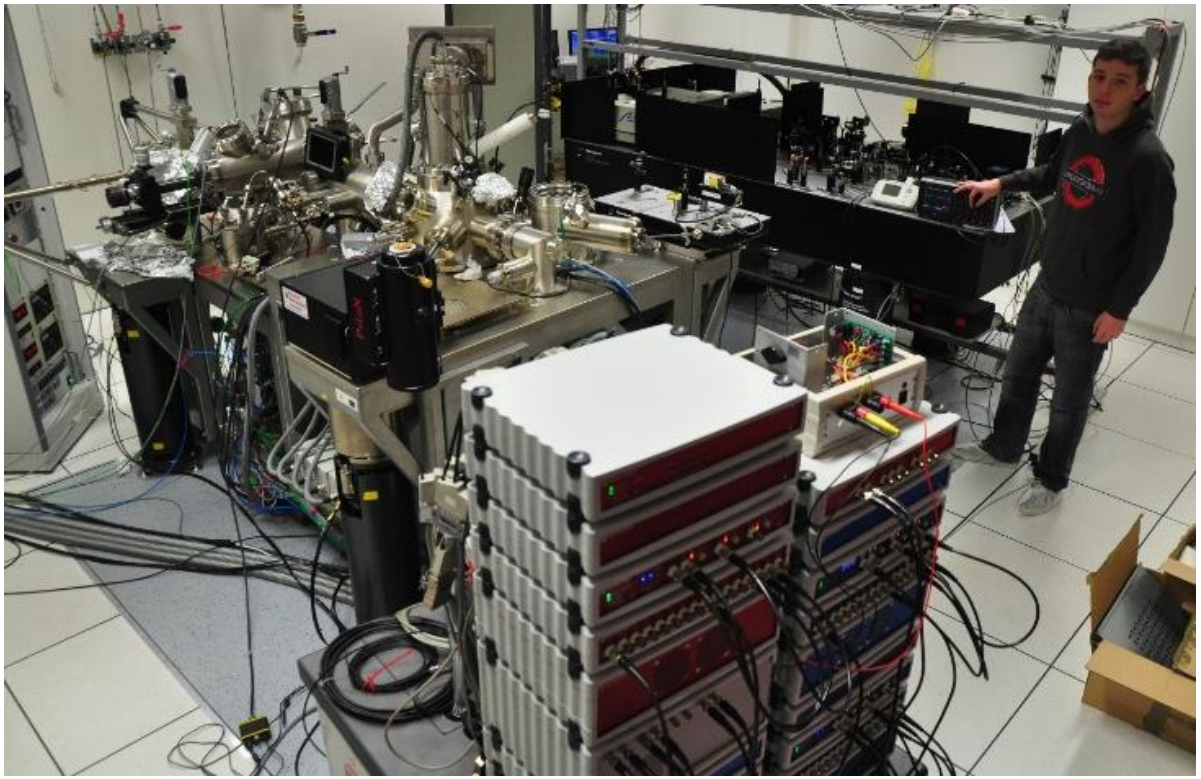
Laser combined-UHV-SEM-STM

UHV system

SEM

4 probes-STM



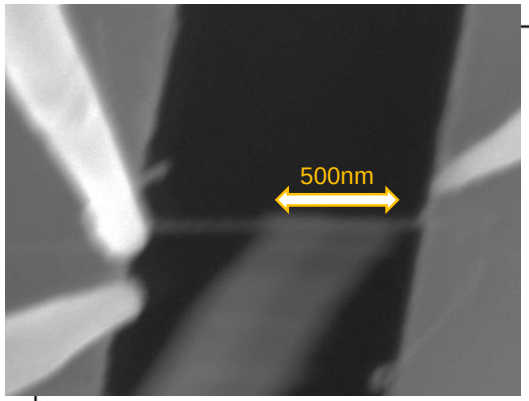
Femto-second laser

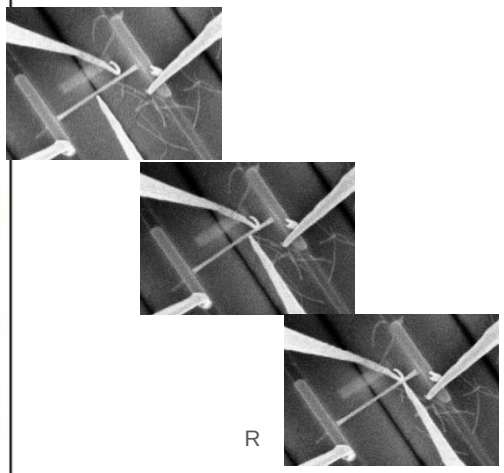
Electrical mapping and testing at the nanoscale

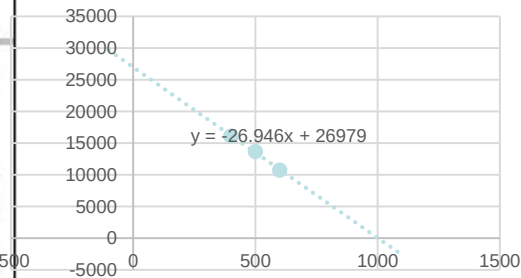
Time resolution

Mesures électriques à l'échelle nanométrique

$V_t (X,Y) = V_{pot} (X,Y, <It>=0)$





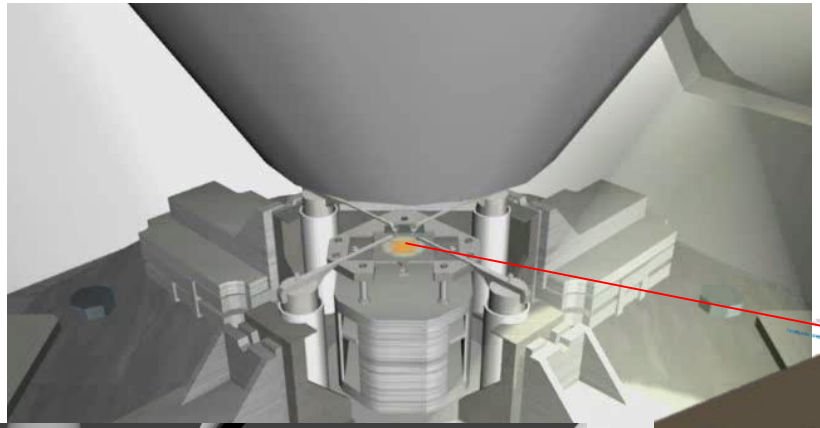


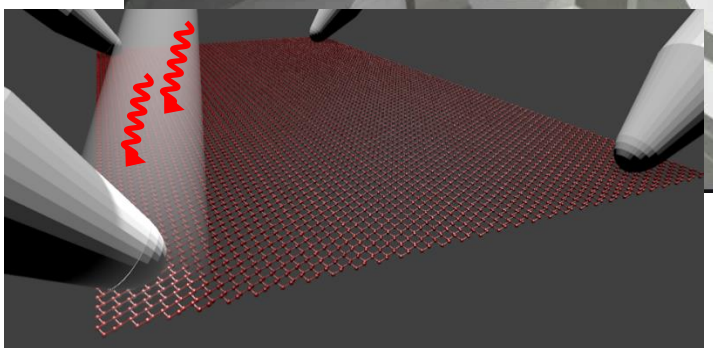
ANR Nanosprings

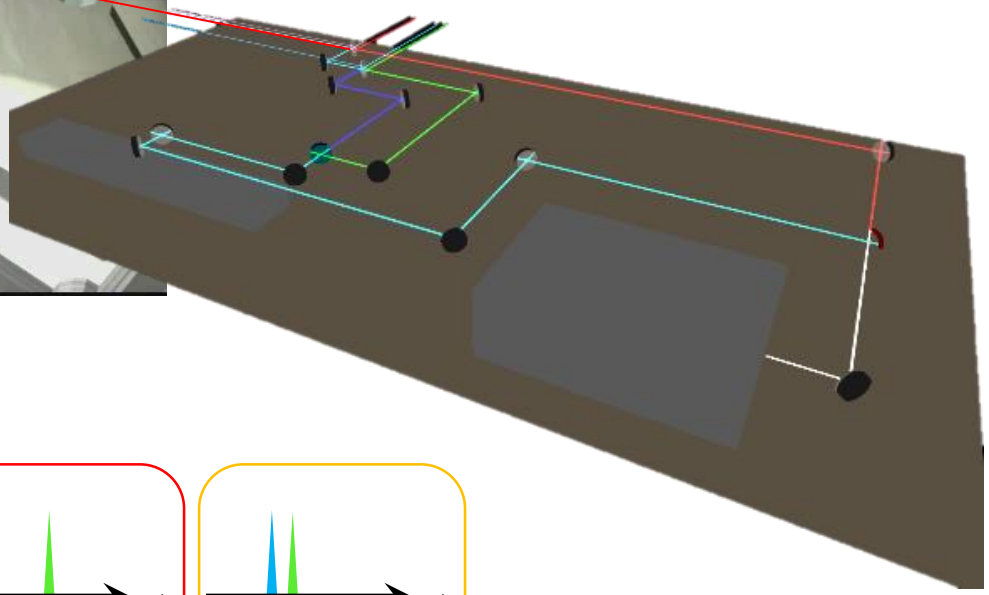
S. Habtoun, Ch. Bergaud (LAAS)
R. Oda (IECB)
MH. Delville (ICMCB)
M. Berthe (IEMN)

h (Ohm)	662	740	977	1210	1600	1210	1200	1130	868	950	605	797	455
L (nm)	49.5	28.3	50.5	33.3	53.5	25.3	55.6	23.2	43.4	22.2	34.3	29.3	24.2
Pente (Ohm/nm)	13.3737374		19.3465347		29.9065421		21.5827338		20		17.638484		18.8016529
LSpire (nm)		45.2318978		49.1339864		47.0000783		54.349481		50.4802479		43.7429751	

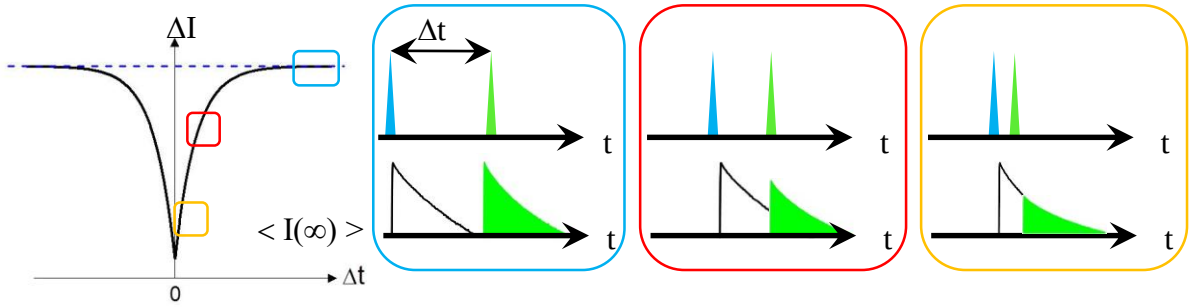
Résolution temporelle : couplage avec un laser femto-seconde







Largeur d'impulsion : 100fs
Taux de répétition : 80MHz
Pulse pickers : sélection de pulse unique



Modulation d'amplitude impossible

Modulation du délai

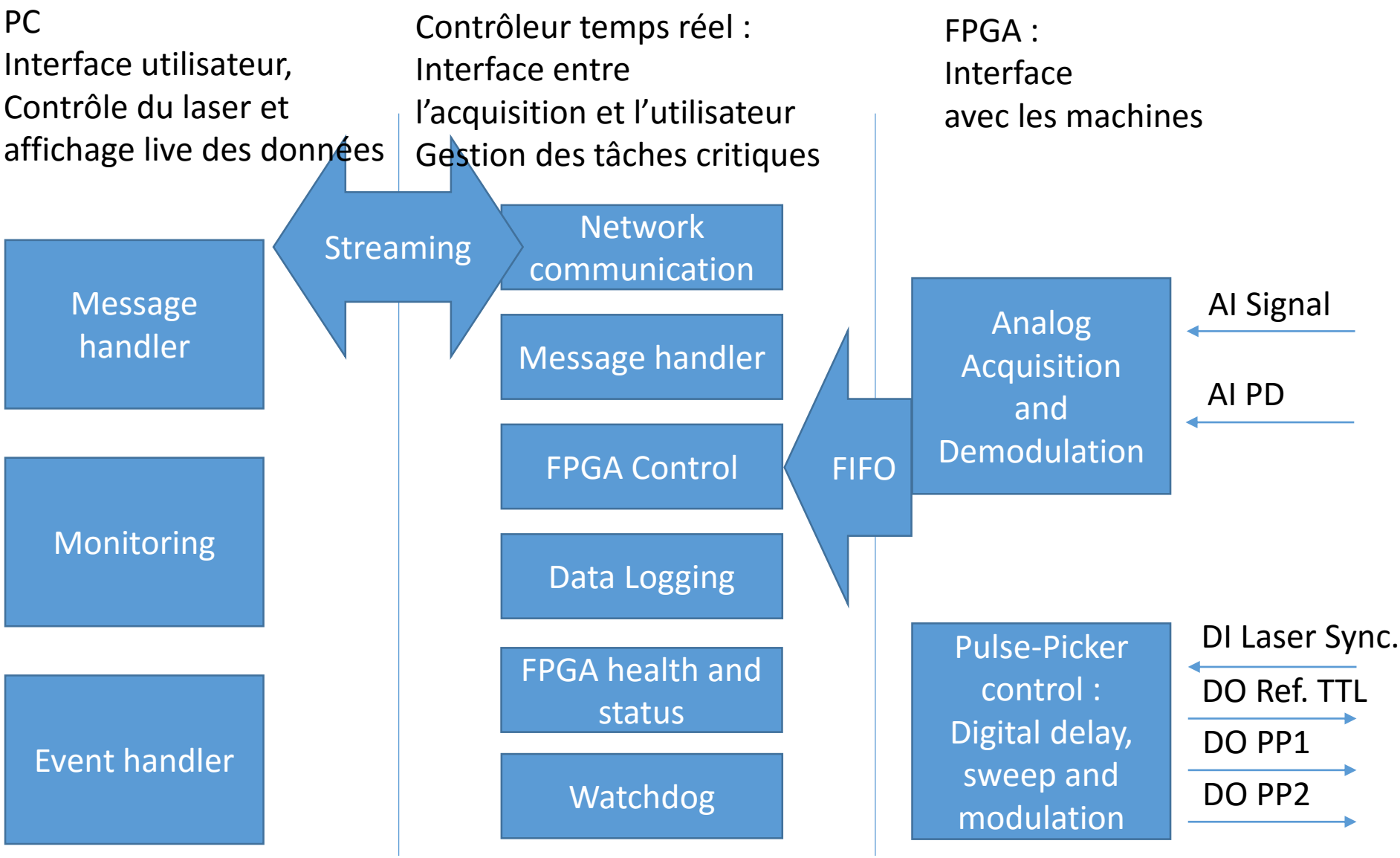
Intérêt

Utilisation d’un FPGA pour :

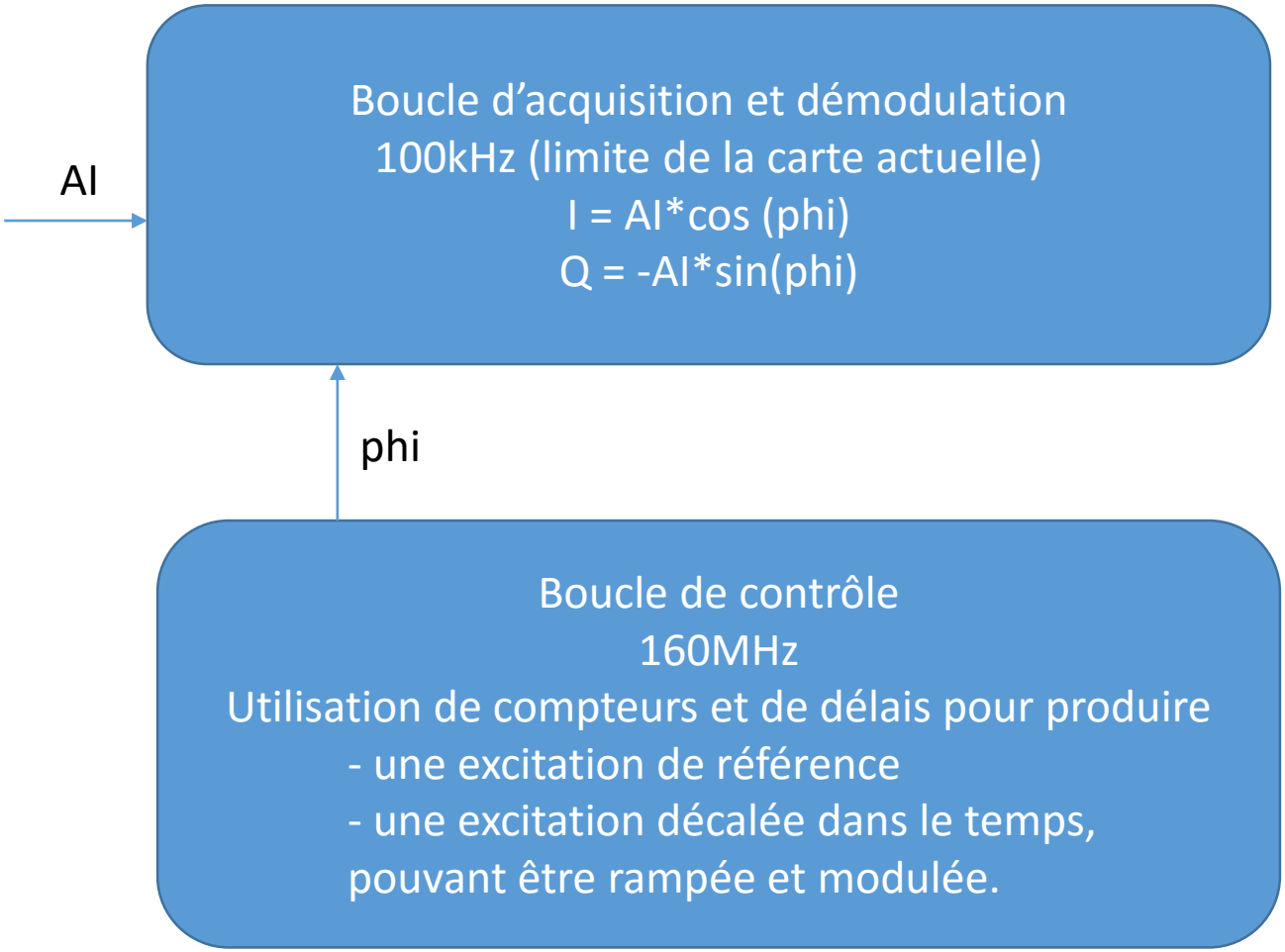
- Créer une excitation synchronisée
- Piloter l’excitation (délais, rampes, modulation)
- Démoduler le signal

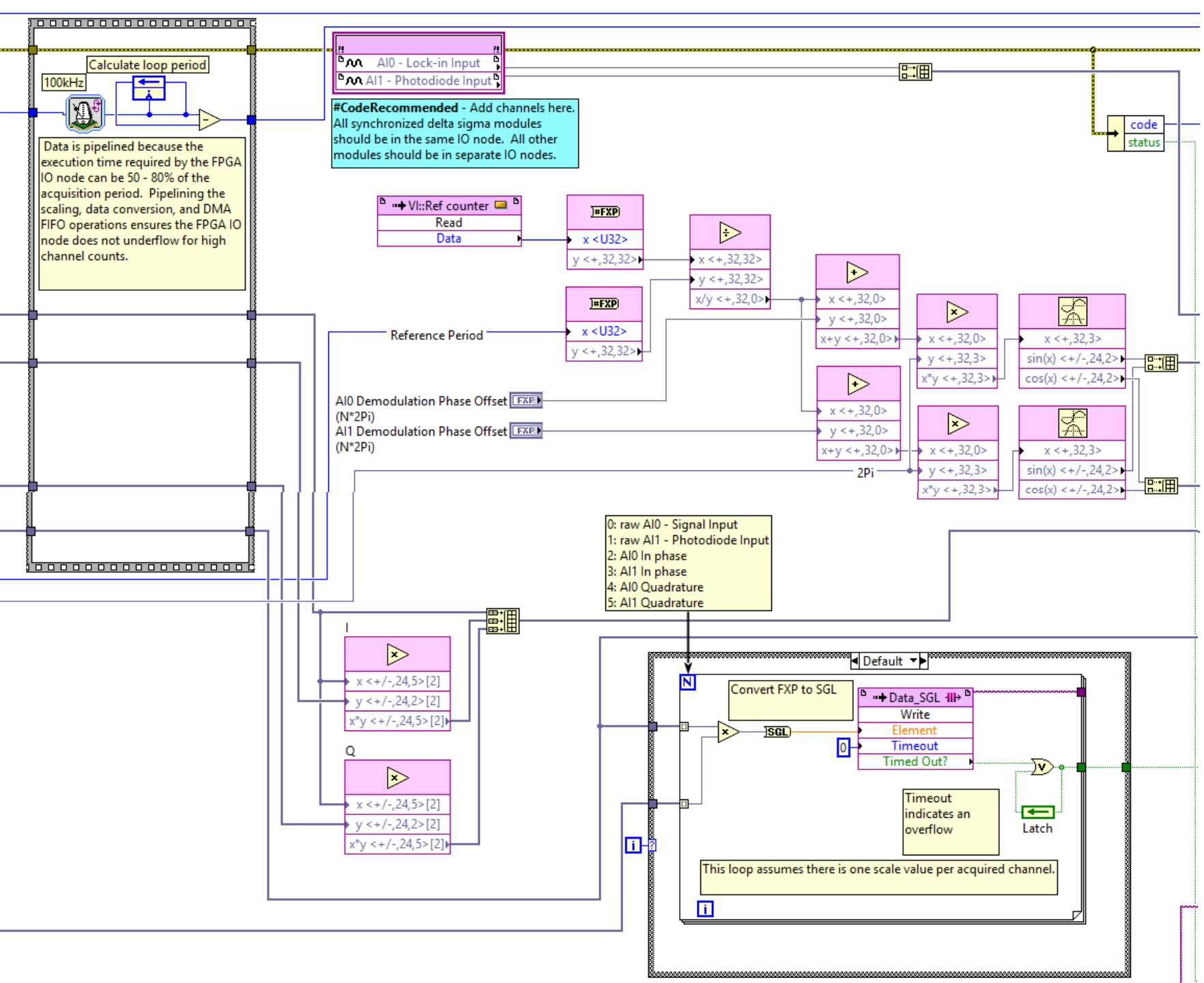
Base du programme : FPGA Waveform Acquisition

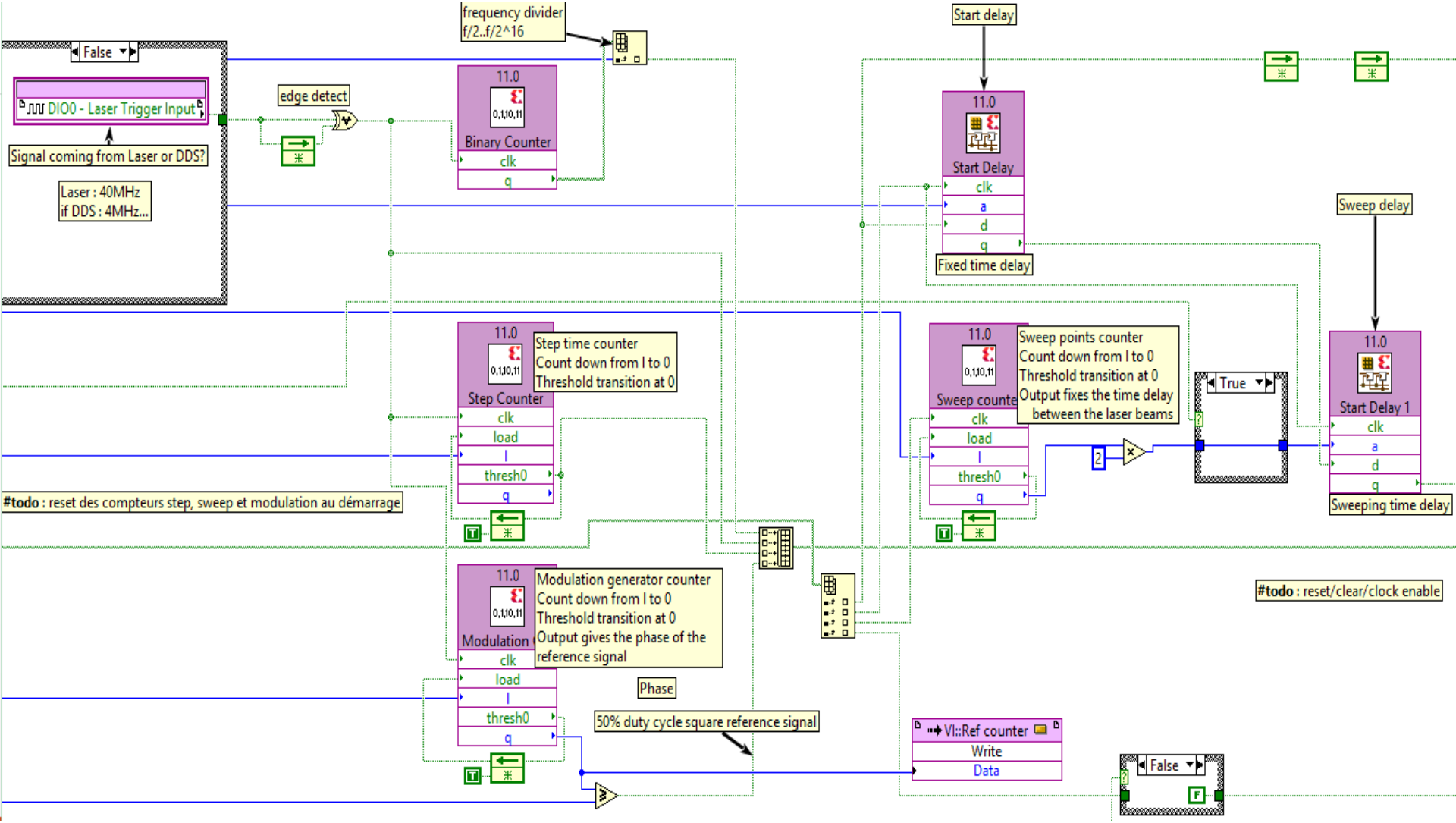
Schéma du programme



Détails du programme FPGA




Calculate loop period
100kHz
Data is pipelined because the execution time required by the FPGA IO node can be 50 - 80% of the acquisition period. Pipelining the scaling, data conversion, and DMA FIFO operations ensures the FPGA IO node does not underflow for high channel counts.
AI0 - Lock-in Input
AI1 - Photodiode Input
#CodeRecommended - Add channels here. All synchronized delta sigma modules should be in the same IO node. All other modules should be in separate IO nodes.
code
status
VI::Ref counter
Read
Data
#FXP
x <U32>
y <+,32,32>
x <+,32,32>
y <+,32,32>
x/y <+,32,0>
Reference Period
x+y <+,32,0>
x*y <+,32,3>
x <+,32,3>
sin(x) <+/-,24,2>
cos(x) <+/-,24,2>
AI0 Demodulation Phase Offset (N*2Pi)
AI1 Demodulation Phase Offset (N*2Pi)
2Pi
0: raw AI0 - Signal Input
1: raw AI1 - Photodiode Input
2: AI0 In phase
3: AI1 In phase
4: AI0 Quadrature
5: AI1 Quadrature
I
Q
x <+/-,24,5> [2]
y <+/-,24,2> [2]
x*y <+/-,24,5> [2]
Default
N
Convert FXP to SGL
SGL
Data_SGL
Write
Element
Timeout
Timed Out?
0
Timeout indicates an overflow
Latch
This loop assumes there is one scale value per acquired channel.
i


frequency divider
f/2..f/2^16
Start delay
False
DIO0 - Laser Trigger Input
Signal coming from Laser or DDS?
Laser : 40MHz
if DDS : 4MHz...
edge detect
11.0
Binary Counter
clk
q
Start Delay
clk
a
d
q
Fixed time delay
Sweep delay
Step Counter
Step time counter
Count down from I to 0
Threshold transition at 0
load
I
thresh0
#todo : reset des compteurs step, sweep et modulation au démarrage
Sweep counte
Sweep points counter
Count down from I to 0
Threshold transition at 0
Output fixes the time delay
between the laser beams
True
2
Start Delay 1
Sweeping time delay
Modulation
Modulation generator counter
Count down from I to 0
Threshold transition at 0
Output gives the phase of the
reference signal
Phase
50% duty cycle square reference signal
#todo : reset/clear/clock enable
VI::Ref counter
Write
Data
False

Difficulté :

- Utilisation des IP : les datasheets ne sont pas toujours bien détaillés en termes de signaux

Risque :

- Fréquence et jitter du FPGA

Perspective :

- Intégration de l'interface dans le contrôleur avec un serveur web -> plus besoin de PC dédié, meilleure intégration avec d'autres logiciels.