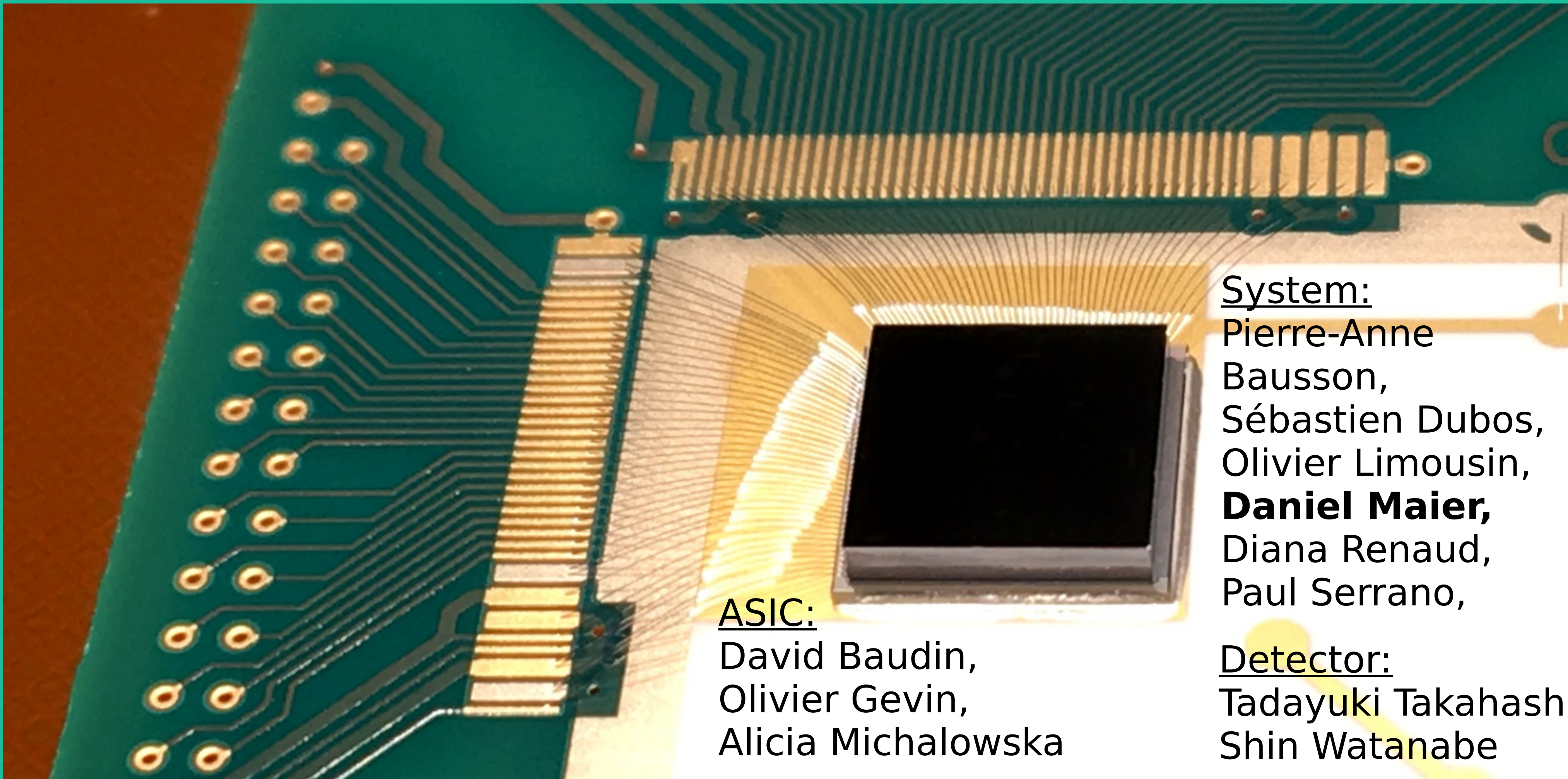


System:
Pierre-Anne Bausson,
Sébastien Dubos,
Olivier Limousin,
Daniel Maier,
Diana Renaud,
Paul Serrano,

ASIC:
David Baudin,
Olivier Gevin,
Alicia Michalowska

Detector:
Tadayuki Takahashi,
Shin Watanabe

D2R1

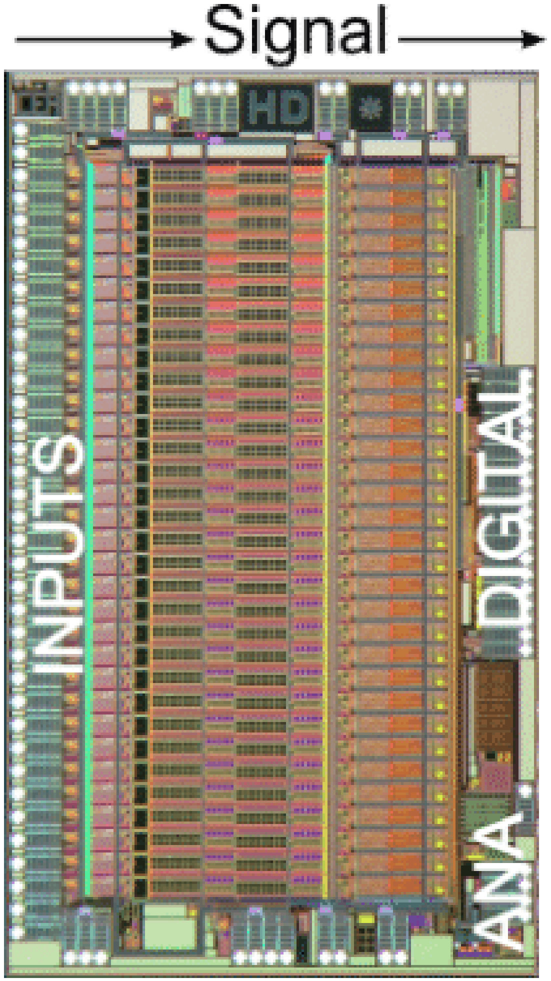
the newest member in the CALISTE family

OVERVIEW

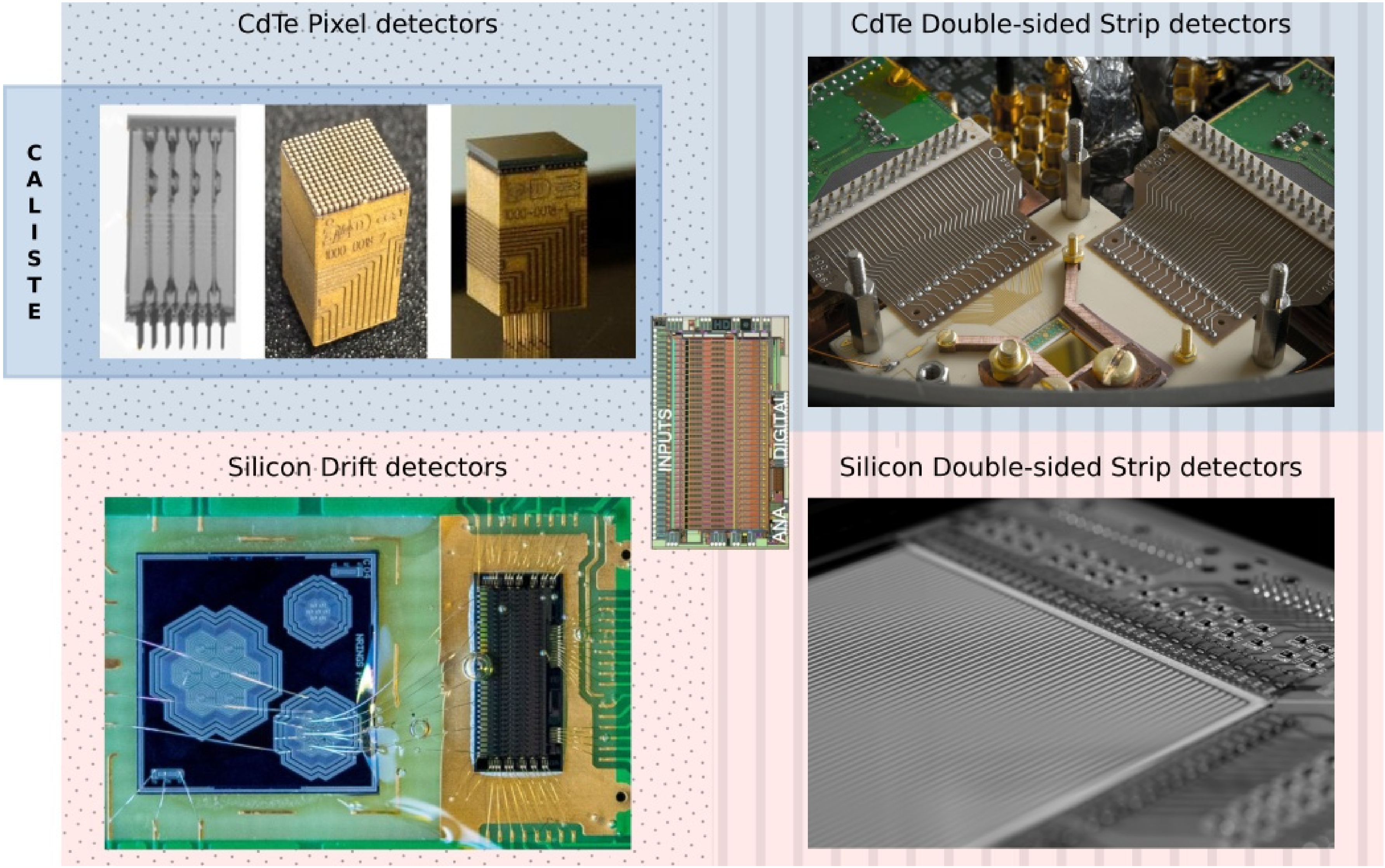
- **review: CALISTE**
- **D2R1:**
  - design and architecture
  - first verification tests
  - next steps
- **outlook: MC2**

REVIEW: CALISTE: IDeF-X

- **the Caliste detector modules are based on IDeF-X readout ASICs**
  - started in 2003; now in 7th generation
  - properties:
    - optimized for low C_{in} & low I_{dark}
    - ultra-low noise,
    - low power consumption
    - channel individual triggered readout
    - designed for space applications

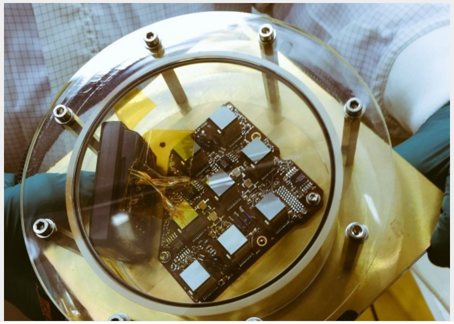


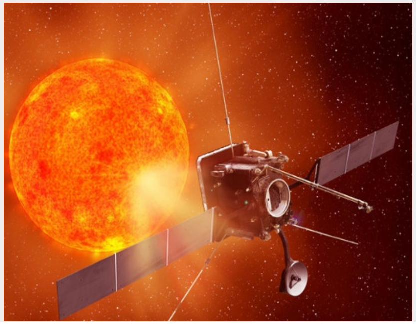
REVIEW: applications of IDeF-X



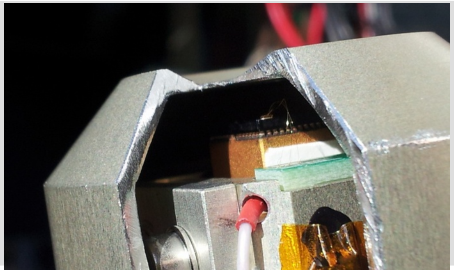
REVIEW: applications of CALISTE

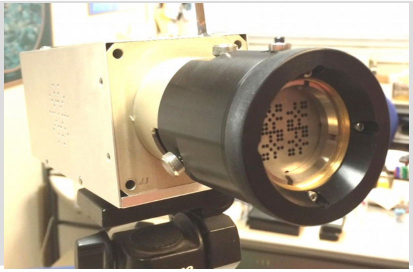
- STIX on Solar Orbiter (CALITE-SO)
  - solar mission, 2020 (ESA Cosmic Vision)



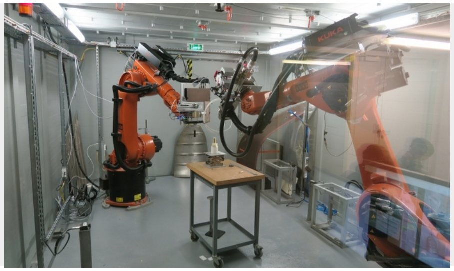


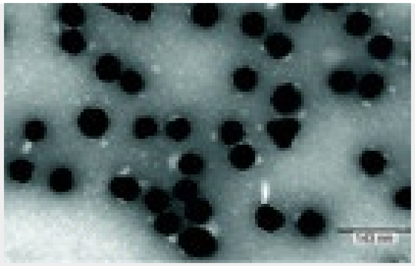
- ORIGAMIX (CALISTE-HD & -O)
  - portable gamma camera for nuclear safety



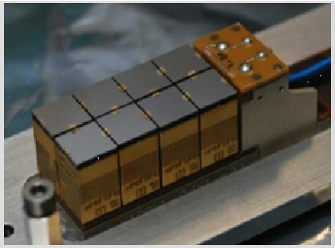


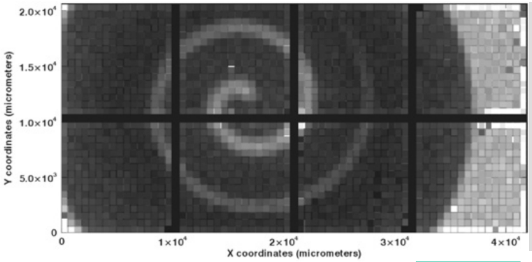
- SATBOT (CALISTE-HD)
  - assisted radiotherapy using Au-NP





- MACSI (8 x CALISTE-HD)
  - proof of concept for large focal planes
  - 4-side buttability





REVIEW: ASIC parameters of interest

	# ch	size	technology	dynamic range	energy range	floor noise	power
	-	um^2	-	fC	keV (CdTe)	e^- (rms)	mW/ch
IDeF-X V1.1	16	3000 x 4000	350 nm 3.3 V	10	250	37	2.8
IDeF-X V2	32	2800 x 6400	350 nm 3.3 V	8	200	33	3.0
IDeF-X HD	32	3500 x 5900	350 nm 3.3 V	10-40	250-1000	31	0.8
D2R1	?	?	?	?	?	?	?

REVIEW: ASIC parameters of interest

- **What do we want to achieve?**
- **Which parameters need modification?**
- **How to do it?**

→ a look on the detector characteristics might help...

REVIEW: detector parameters of interest

	ASIC	# pix	pixel pitch	detector area	thickness	spectr. res	power
			um	mm^2	mm	eV (FWHM @ 60 keV)	mW/mm^2
Caliste-64	4 x IDeF-X V1.1	8 x 8	900	10 x 10	1	900	3.0
Caliste-256	8 x IDeF-X V2	16 x 16	580	10 x 10	1	860	8.3
Caliste-HD	8 x IDeF-X HD	16 x 16	625	10 x 10	1	670	2
Caliste-O	8 x IDeF-X HD	16 x 16	800	14 x 14	2	927	1

D2R1: design changes

- **What do we want to achieve?**
  - Spectro-imaging detector placed in the focus of a high resolution X-ray optics (10-20’’ for a focal length of 10-20m)
- **Which parameters need modification?**
  - pixel pitch → much lower (defined by the mirror resolution and by the constraints for the spectral resolution)
  - power consumption per channel → much lower as there are many channels per area
- **Important parameters to keep:**
  - spectral res. → nearly Fano limited (like for Calsite-HD)
  - dynamic range → 2-250 keV (limited by mirror efficiency)
- **How to do it?**
  - New concept: hybrid detector

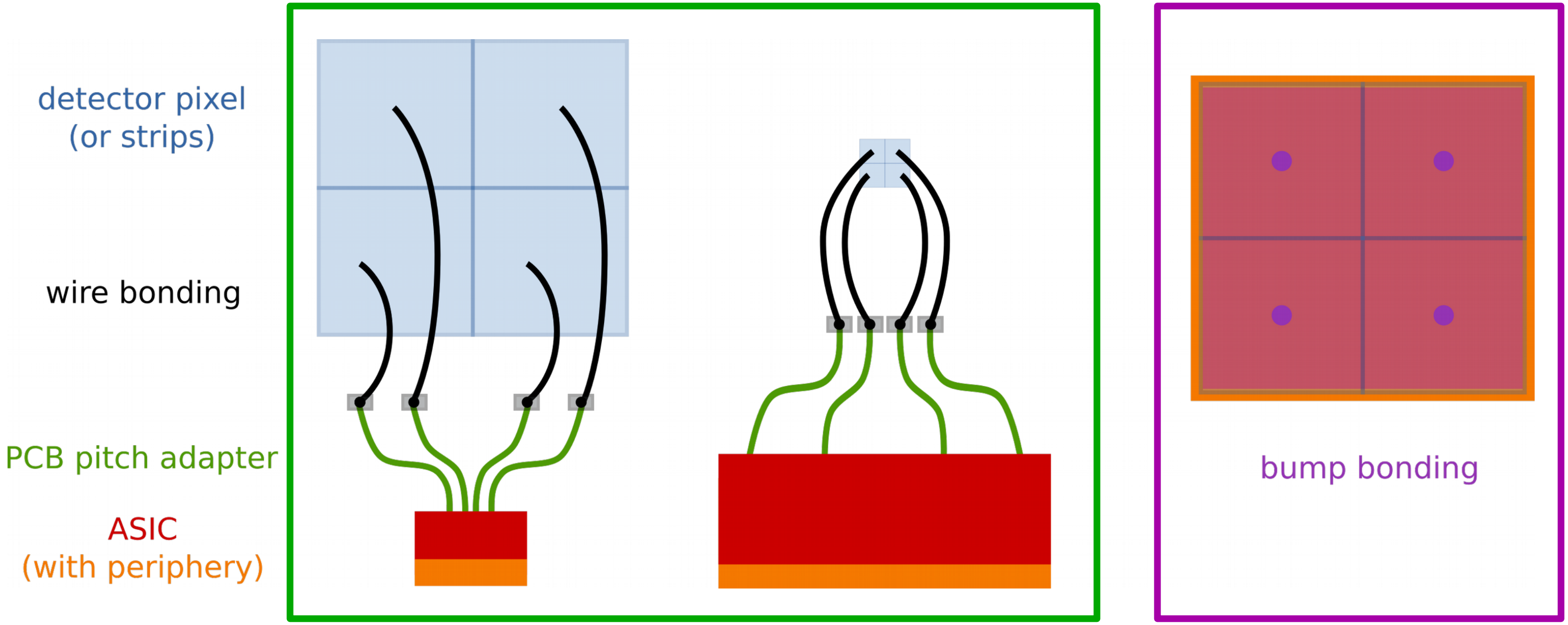
REVIEW: ASIC parameters of interest

	# ch	size	technology	dynamic range	energy range	floor noise	power
	-	um^2	-	fC	keV (CdTe)	e^- (rms)	mW/ch
IDeF-X V1.1	16	3000 x 4000	350 nm 3.3 V	10	250	37	2.8
IDeF-X V2	32	2800 x 6400	350 nm 3.3 V	8	200	33	3.0
IDeF-X HD	32	3500 x 5900	350 nm 3.3 V	10-40	250-1000	31	0.8
D2R1	256	**16 x 16 (300 x 300)** + 300 um GR	**180 nm 1.8 V**	10	250	<=31	**0.18**

D2R1: a hybrid detector

– how to connect detector and ASIC?

- **wire bonding**: + (almost) independent of detector or ASIC layout
  - additional stray capacitance
- **bump bonding**: + minimal stray capacitance
  - ASIC size has to be adapted to detector size

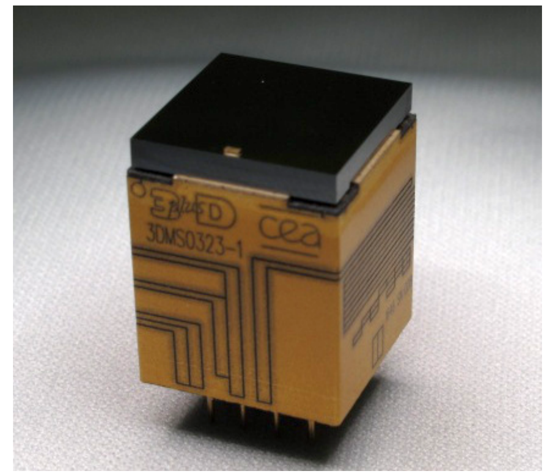


D2R1: a hybrid detector

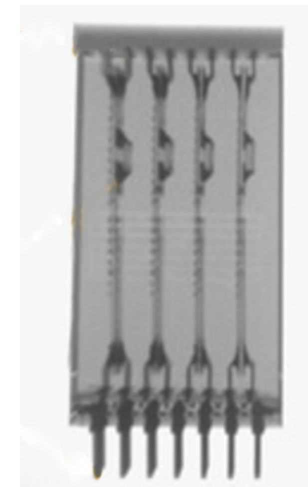
Wire bonding connection
(System in Package)

hybrid detector

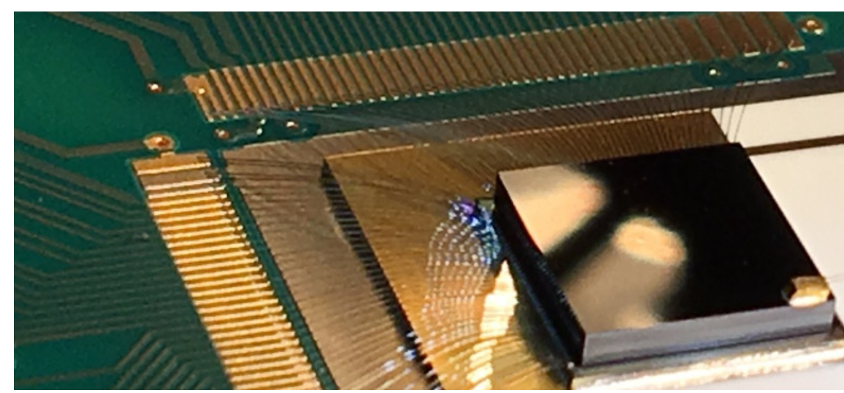
- 4-side buttability
- stray capacitance



Caliste-O



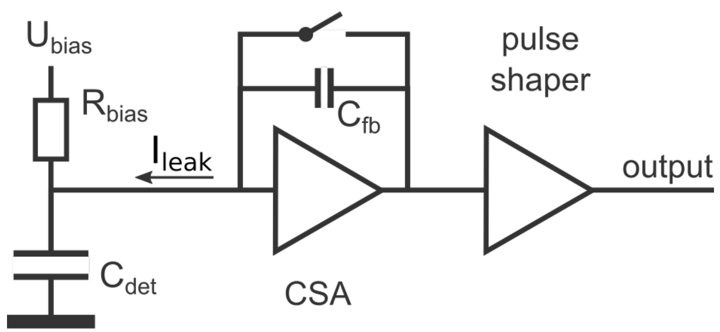
Caliste-256

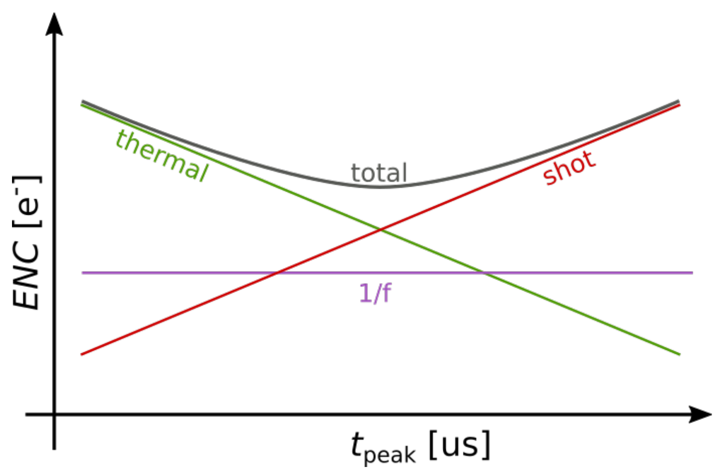


D2R1

D2R1: noise analysis in a nutshell

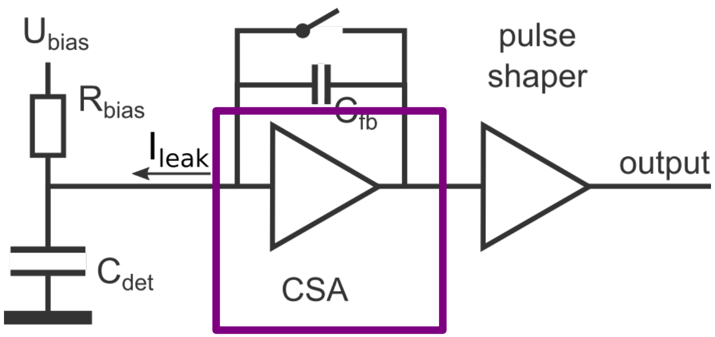
- electronic noise mainly defined by the CSA
- $ENC^2 = ENC_{TH}^2 + ENC_F^2 + ENC_{SH}^2$
  - thermal noise $ENC_{TH}^2 = (C_{fb} + C_{in})^2 * a_{TH} / t_{peak}$
  - 1/f noise $ENC_F^2 = (C_{fb} + C_{in})^2 * a_F$
  - shot noise $ENC_{SH}^2 = I_{leak} * t_{peak} * a_{SH}$
- detector parameters:
  - input capacitance C_{in}
  - leakage current I_{leak}
- ASIC parameters: a_{TH}, a_F, a_{SH}, C_{fb}
  - the a-parameters depend on the shaper and on the CSA input transistor → “Caterpillar” optimization
  - C_{fb} defines the dynamic range
- operational parameters: shaping time t_{peak}

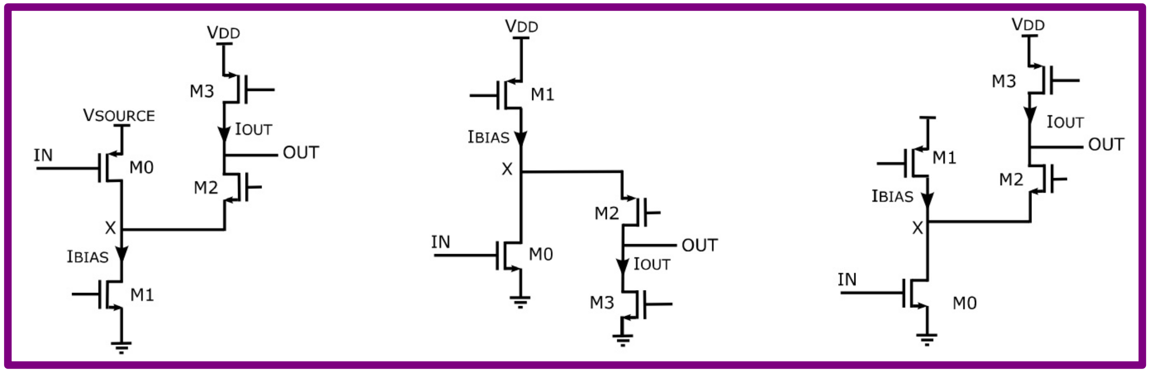


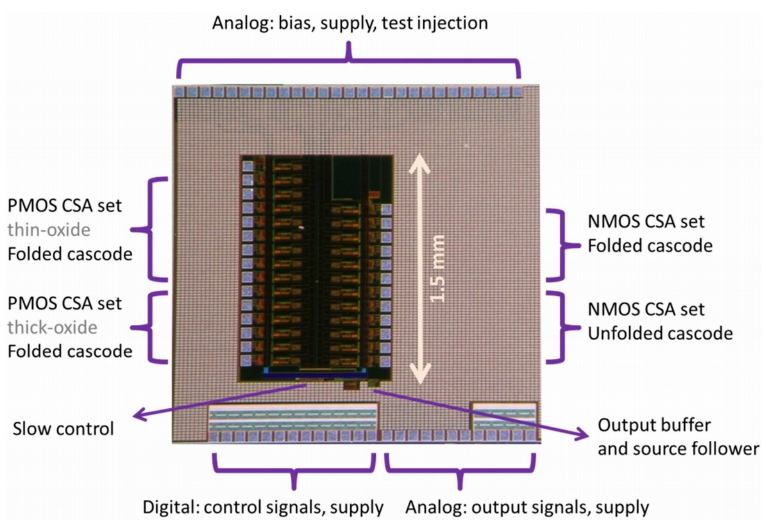


D2R1: CSA optimization

– electronic noise mainly defined by the CSA







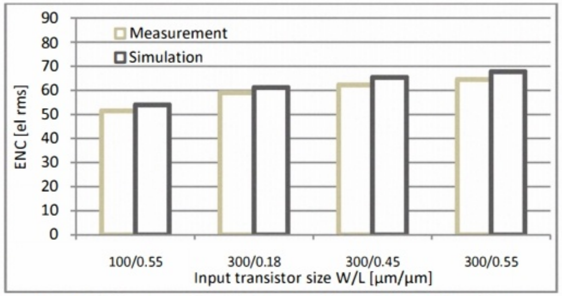


Fig. 16 PMOS thin ox. ENC_{MIN} for I_{BIAS}=2 µA I_{LEAK}=5 pA and C_{IN}=0.3 pF

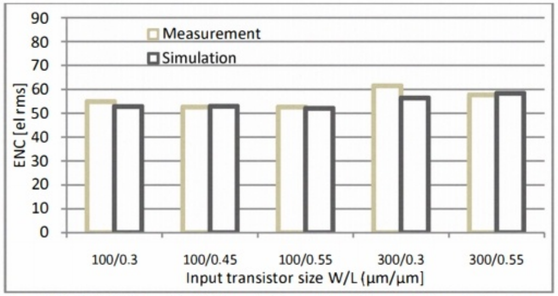


Fig. 19 PMOS thick oxide ENC_{MIN} for I_{BIAS}=10 µA I_{LEAK}=5 pA and C_{IN}=1 pF

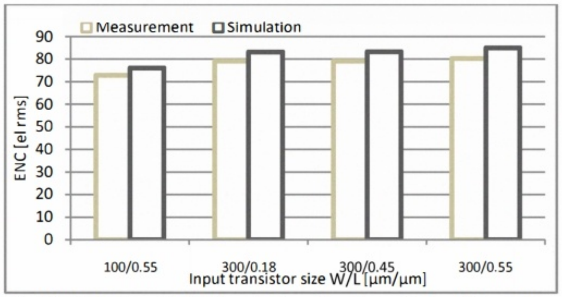


Fig. 17 PMOS thin oxide ENC_{MIN} with I_{BIAS}=2 µA I_{LEAK}=5 pA and C_{IN}=1 pF

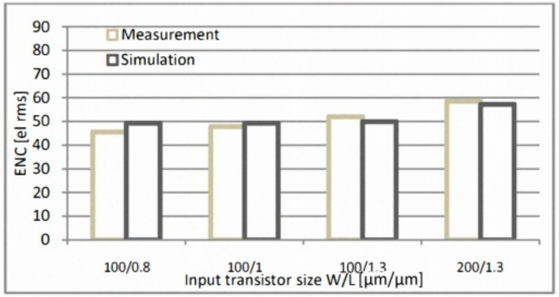
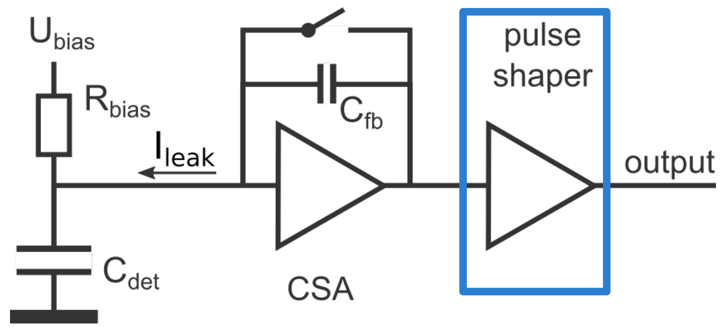


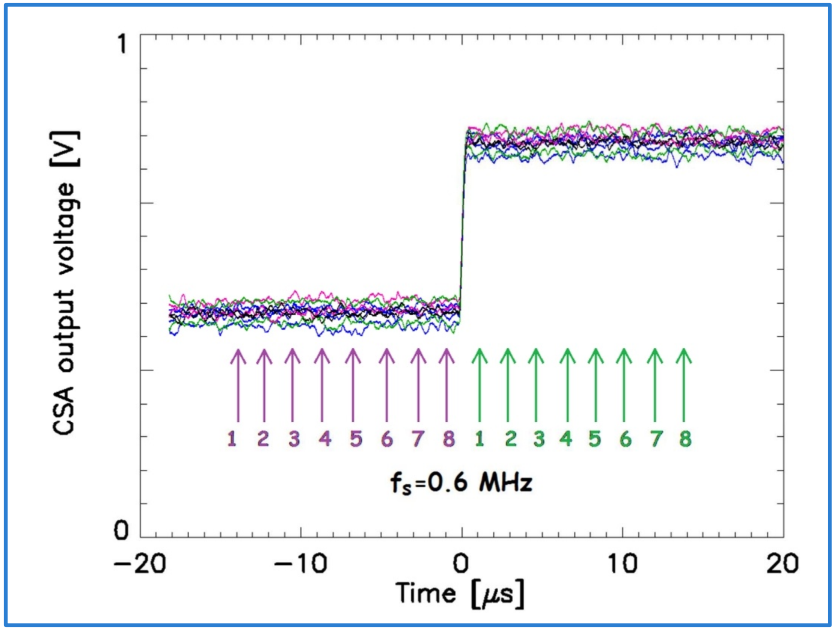
Fig. 20 NMOS thin ox. ENC_{MIN} for I_{BIAS}=10 µA I_{LEAK}=5 pA and C_{IN}=0.3 pF

see Michalowska et al., 2011, IEEE, 653-659

D2R1: filter = pulse shaper

- signal : U(t) --FT--→ signal power (f)
- noise: U(t) --FT--→ noise power (f)
- optimize SNR by attenuating more noise than signal
  - band pass: low-pass + high-pass filter
- within IDeF-X: CR-RC^N filter (semi-Gaussian)
  - implementation as analog electronics
  - realized as opamp-based active filter
  - $t_{peak} = N * RC$
- Multi Correlated Double Sampling (MCDS)
  - discrete processing method with sampling rate f_S
  - output = mean(baseline) - mean(baseline + signal)
  - averaging → low-pass filter
  - subtraction → high-pass filter
  - filter parameter can be adjusted easily: $t_{peak} = N/f_S$

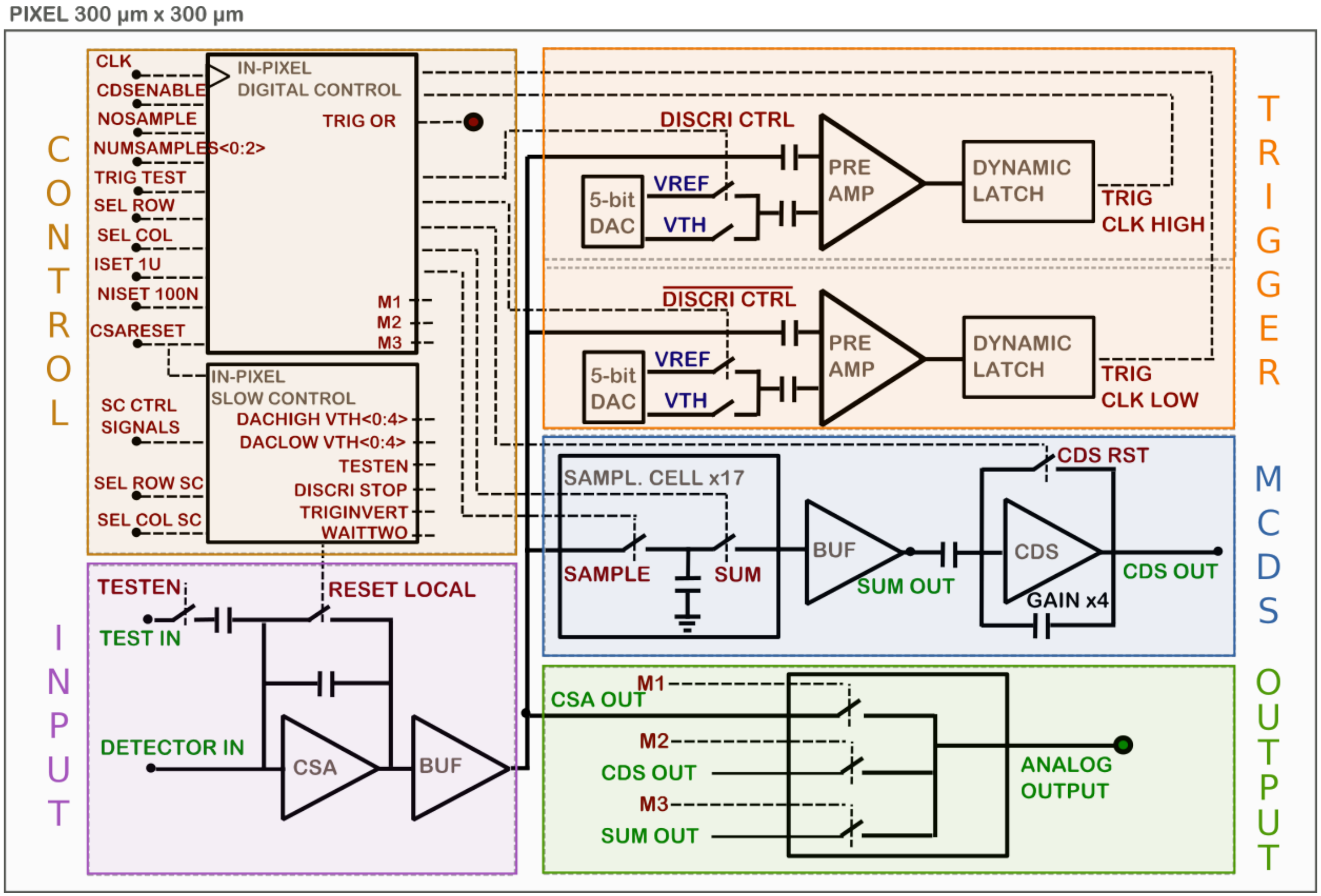




Michalowska, thesis Irfu, 2013

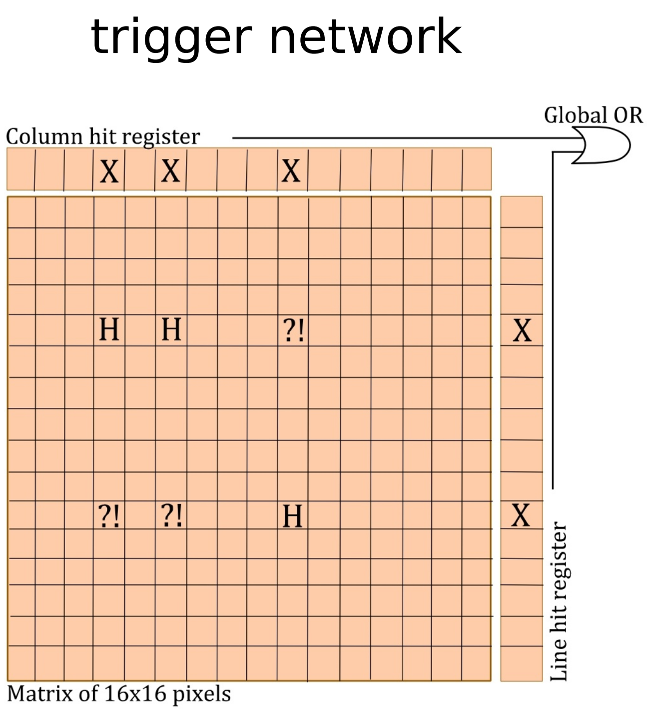
D2R1: architecture

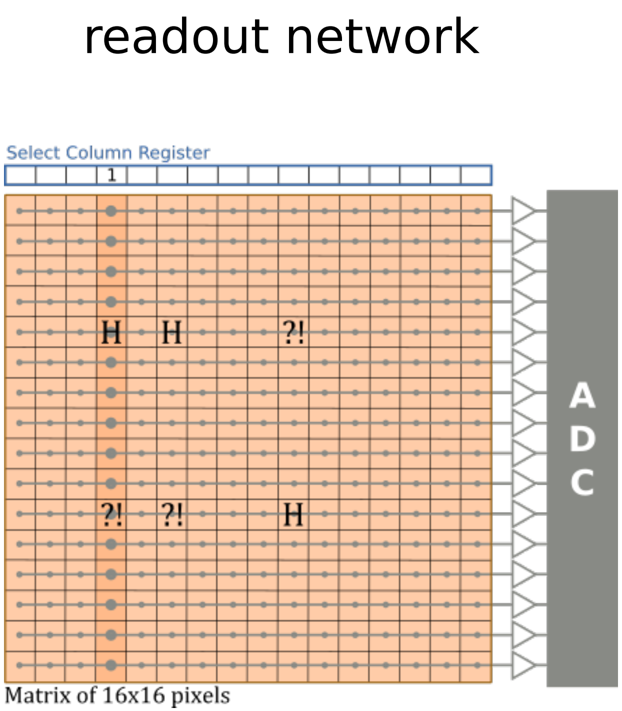
- **256 x pixel architecture**
  - CSA
  - MCDS
  - Trigger logic
  - control



D2R1: architecture

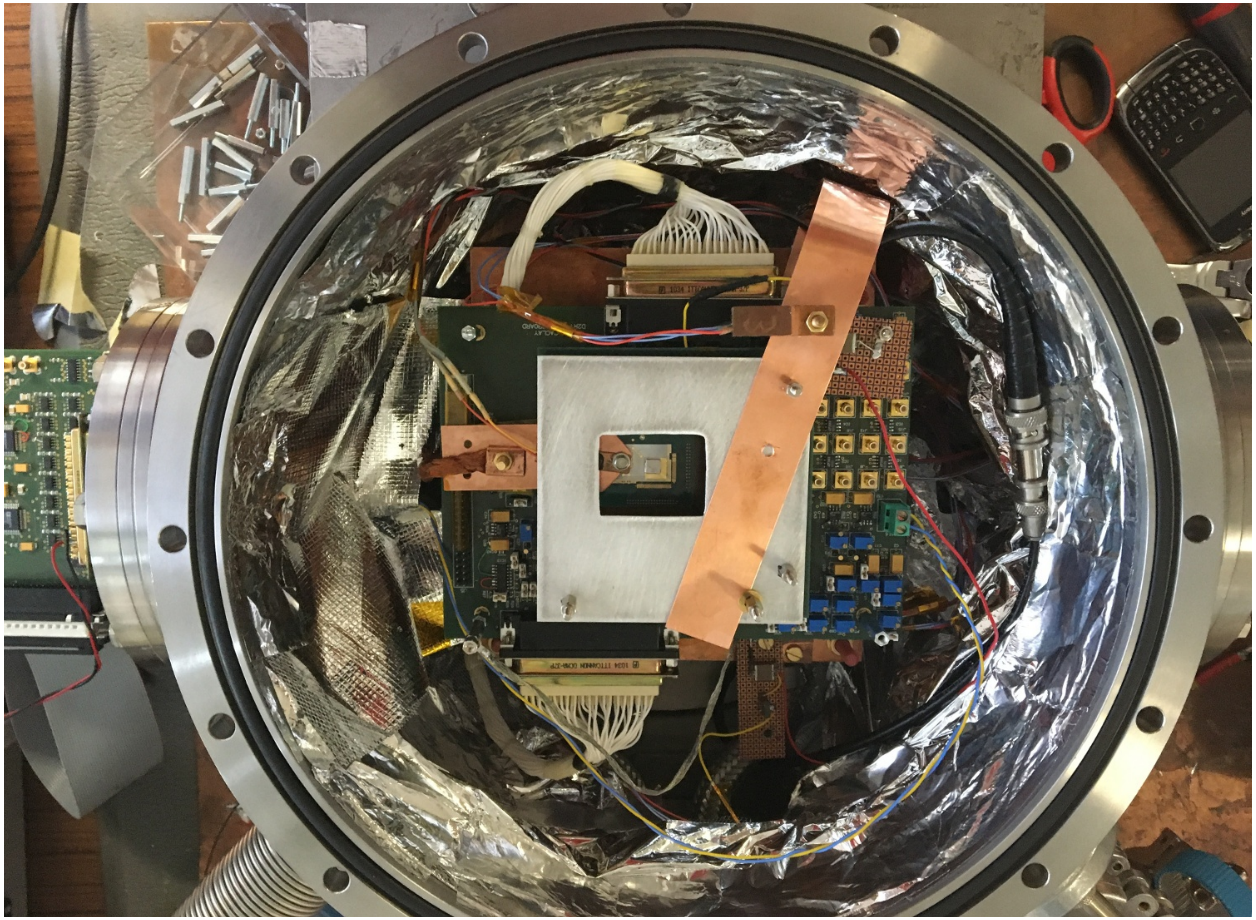
- 256 x pixel architecture
  - CSA
  - MCDS
  - Trigger logic
  - control
- **1 x top-level architecture**
  - set in-pixel slow control
  - global trigger
  - addressing column to read





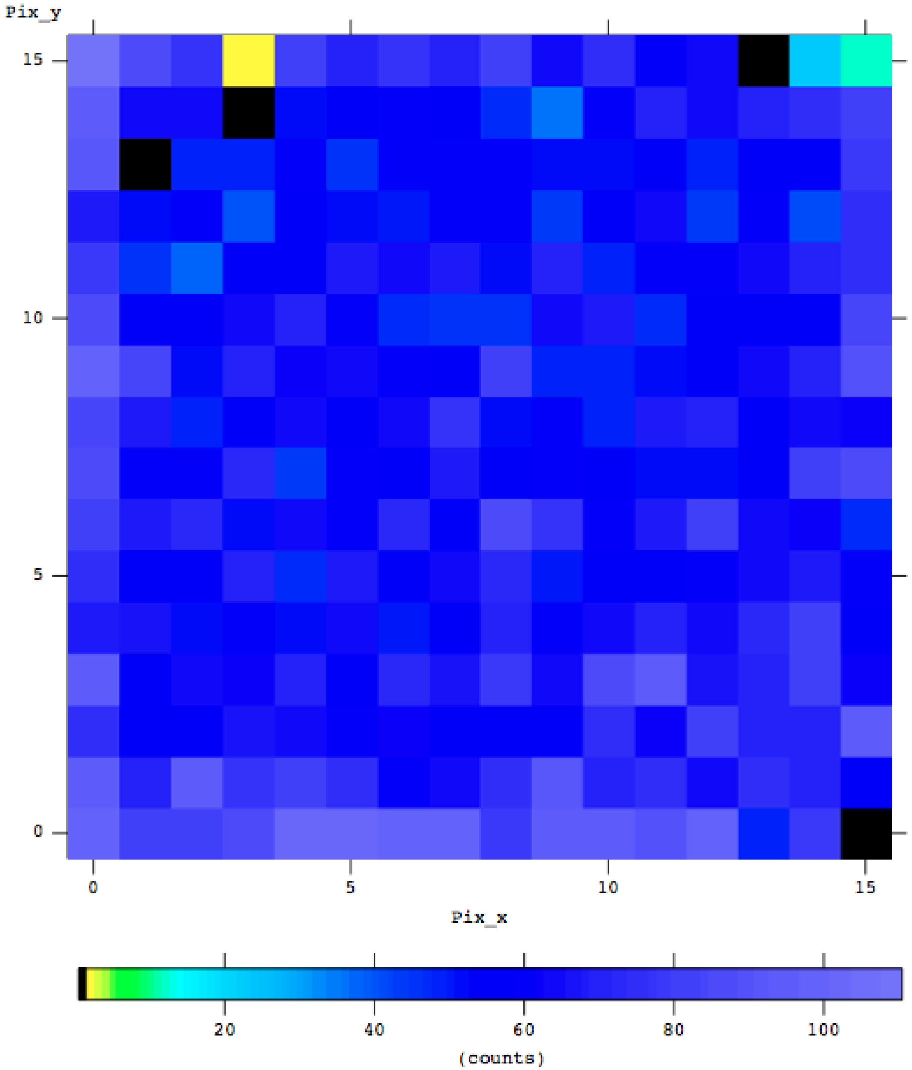
D2R1: measurements

- cooling down to T = -7°C
- depletion voltage U = 300V for d = 750 um detector thickness
- sources:
  - Am-241
  - Co-57



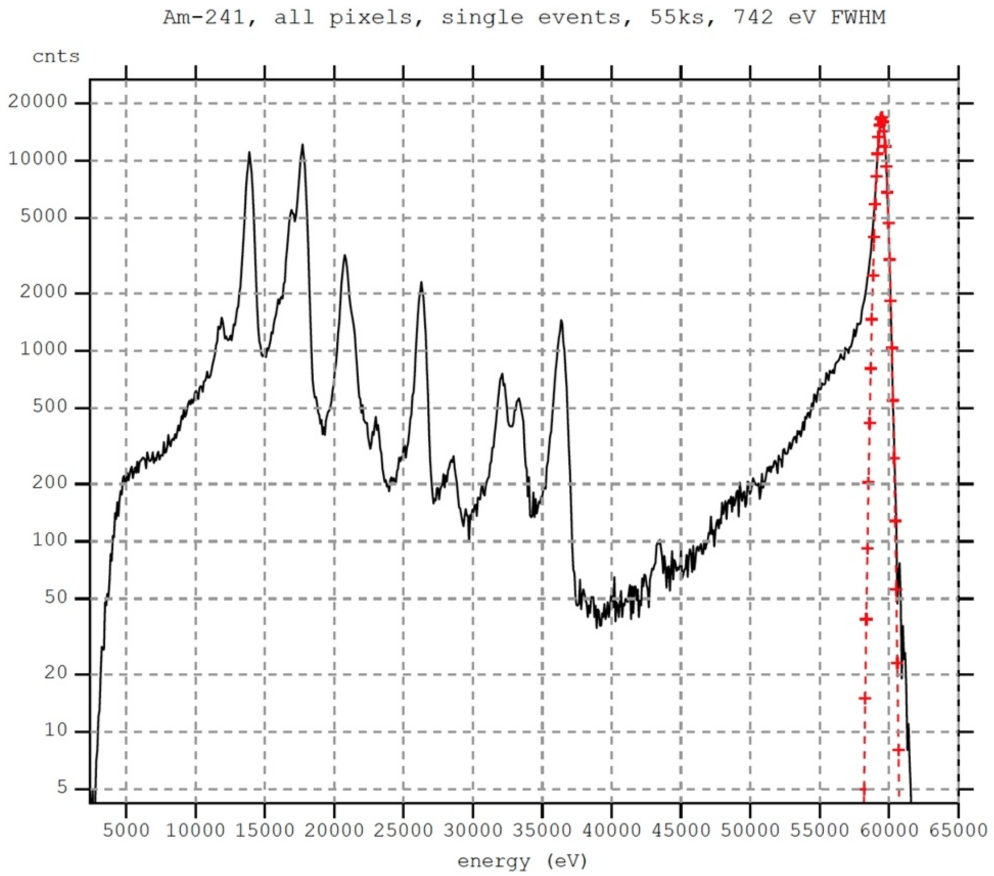
D2R1: measurements

- cooling down to T = -7°C
- depletion voltage U = 300V
- sources:
  - Am-241
  - Co-57
- results:
  - (almost) all pixel are working → bump bonding seems fine



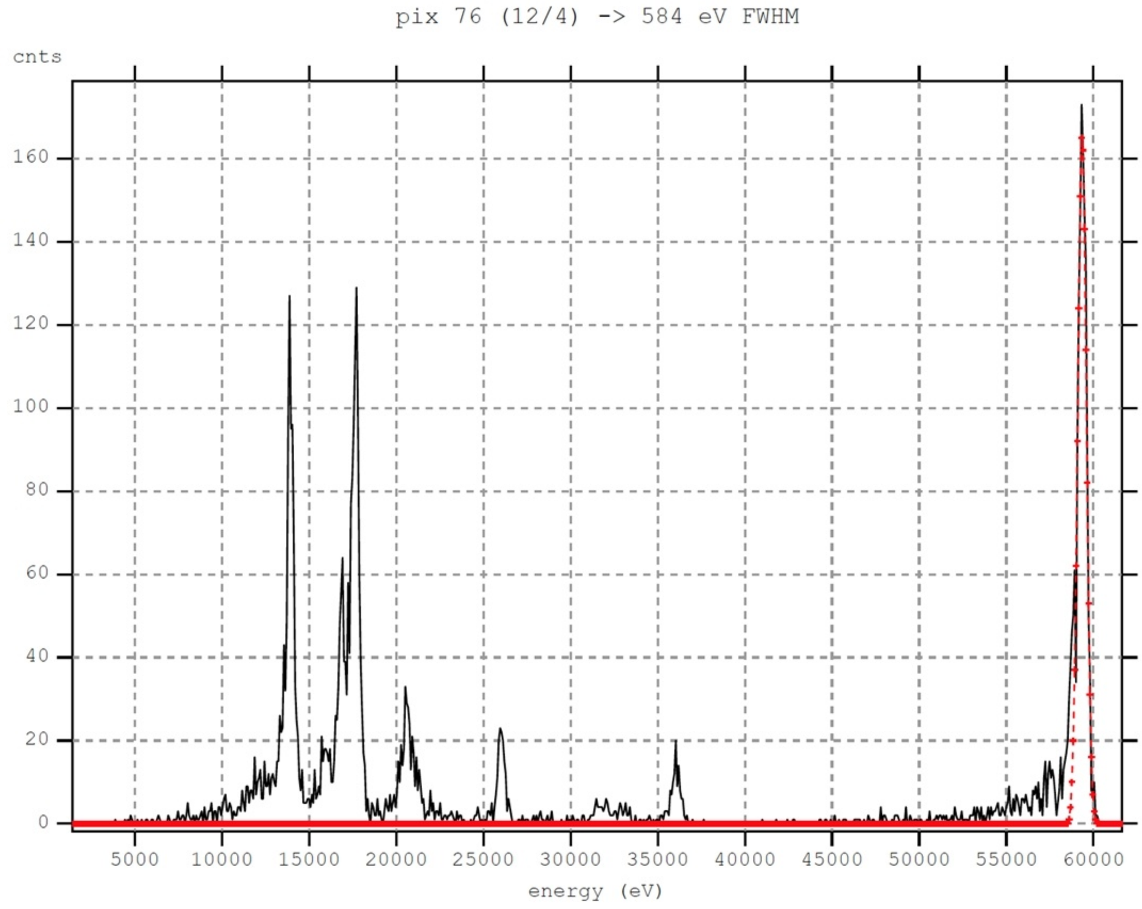
D2R1: measurements

- cooling down to T = -7°C
- depletion voltage U = 300V
- sources:
  - **Am-241**
  - Co-57
- results:
  - (almost) all pixel are working → bump bonding seems fine
  - avg. resolution: 742 eV FWHM @ 60 keV



D2R1: measurements

- cooling down to T = -7°C
- depletion voltage U = 300V
- sources:
  - **Am-241**
  - Co-57
- results:
  - (almost) all pixel are working → bump bonding seems fine
  - avg. resolution: 742 eV FWHM @ 60 keV
  - best pixel: 584 eV FWHM @ 60 keV



D2R1: measurements

- cooling down to T = -7°C
- depletion voltage U = 300V
- sources:
  - **Am-241**
  - Co-57
- results:
  - (almost) all pixel are working → bump bonding seems fine
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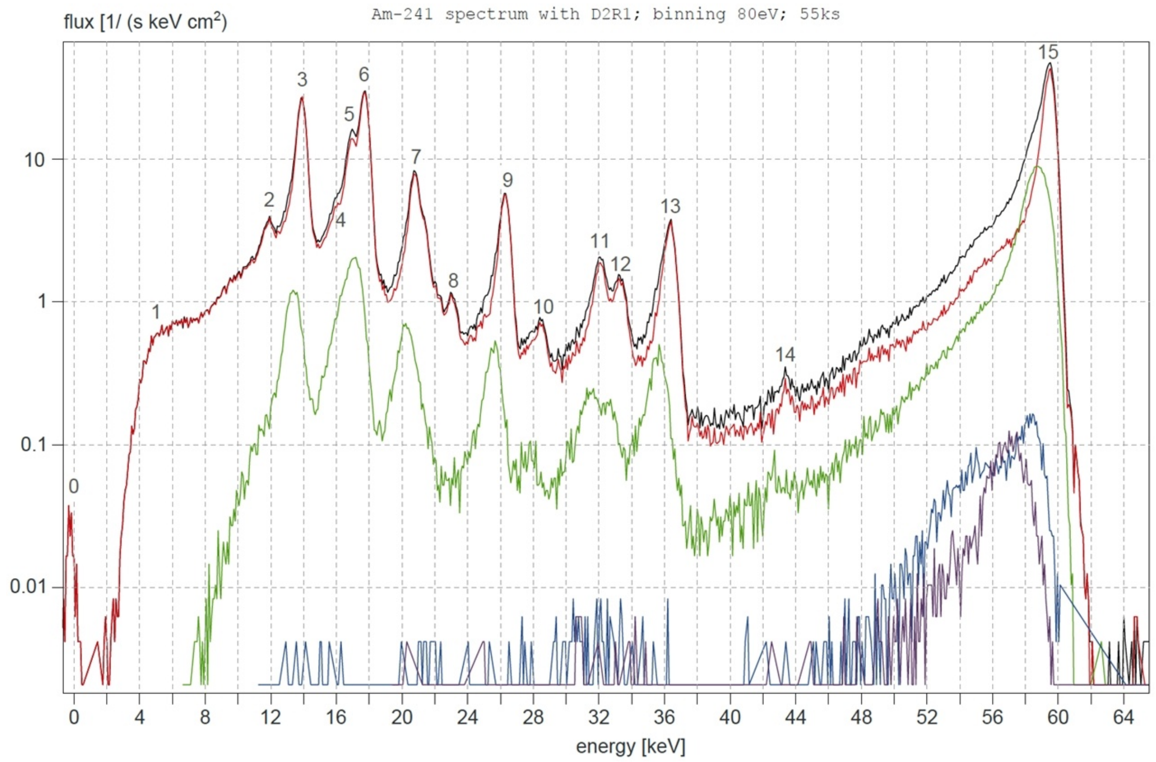
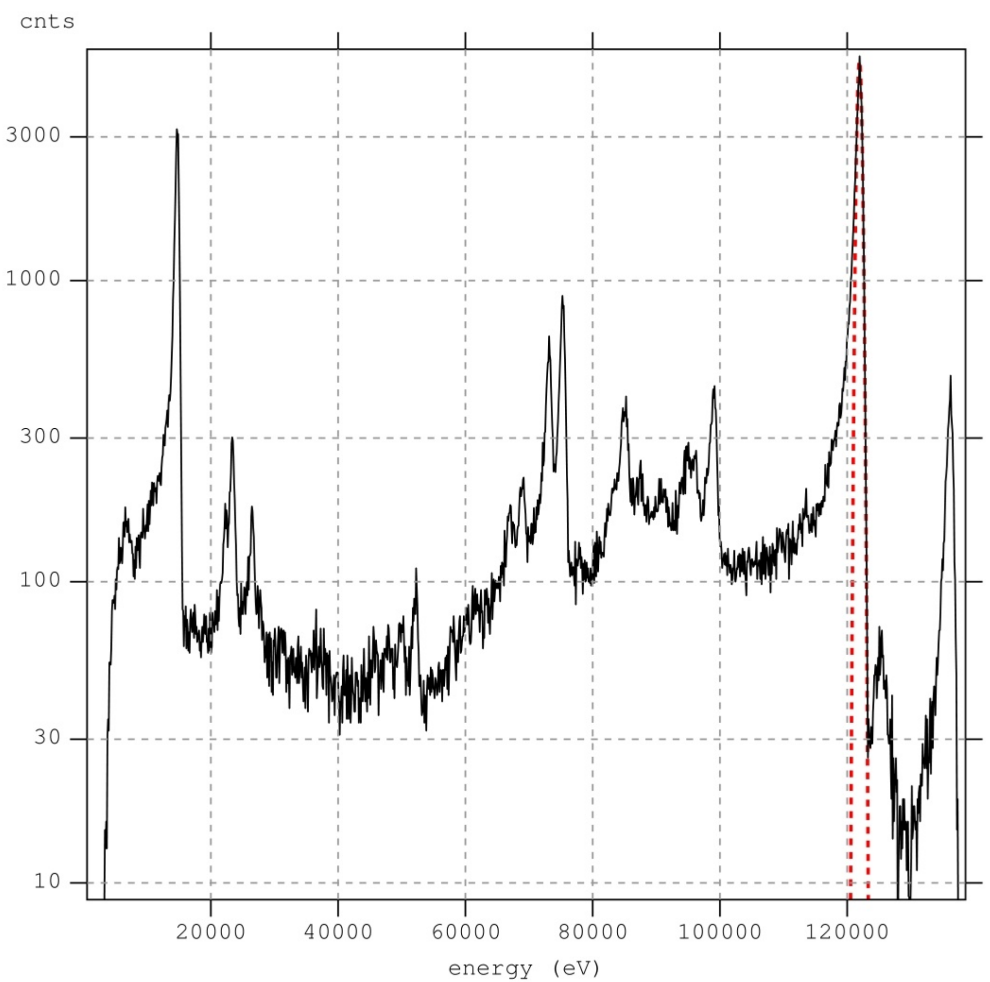
  - best pixel: 584 eV FWHM @ 60 keV



D2R1: measurements

- cooling down to T = -7°C
- depletion voltage U = 300V
- sources:
  - Am-241
  - **Co-57**
- results:
  - (almost) all pixel are working → bump bonding seems fine
  - avg. resolution: 919 eV FWHM @ 122 keV
  - best pixel: 817 eV FWHM @ 122 keV



D2R1: measurements

- cooling down to T = -7°C
- depletion voltage U = 300V
- sources:
  - Am-241
  - **Co-57**
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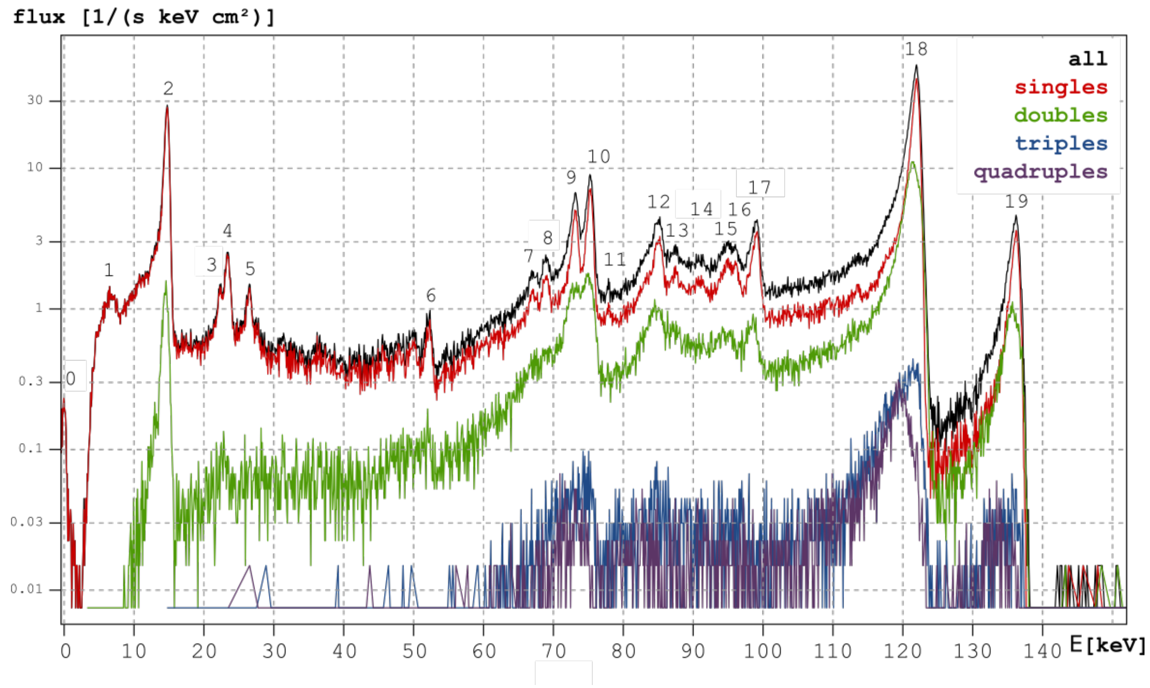
  - (almost) all pixel are working → bump bonding seems fine
  - avg. resolution: 919 eV FWHM @ 122 keV
  - best pixel: 817 eV FWHM @ 122 keV



D2R1: next steps

- **Test pixel homogeneity and bump bonding reliability with 4 more D2R1 detector modules**
- **Study splits events in more detail:**

– singles	81.2 %	for Am-241
– doubles	16.5 %	
– triples	0.6 %	
– quadruples	0.7 %	
– mismatches	1.0 %	

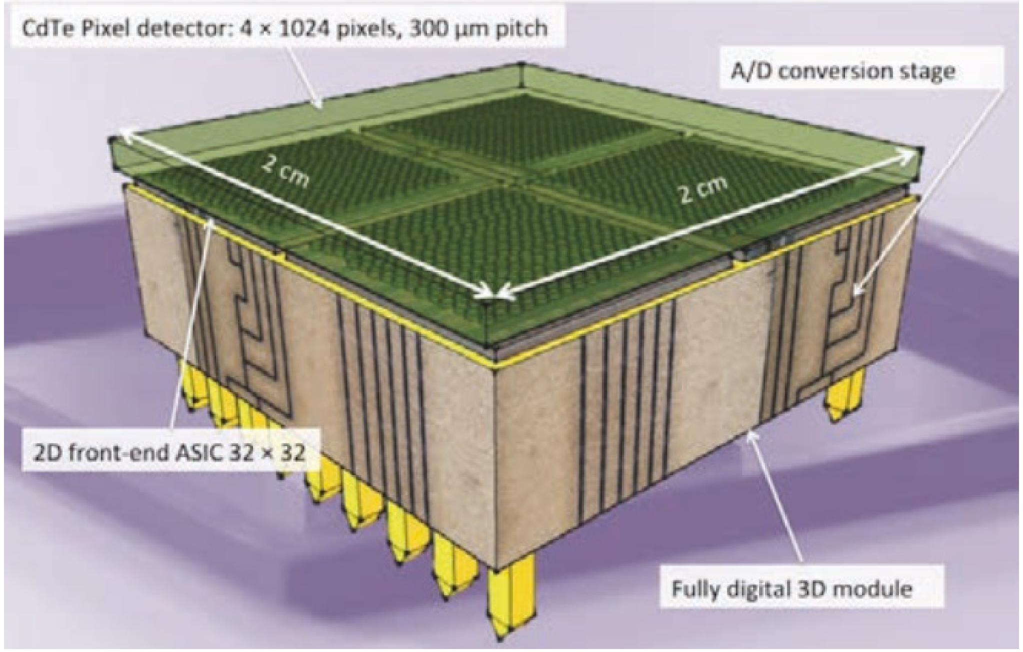
- **Investigate the application as X-ray polarimeter**

OUTLOOK: MC2

- D2R1 → D2R2:
  - 16 x 16 pixels → 32 x 32 pixels
  - 0.5 x 0.5 cm² → 1 x 1 cm²

- OWB-1: ADC
  - 32 channel 13 bit ADC for space applications

- MC2: 4 x (D2R2 + OWB-1)
  - 64 x 64 pixel
  - 2 x 2 cm²
  - fully digital (ADC included)



OUTLOOK: MC2

	ASIC	# pix	pixel pitch	detector area	thickness	spectr. res	power
			um	mm^2	mm	eV (FWHM @ 60 keV)	mW/mm^2
Caliste-64	4 x IDeF-X V1.1	8 x 8	900	10 x 10	1	900	3.0
Caliste-256	8 x IDeF-X V2	16 x 16	580	10 x 10	1	860	8.3
Caliste-HD	8 x IDeF-X HD	16 x 16	625	10 x 10	1	670	2
Caliste-O	8 x IDeF-X HD	16 x 16	800	14 x 14	2	927	1
Caliste-MC2	4 x D2R2	64 x 64	300	20 x 20	0.75 – 2.0	at least like Caliste-HD	2

References:

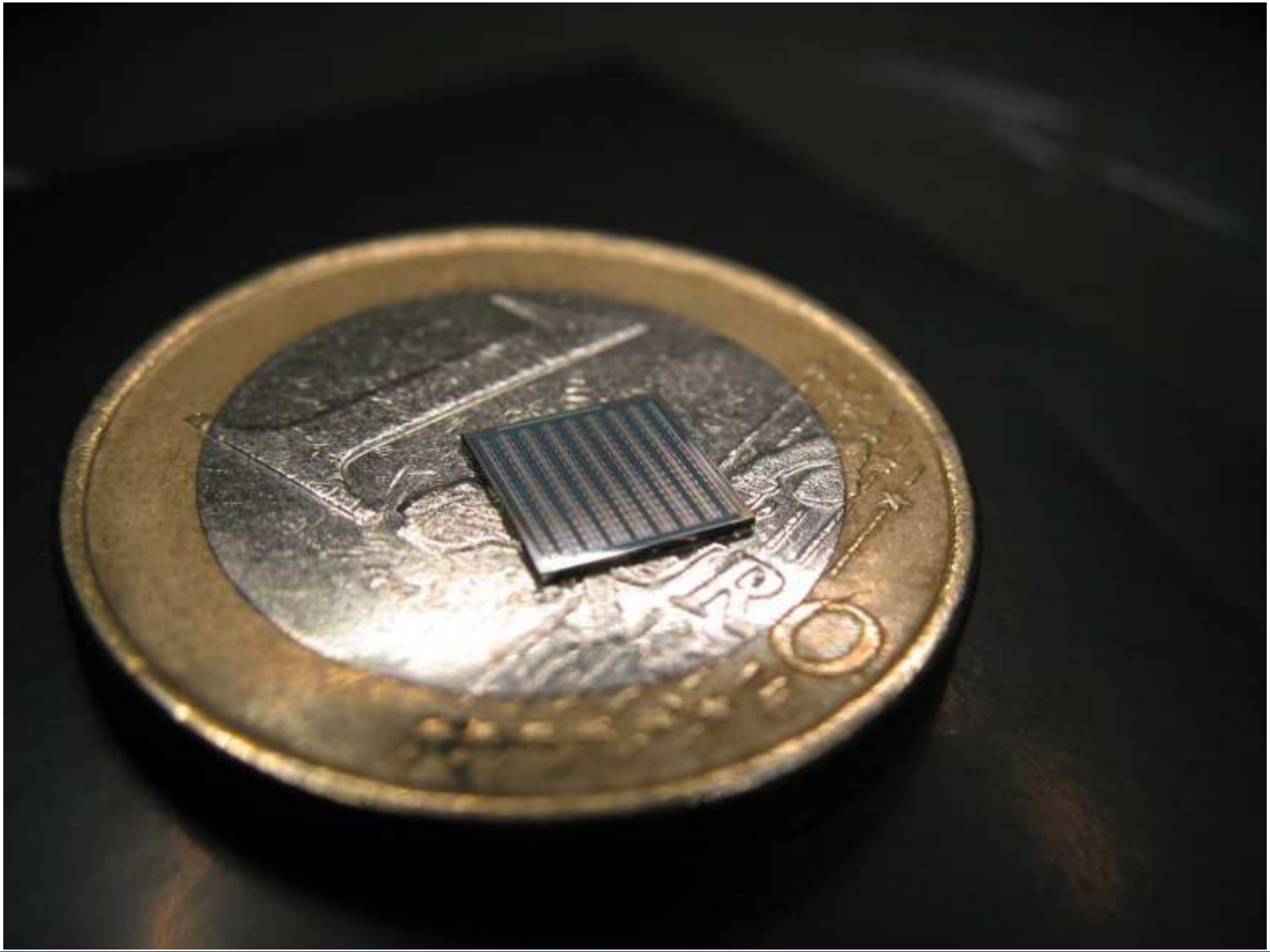
- A. Michalowska et al., 2011, “Multi-dimensional optimization of charge preamplifier in 0.18 um CMOS technology, IEEE

- A. Michalowska, 2013, “Studies and development of a readout ASIC for pixelated CdTe detectors for space applications”, Ph. D. dissertation, Université Paris Sud – Paris XI, Saclay, France

- F. Bouyjou et al., 2017, “A 32-Channel 13-b ADC for Space Applications”

Thanks for your attention !

D2R1



D2R1: trigger

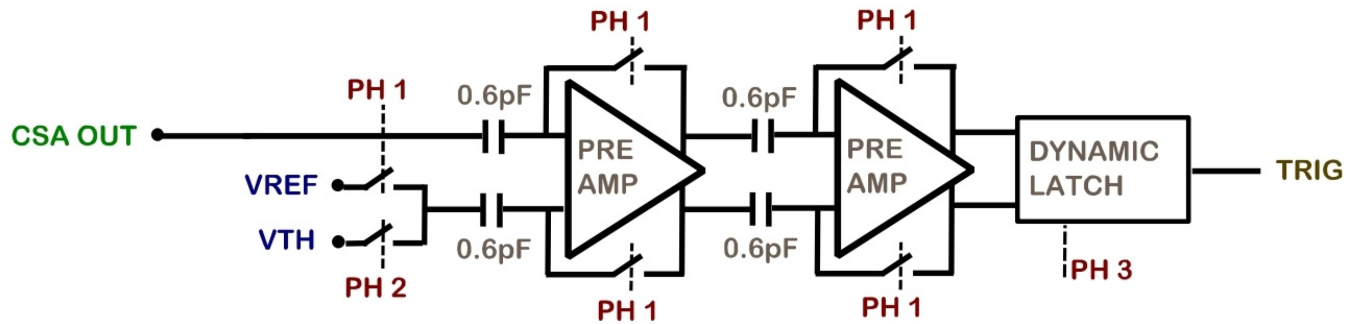


Figure 4.6 Block diagram of a single discriminator in the D^2R_1 readout channel. Each channel contains two identical discriminators, operating with interleaved clock phases.

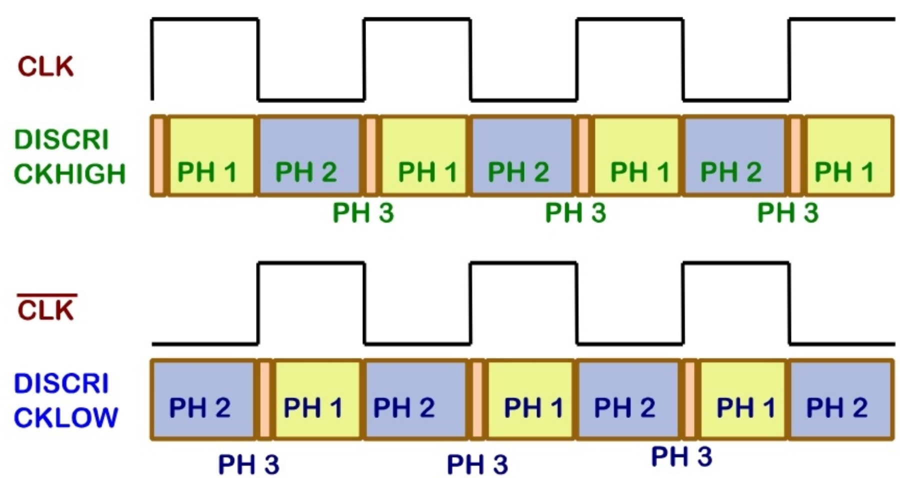


Figure 4.7 Chronogram of control phases of two parallel discriminators of D^2R_1 readout channel. One supervised by the CLK signal and one by the $\overline{CLK}$ signal.