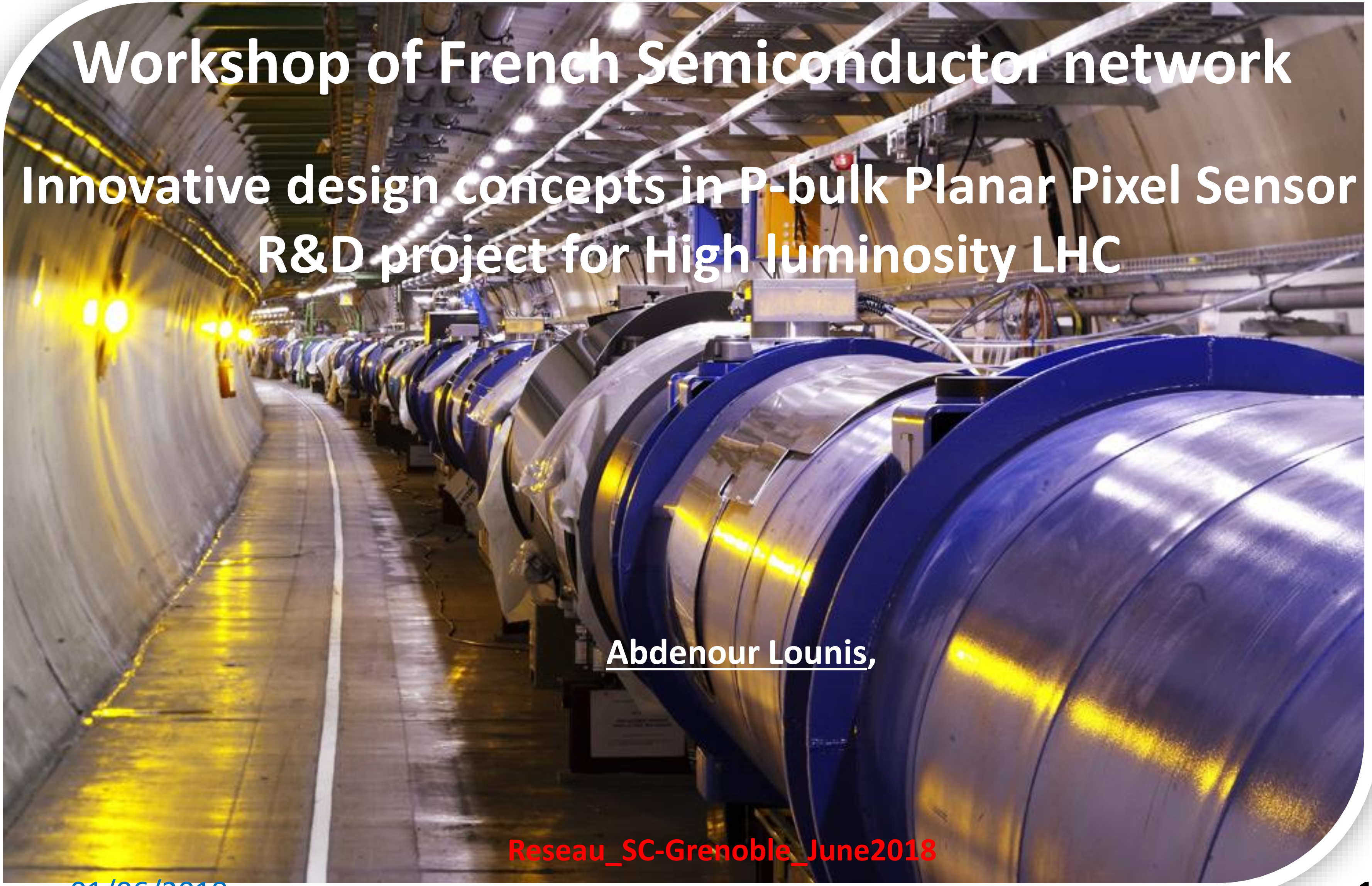


Workshop of French Semiconductor network

Innovative design concepts in P-bulk Planar Pixel Sensor R&D project for High luminosity LHC

Abdenour Lounis,

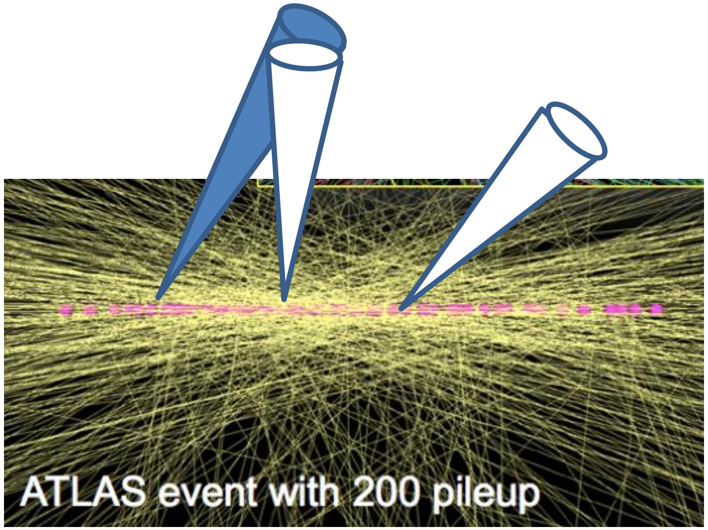
Reseau_SC-Grenoble_June2018

Framework : ATLAS Upgrade for HL-LHC

- **High Luminosity LHC (HL-LHC)**
  - Start around 2026
  - Target : $\sqrt{s}$=14TeV L=5x10^{34}cm^{-2}s^{-1} $\int Ldt$=3000-4000fb^{-1}
  - Physics program focus on the precise measurements of the Higgs couplings and BSM searches.
- **Tracking detector is key element**
  - To keep B/τ-tagging performance up to μ=200 pileup in an event.
  - Need to launch **innovative solution for detectors**, mechanics, efficient triggering and advanced analysis technics.

The ATLAS upgrade plans full replacement of Inner Tracker

- All silicon tracker (Pixel & Microstrip)
- ***Requirements for Pixel detector***
  - Pixel Size : 50um x 50um
  - Radiation @ outer layer : 3x10^{15}n$_{eq}$/cm^2
  - Thickness : 100 or 150um
  - Low noise (<100e) → 600e stable threshold
  - High Readout Rate : 5.2Gbps (or 4x1.28Gbps)



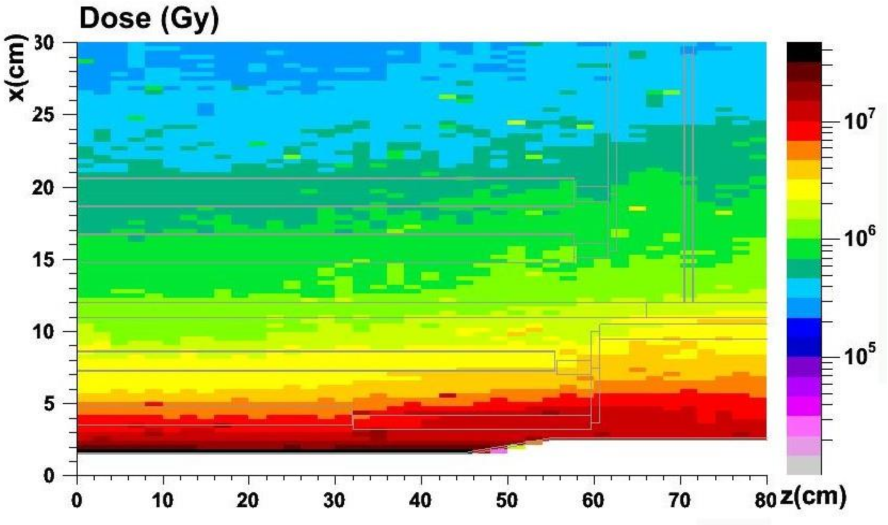
The question of the high radiation at HL-LHC

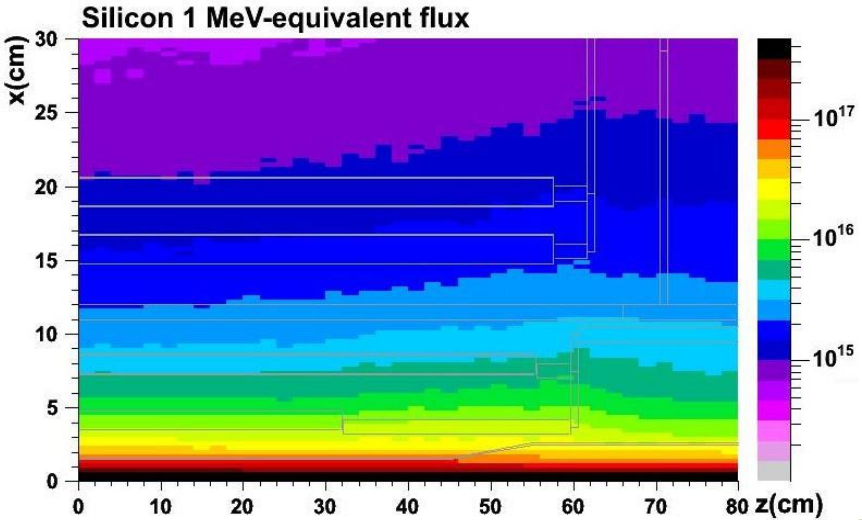
Why new sensors for HL-LHC ?

- Integrated luminosity: 3000 fb^{-1},
- so : for low radius area (<5 cm radius):
  - $2x10^6$ n_{eq} cm^{-2} (1500 Mrad) : *severe irradiation damage*
- For higher radius (25 cm) :
  - Up to 10^{15} n_{eq} cm^{-2} (100 Mrad)
  - Several m^2 of silicon

For outer region > 25 cm radius ~ 10^{14} n_{eq} cm^{-2}

  - Up to 200 m^2 of silicon





Drive to idea to construct a new inner tracker

- Radiation damage =➔ material with more radiation tolerance for bulks
- Radiation tolerant ASIC readout
- Higher occupancy =➔ granularity

Radiation Damage in Silicon Sensors

- Two general types of radiation damage to the detector materials:

- **Bulk (Crystal) damage due to Non Ionizing Energy Loss (NIEL)**
  - displacement damage, built up of crystal defects –

  I. Change of effective doping concentration (higher depletion under- depletion)

  question : How does it change ??

  II. Increase of leakage current (increase of shot noise, thermal runaway)

  How can we lower this effect ??

  III. Increase of charge carrier trapping (loss of charge)

  How do we recover charge loss?

- **Surface damage due to Ionizing Energy Loss (IEL)**
  - accumulation of positive in the oxide (SiO_2) and the Si/SiO_2 interface – affects: interpixelcapacitance (noise factor), breakdown behavior, …

- **Impact on detector performance and Charge Collection Efficiency**
  (depending on detector type and geometry and readout electronics!)

TCAD simulation play a key role !!

Signal/noise ratio is the quantity to watch

$\Rightarrow$ *Sensors behavior very sensitive to radiation damage !*

Reverse Current

- Diffusion current
  - *Negligible for a fully depleted detector, but function of T*
- Generation recombination current
  - From generation in the depletion region
  - *Reduced by using material pure and defect free*

  - ***Anyway Must keep temperature low & controlled***

$$n_i^2 = N_C N_V \exp\left(-\frac{E_g}{kT}\right) \qquad j_{gen} \propto T^{3/2} \exp\left(\frac{1}{2kT}\right) \qquad j_{gen} \times 2 \; for \; \Delta T = 8K$$

Radiation-hard sensors

1. Radiation induced leakage current

independent of impurities; every 7°C of temperature reduction halves current

⇔ cool sensors to ≈ -25°C

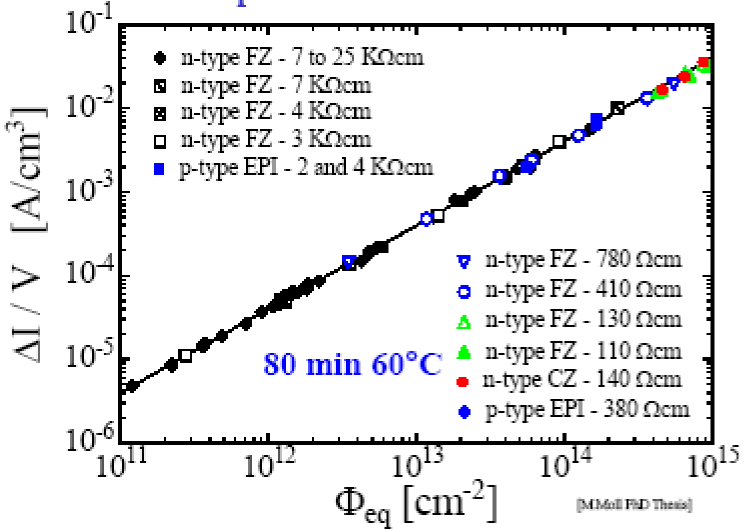
2. “type inversion” from n to p-bulk ⇔ increased depletion voltage

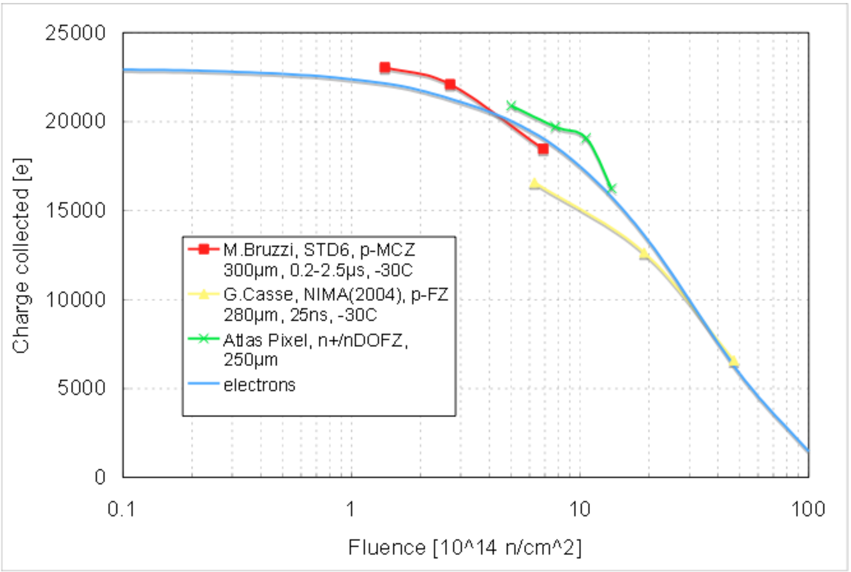
oxygenated silicon helps (for protons);
n+-in-n-bulk or n+-in-p-bulk helps

3. Charge trapping

the most dangerous effect at high fluences
⇔ collect electrons rather than holes
⇔ reduce drift distances =➔ thinning or innovation!!

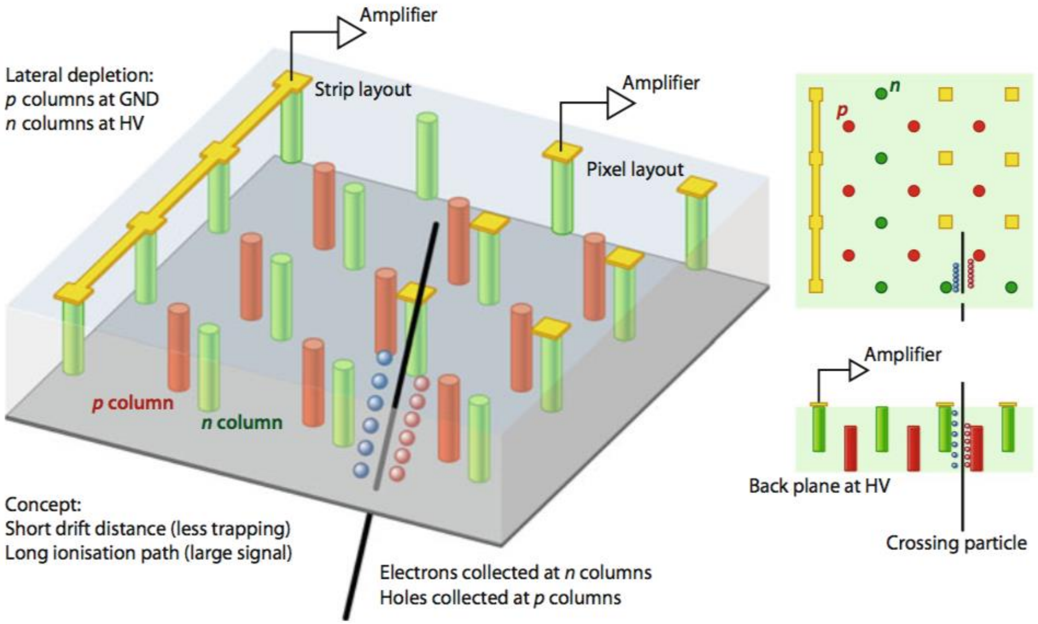
…. with particle fluence:

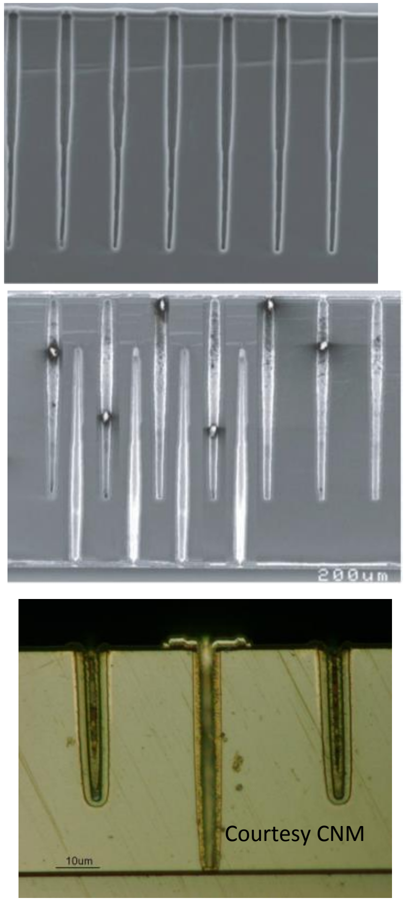




Reduce Trapping: 3D Concept

- Charge drift horizontally





Courtesy CNM

Drawback : higher thickness, so higher capacity, Yield issue, cost …

Noise issue

- Depends upon detector capacitance and reverse current : TCAD design helps !
- Depends upon electronics design: Low noise E
- Function of signal shaping time =
- Lower capacitance ⇒ lower noise =
- Faster electronics ⇒ noise contribution from reverse current less significant
- Rad Hard electronics => towards CMOS Sub-micron technologies (TSMC 65 nm)

Depletion width

- Depletion Width depends upon Doping Density:

$$W = \sqrt{\frac{2\varepsilon V}{q}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)}$$

Doping profile study through Secondary Ions Mass spectroscopy SIMS

- For a given thickness, Full Depletion Voltage is:

$$V_{fd} = \frac{qN_D W^2}{2\varepsilon}$$

- W = 300µm, $N_D \sim 5 \times 10^{12}$cm^{-3}: V_{fd} = 100V

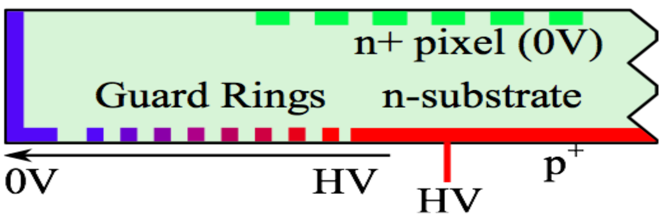
But for irradiated 300 um sensors, for 2x2 cm2 pixel sensor of 300 um thickness Vfd # 1000 V !!

Sensor technology improvement

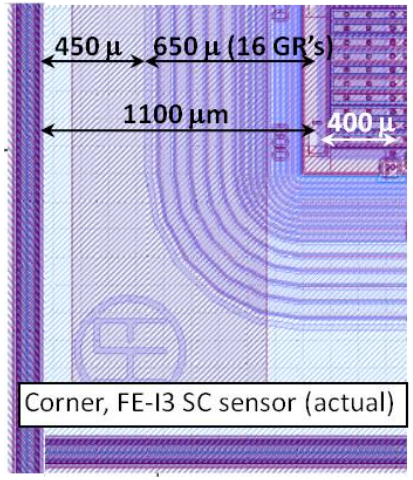
Irradiation issue: Planar technologies

ATLAS CONFIGURATION

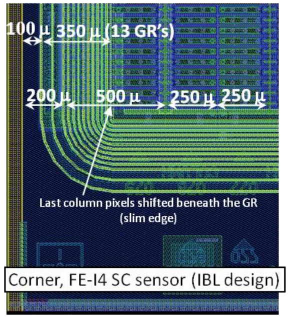
n-in-n



- Double sided process
- Pixels are under guard rings
- Mainstream design



Corner, FE-I3 SC sensor (actual)



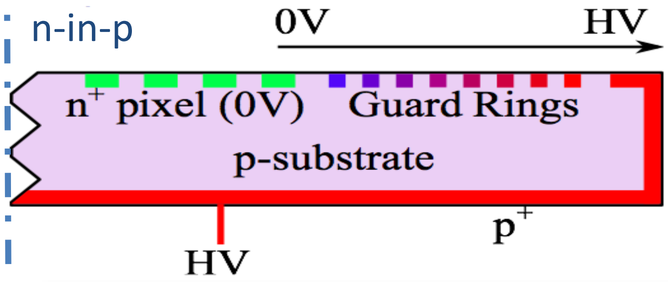
Last column pixels shifted beneath the GR (slim edge)

Corner, FE-I4 SC sensor (IBL design)

Edge efficiency to be improved

ATLAS HL-LHC

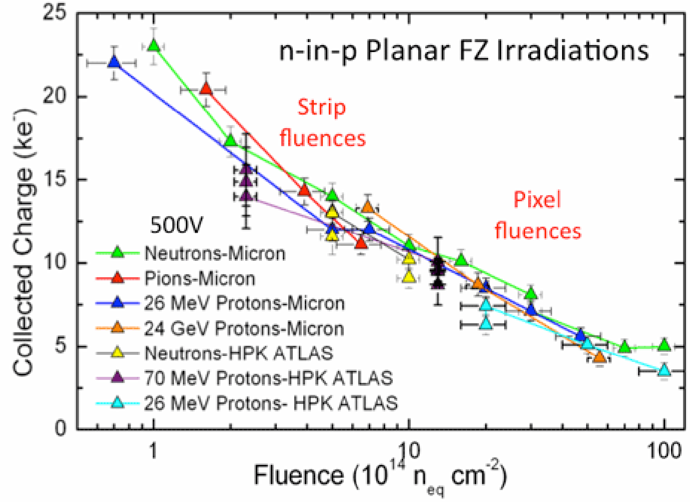
n-in-p



- Simple sided process
- No alignment needed between the two faces
- Improved radiation hardness

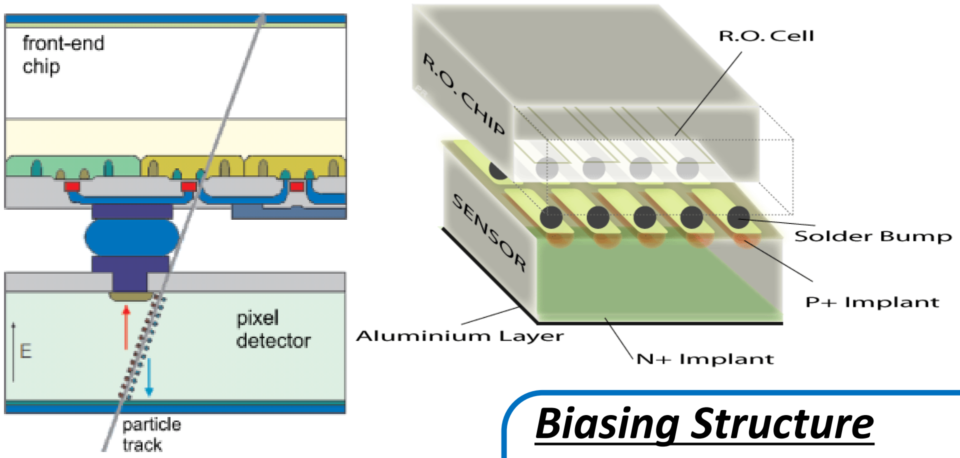
More foundries available, testing and handling easier

- Cost reduction
- Danger : short between sensor and readout chip

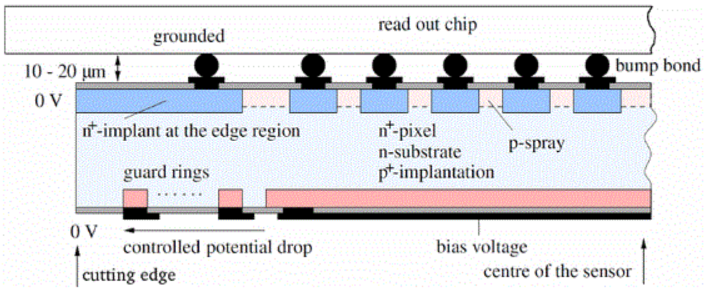


Summary of R&D issues

Elementary pixel cell



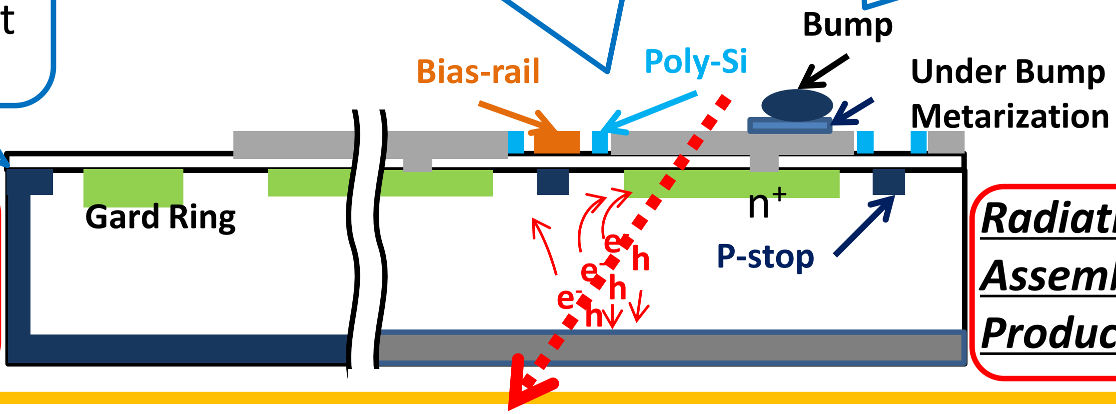
Pixel Module assembly



Biasing Structure
- Optimize Biasing structure
- Higher Efficiency at Pixel boundary

Bumpbonding
- Better UBM material
- Higher Flip-Chip Yield

Active Edge
- Smaller Edge size
- Higher Efficiency at Edge region

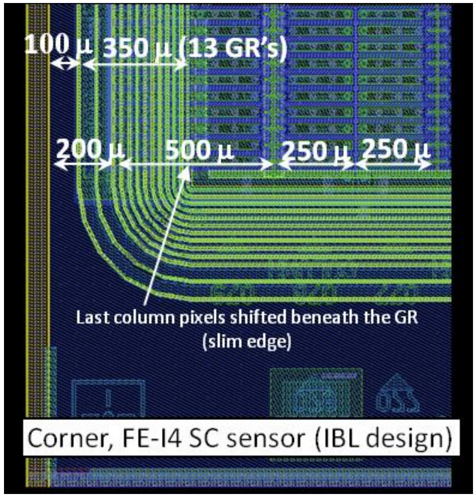


Simulation
- Doping concentration
- Charge collection

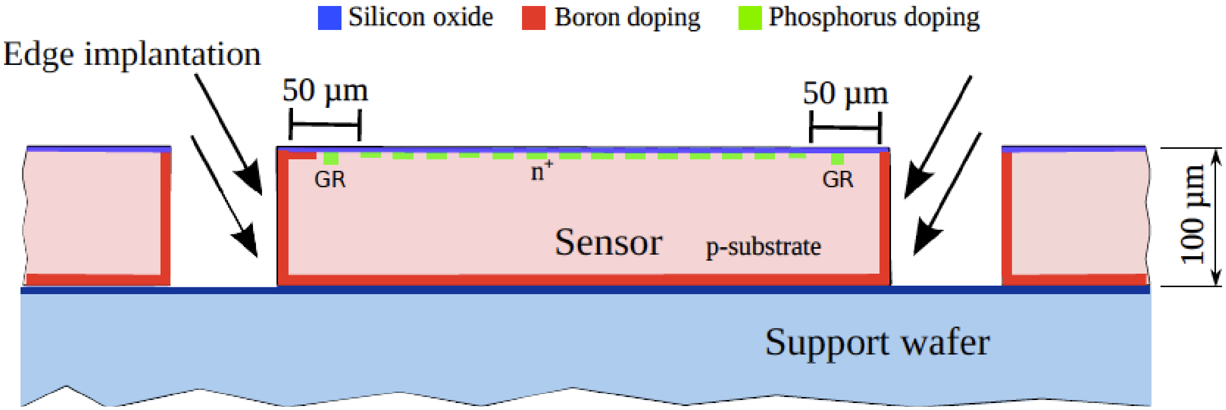
Radiation Tolerance
Assembly
Production…

R&D on Active Edge issue

- Active edge designs for planar pixels.
  - To decrease the Edge inefficiency, active edge process has been developed over 4 years with VTT.
  - To achieve a fully efficient and slim edge sensor, edge implantation (Boron) is performed.
  - 100-200um thick sensor with this active edges makes it a very attractive candidates for the inner layer(s).
  - Guard ring number are optimized.



Previous slim design

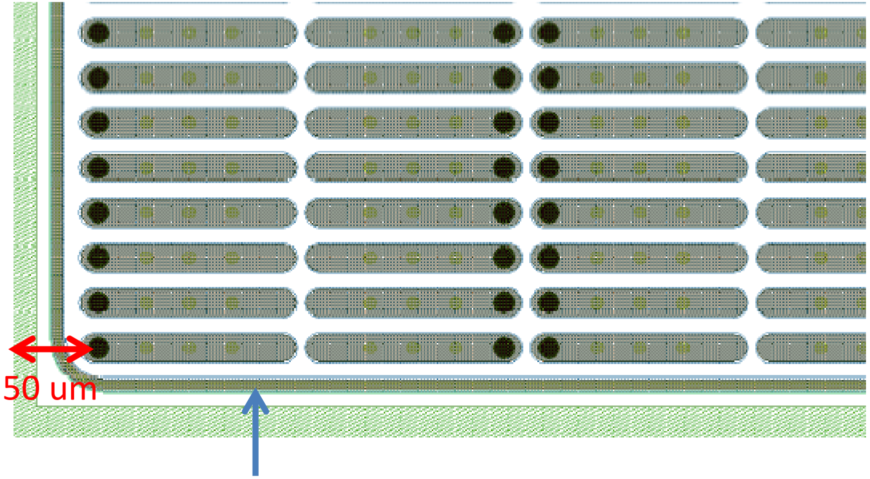


Increase edge efficiency

- Some examples of Planar pixel designs
  - Investigate various n-in-p planar pixel sensors designs with the active edge design produced by **ADVACAM company (Norway);**
  - Calculate the global and edge efficiency ;

DUT#20

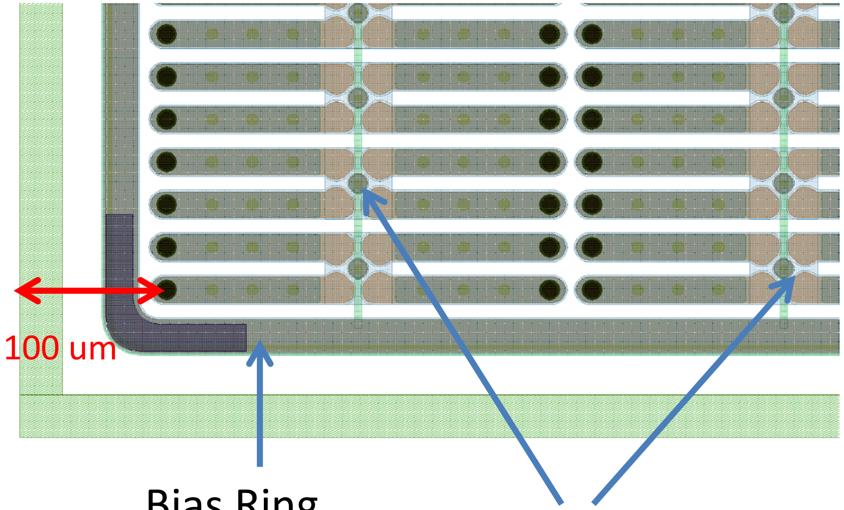
ADVACAM NP150-6-1A
(thickness – 150 um) active edge



Guard Ring

DUT#21

ADVACAM NP100-7-2A
(thickness – 100 um) slim edge

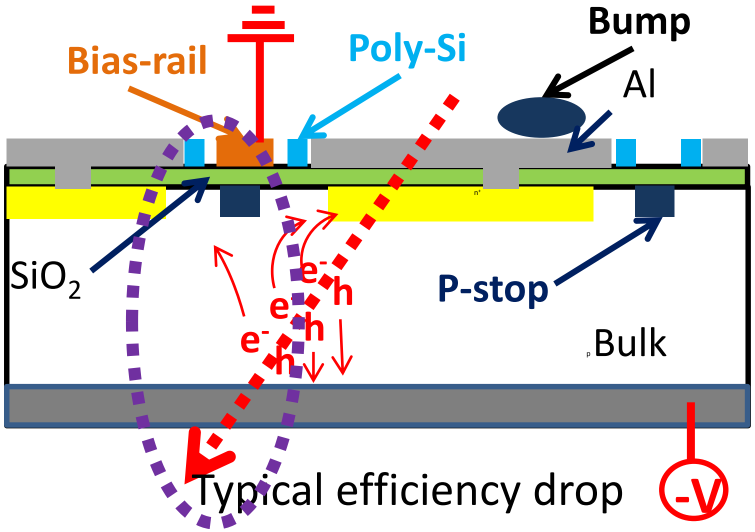


Bias Ring

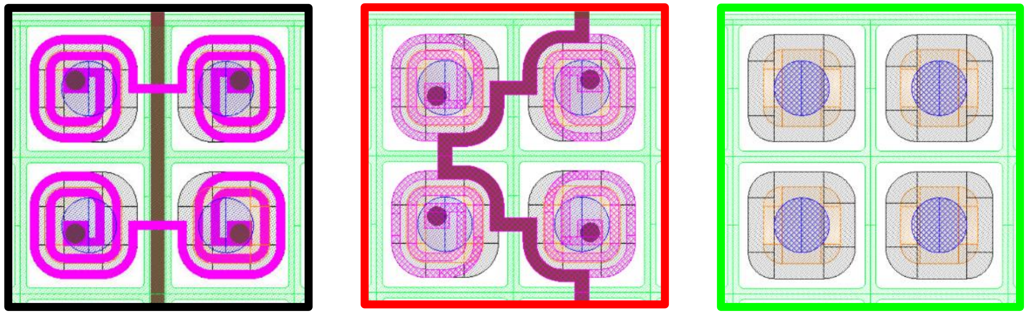
Punch-through structure

Biasing structure optimization

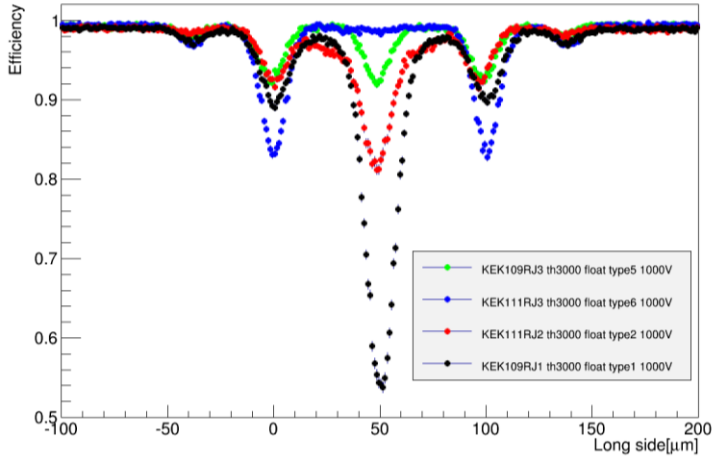
- <u>Biasing Structure</u>
  - Plays a role for pixel biasing before bump bonding. When pixel is bump bonded, in case of missing bond connection, bias grid hold the unconnected pixel to the ground (prevent discharge)
  - **On the other hand we observed Efficiency drop under the structure due to field effect.**



- Biasing structure optimization
  - **Better Efficiency with optimized bias rail path.**

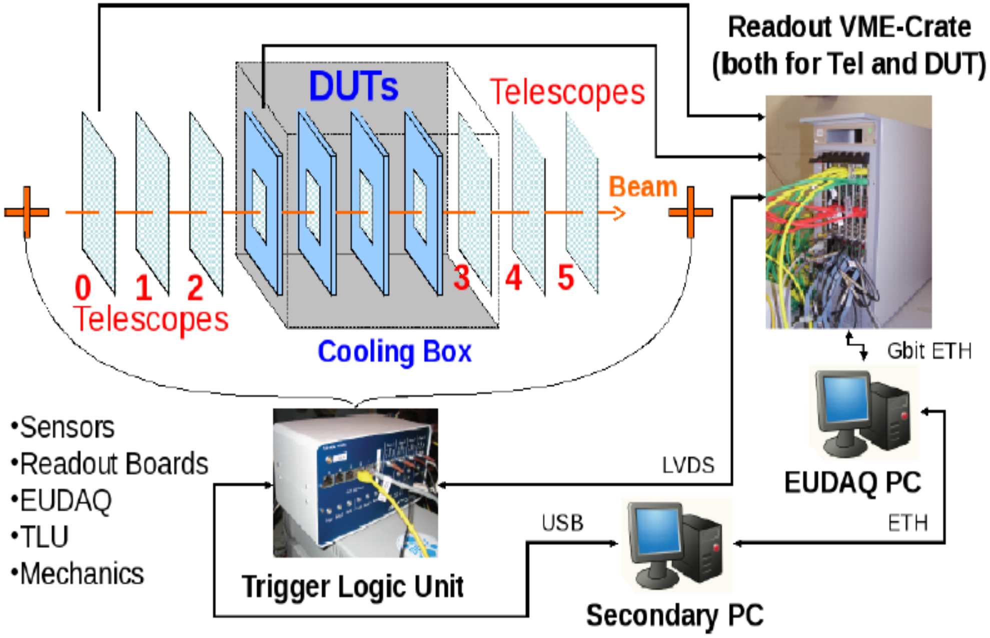


Testbeam result in Aug. 2016 @ CERN

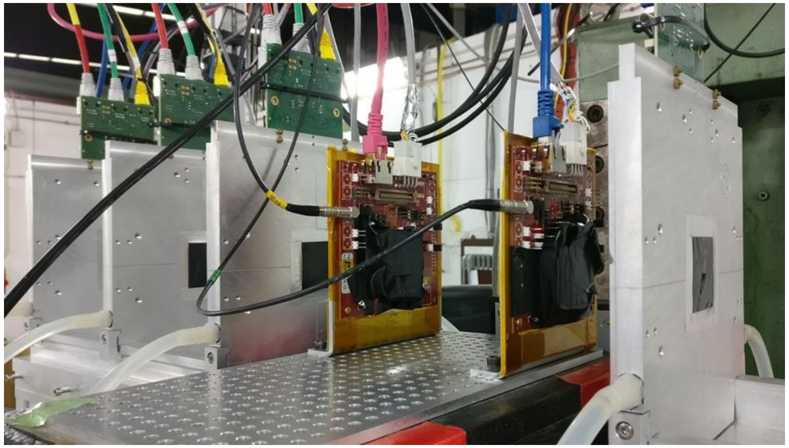


Instrumental Facilities and expertise

- Test Beam setup



- Sensors
- Readout Boards
- EUDAQ
- TLU
- Mechanics



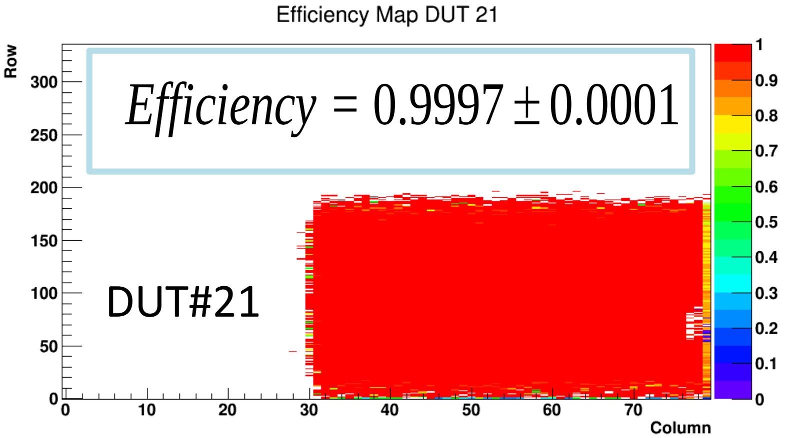
- EUDET telescope;
- Telescope planes are Mimosa26 sensors (1152 x 576) with a pixel pitch of 18.4 μm;
- 50μm thick;
- System wide synchronization via trigger hardware
- Pixel read-out systems fully integrated into EUDAQ software framework
- FE can be configured via data acquisition (DAQ) hardware connected to PC
- Multiple DAQ systems for lab tunings and measurements: USBPix, RCE, etc.

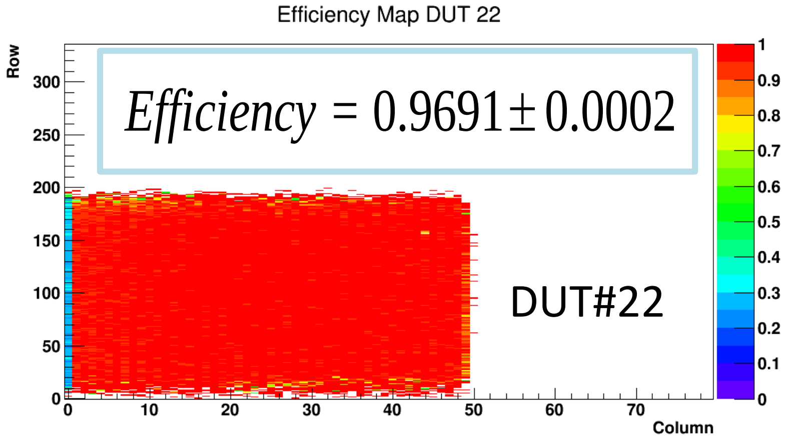
- Particles:
- DESY: electrons 1 – 6 GeV
- CERN : pions 20 – 120 GeV

Efficiency maps

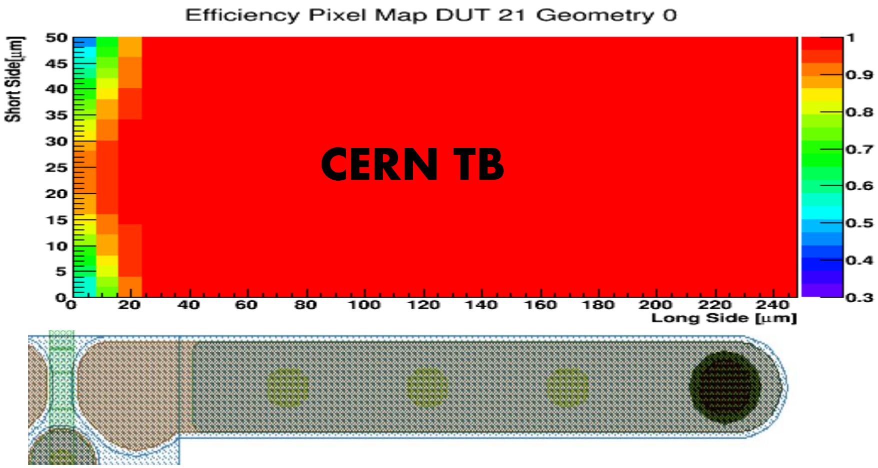
- *Overall sensor efficiency*

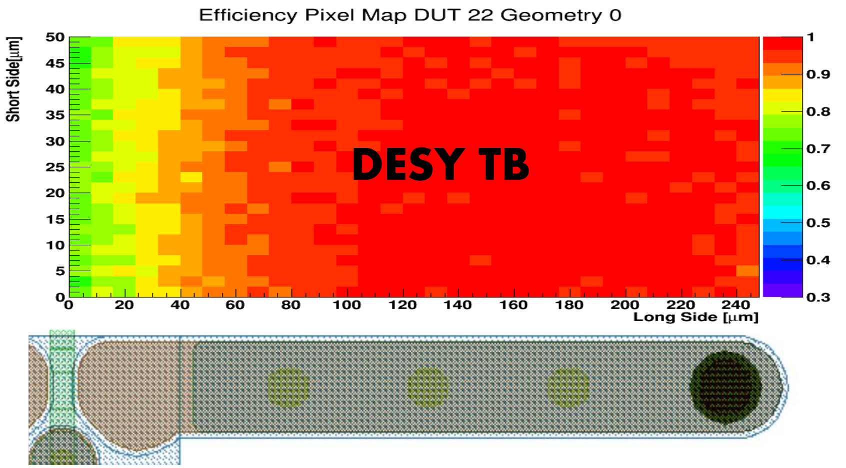
$$Efficiency = \frac{Number\ of\ Matched\ Tracks}{Number\ of\ Total\ Tracks}$$





- *In-pixel efficiency map* (slim edge DUT#22)

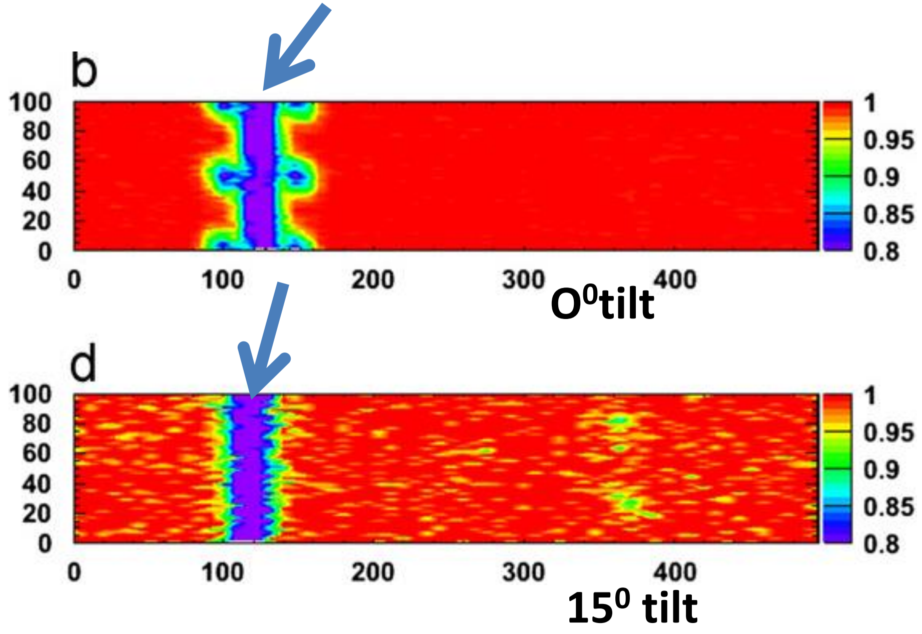




R&D issues to improve

- Bias rail loss of efficiency

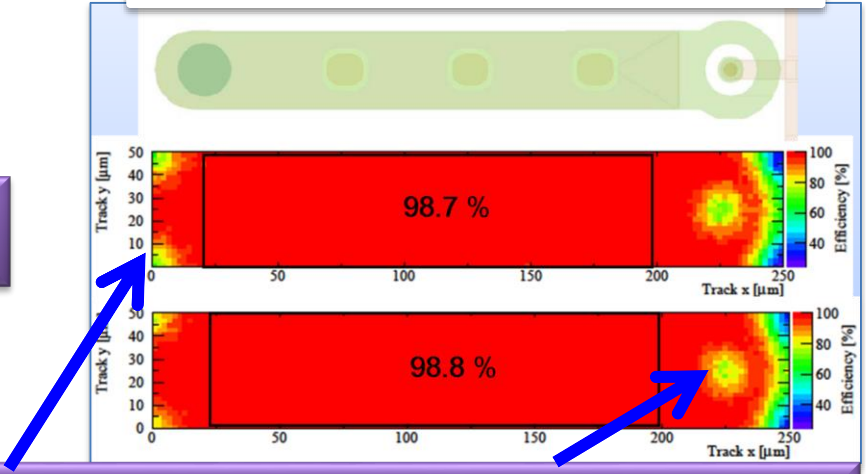
Position of polarization rail



Pixel efficiency map for the sensors irradiated to 5. 10^{15} neq/cm^2 and cooled to -15^0c.

Igor Rubinski, Nuclear Instruments and Methods in Physics Research A 699 (2013) 67–71

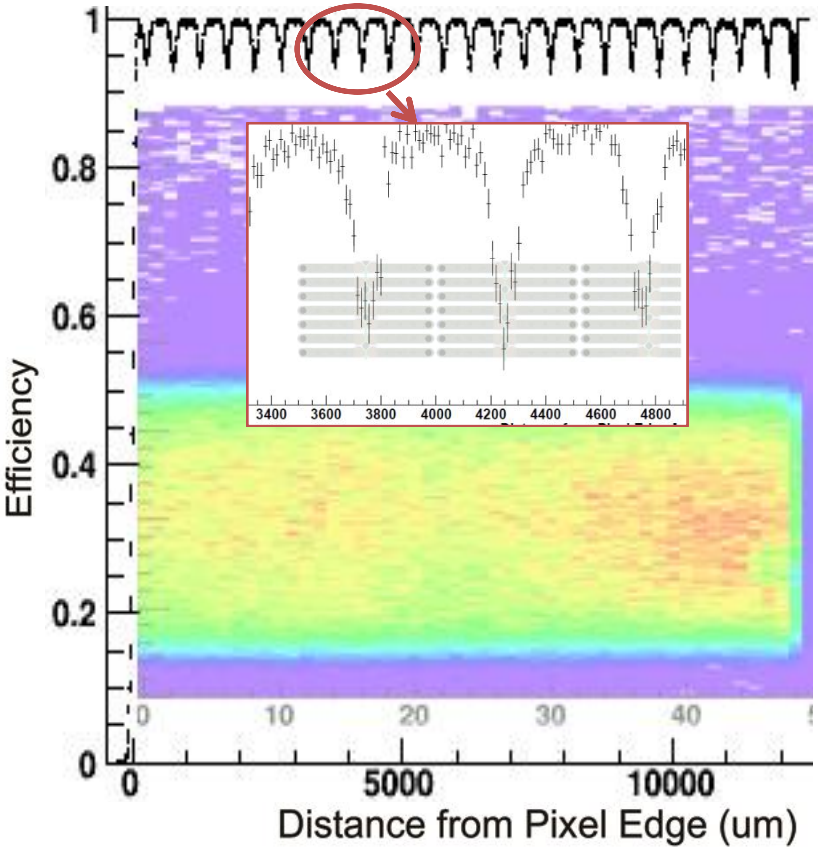
Eudet 120 GeV pions/ $\Phi=4\times10^{15}$ n_{eq} cm^{-2}

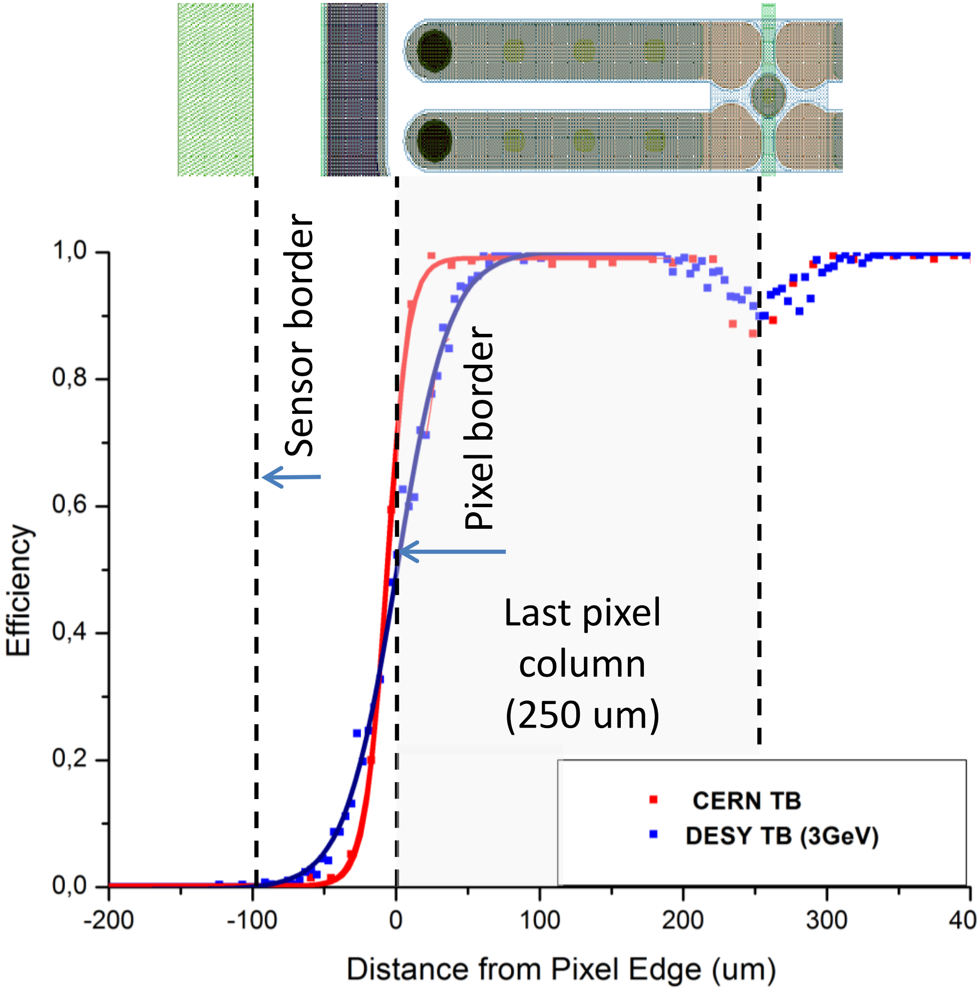


Loss of efficiency around bias dots

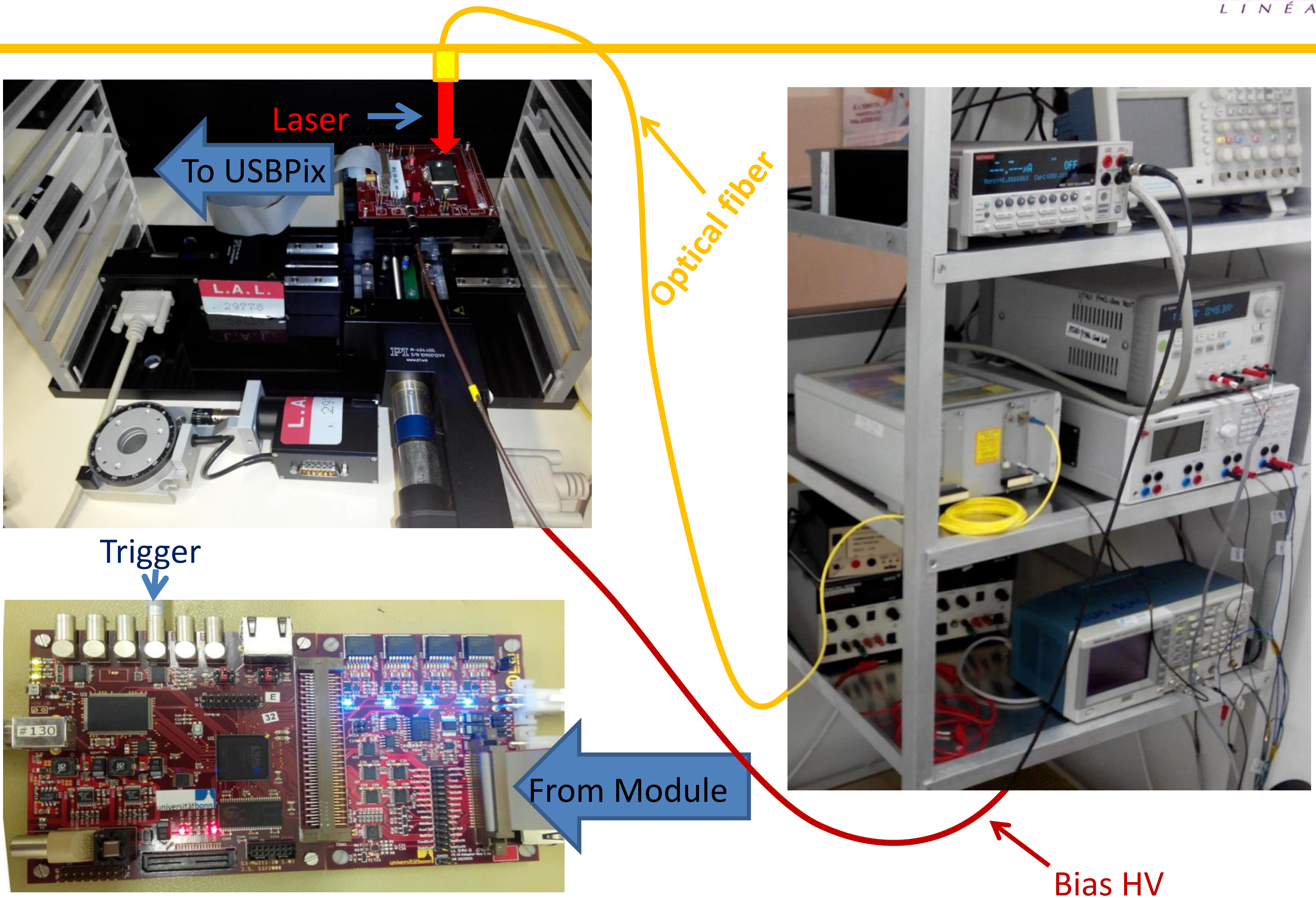
Bias rail profile

- *Efficiency vs track impact position DUT#22*





Laser test bench setup



Laser

To USBPix

Optical fiber

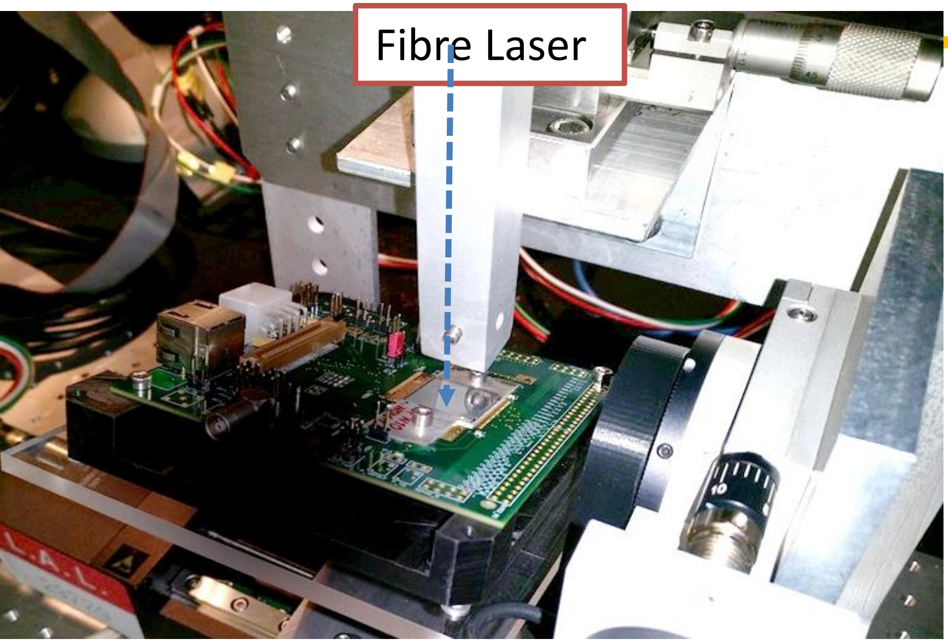
Trigger

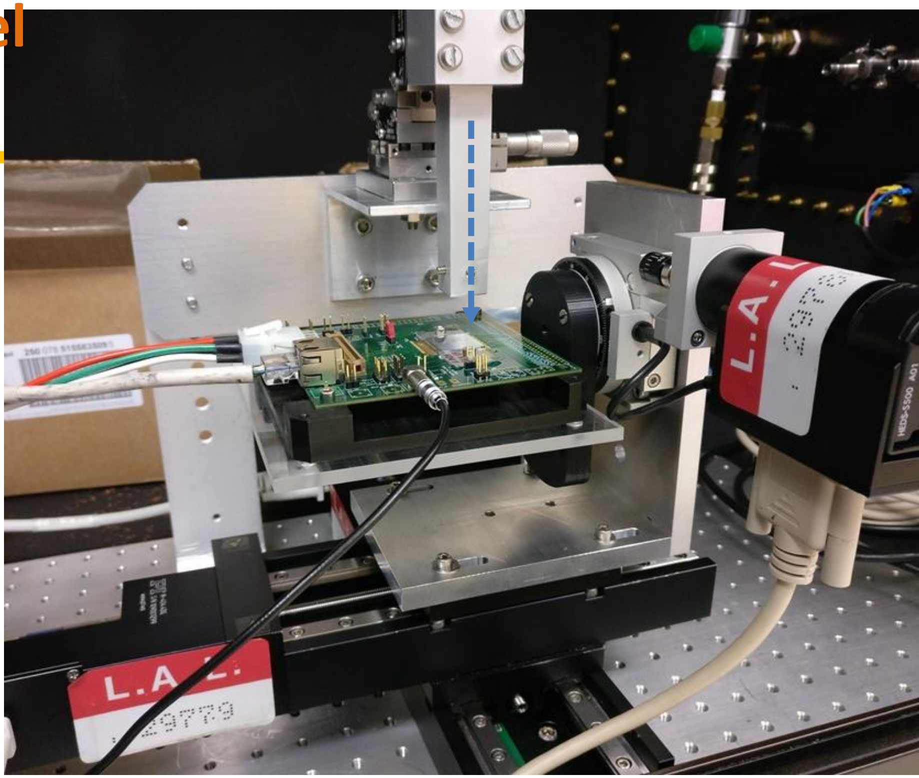
From Module

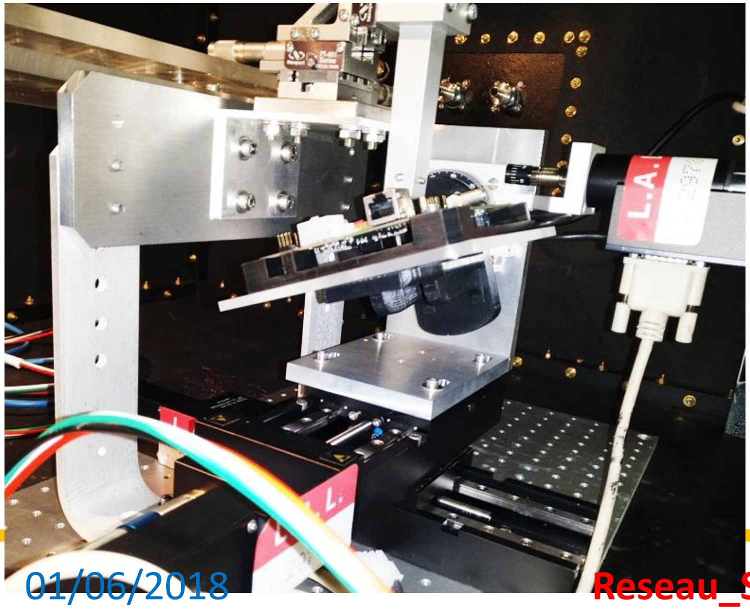
Bias HV

USBPix system

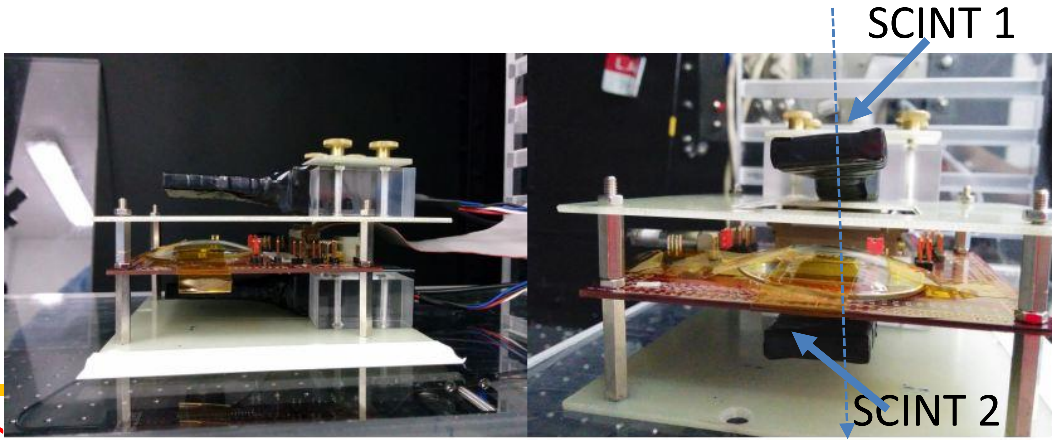
Clean room infrastructure for Pixel



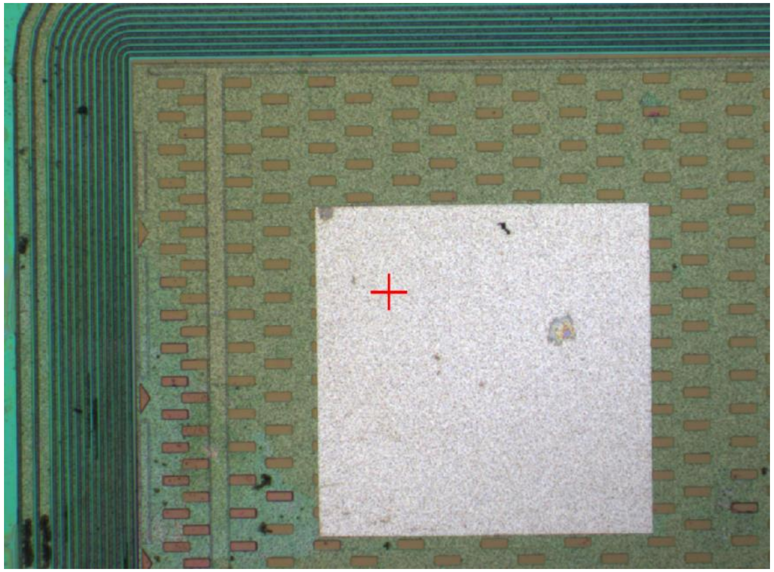


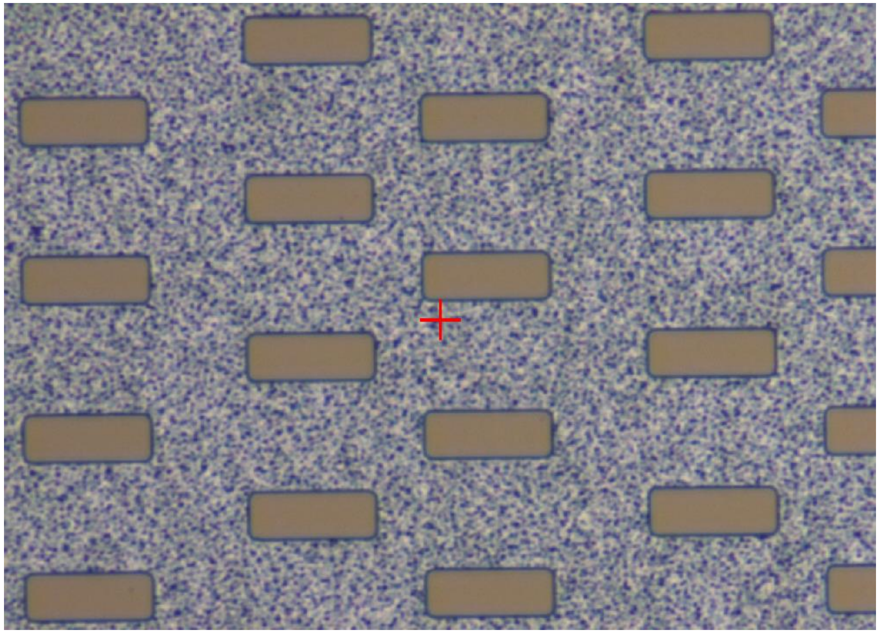


- Laser and cosmic test bench



Openings





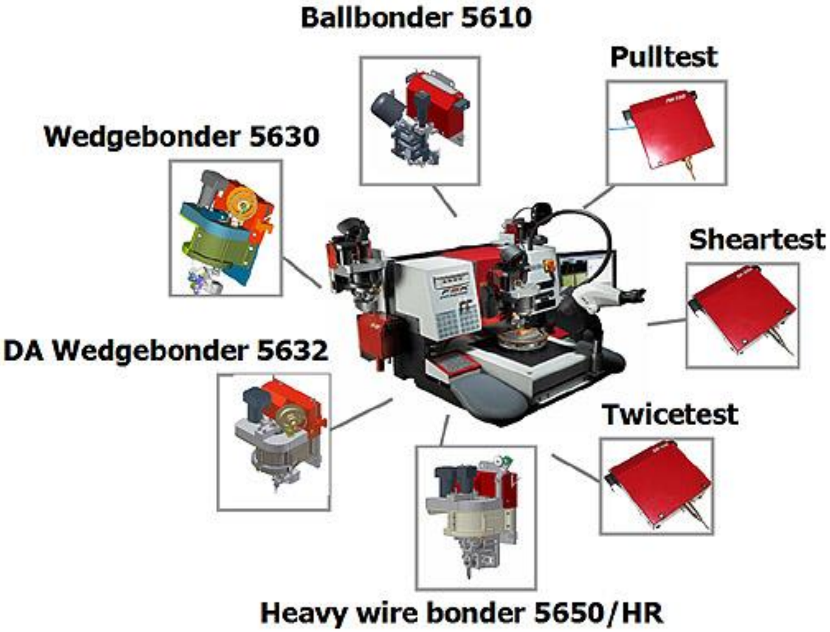
The openings in Al layer

Test infrastructure for Si Pixel characterization

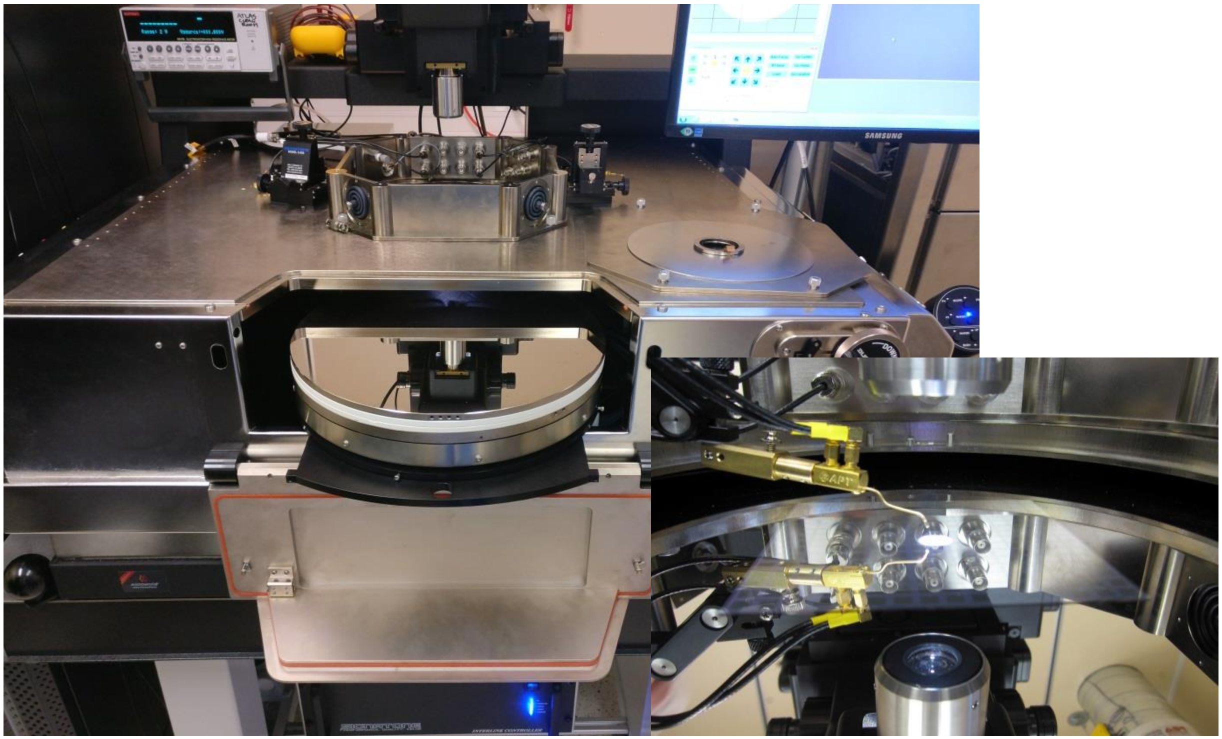
CAPTINOV Plateform based in LAL Orsay based on Probe station and Wire bonding machine in CEA IRFU

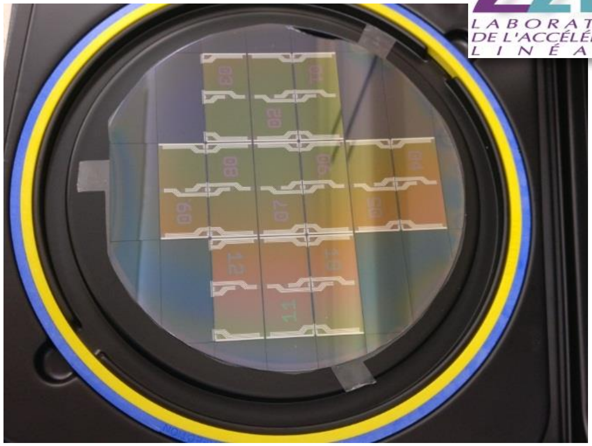
CAPTINOV

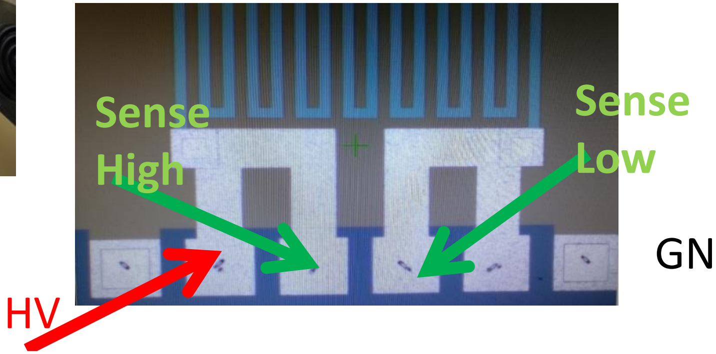
SEMI AUTOMATIC PROBE STATION

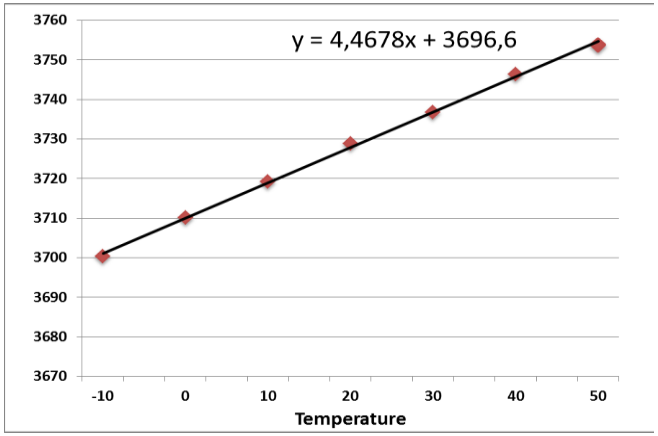


Universal Semi-Automatic Wire Bonders

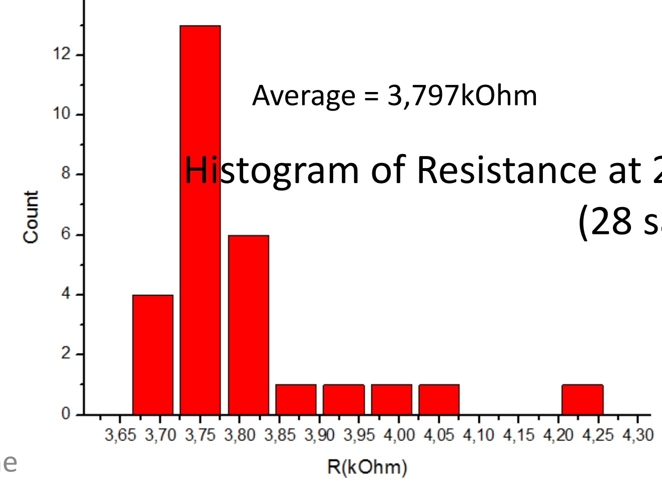








Resistance vs Temperature

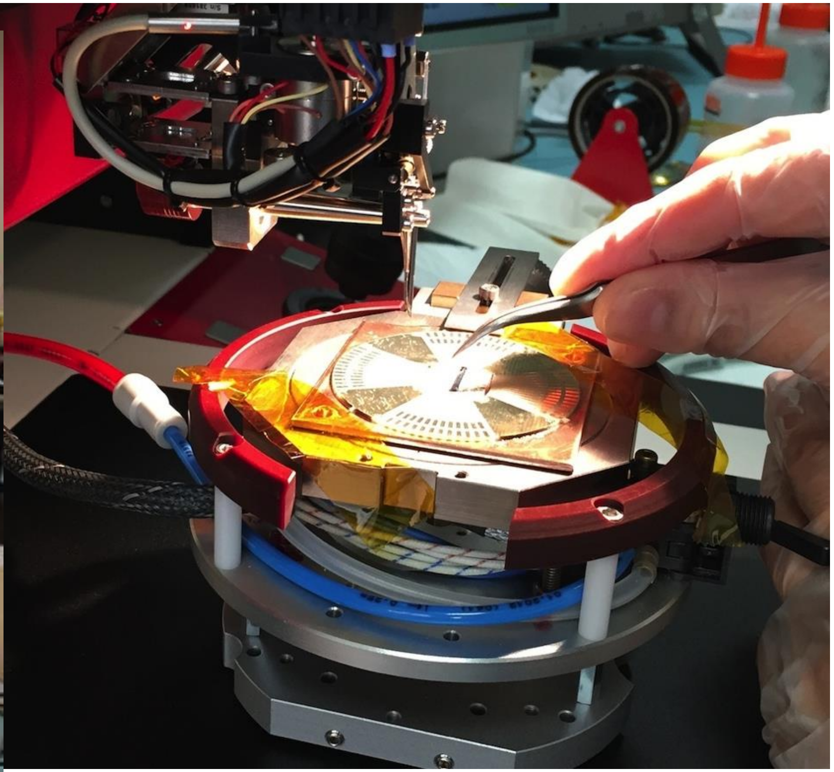


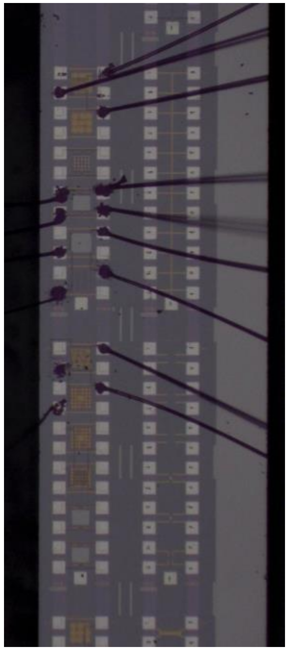
Average = 3,797kOhm

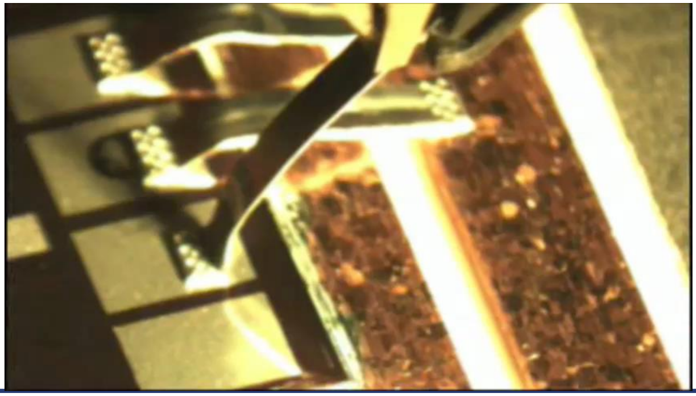
Histogram of Resistance at 20°C (28 samples)

Bonding Machine

- Machine inside the P2IO CAPTINOV Plateforme



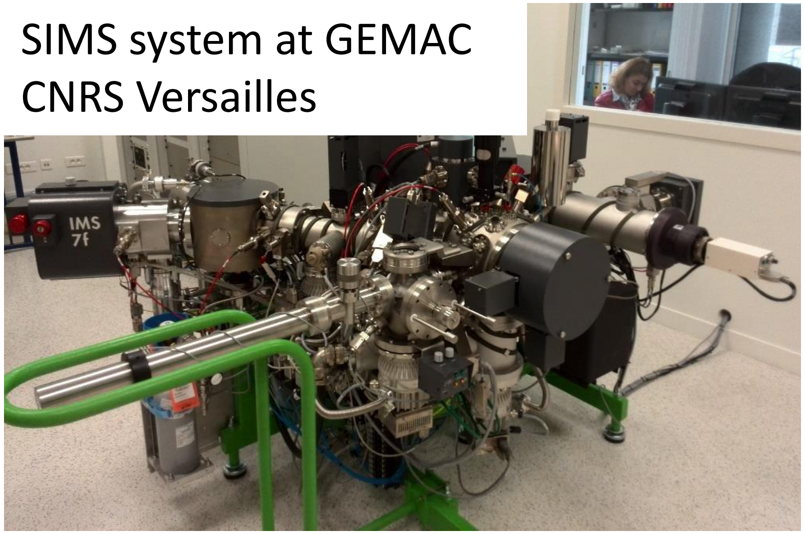




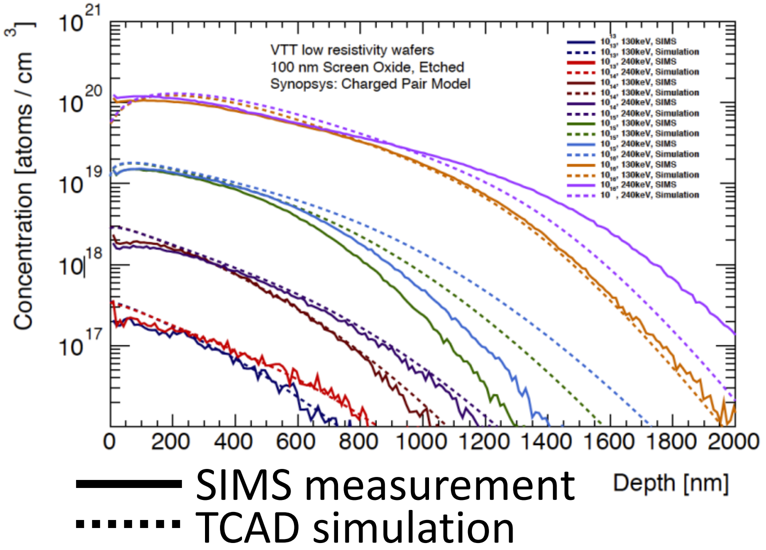
IRFU

Doping profile analysis and TCAD simulation : Secondary Ion Mass Spectrometry

- SIMS measurement
  - Analytical technique to characterize the impurities near surface(<30um) by ionized secondary particles.
  - Good detection sensitivity for **B, P, Al, As, Ni, O, Si** etc down to 10^{13} atoms/cm^3 with 1-5nm depth resolution.
- Synopsys TCAD simulation
  - Process simulation:
    - Simulate implantation and resulting concentrations.
    - **Can compare to SIMS result.**
  - Device Simulation :
    - Simulate Electric field to understand the performance of silicon device.
    - Possible to perform simulation for charge correction of MIP signal.

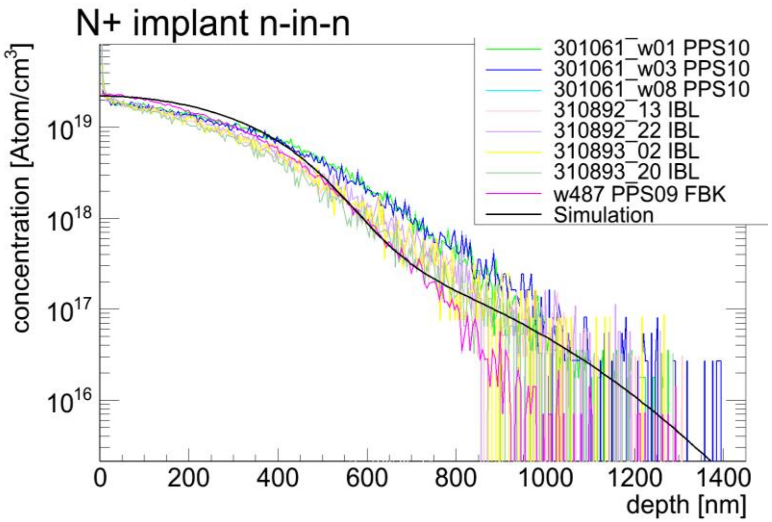


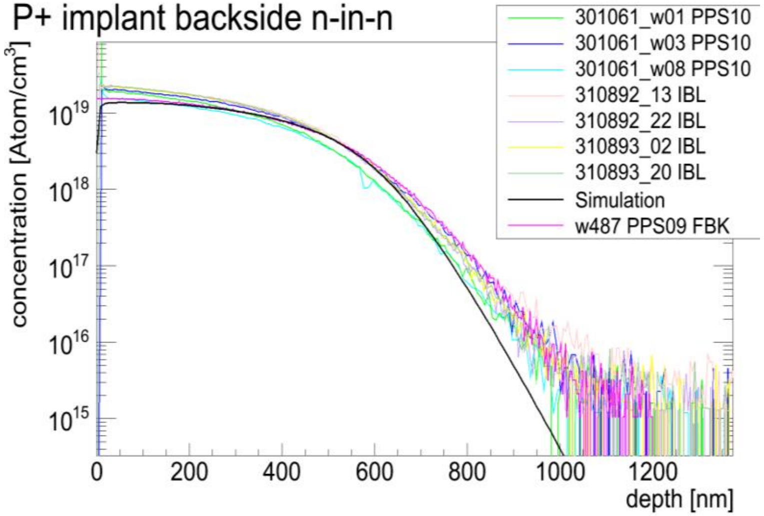
SIMS system at GEMAC
CNRS Versailles



Comparison: experimental measurements / TCAD simulations

- Optimization of implantation & annealing parameters:
  - energy and dose, oxide thickness, annealing time and temperature



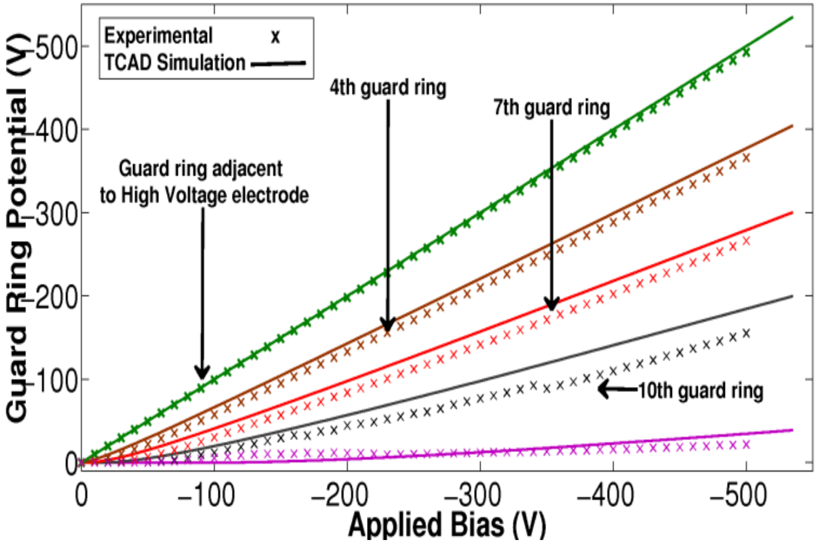


- Optimization of geometrical and structural characteristics of GR's:
  - number & width, gap size, metal overhang width

Phd Thesis, Mathieu Benoit, Now Uni. Geneve

Phd thesis, Evangelos Gkougkoussis, Now IFAE Barcelona & CERN

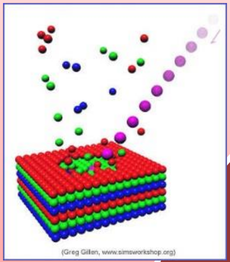
PhD thesis, Tasneem Rachid, LAL



Strategy : R&D Contributions for pixels développement for ATLAS HL-LHC

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

- SIMS (CNRS-U. Versailles GEMAC)
- AFM (IEF ORSAY)
- SPR


(Greg Gillen, www.simsworkshop.org)

Partenariats Académiques

- **Doping profiles and TCAD simulations of ATLAS planar pixel sensors for HL-LHC**

PROFILS DE DOPAGES

Comprendre la structure des pixels

- SYNOPSIS 3D
- SILVACO

Analyse et Prédictions comportements des systèmes

Technology Computed Aided Design

Simuler

Partenariats Industriels
- MPI-CiS Institut für Mikrosensorik gGmbH (Erfurt, Germany) ,
- LETI Grenoble, France
- VTT Technical Research Center of Finland,

Valider

CHARACTERISATION

SALLE BLANCHE

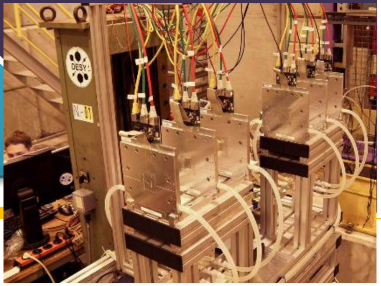
FAISCEAUX TESTS AU CERN

Produire

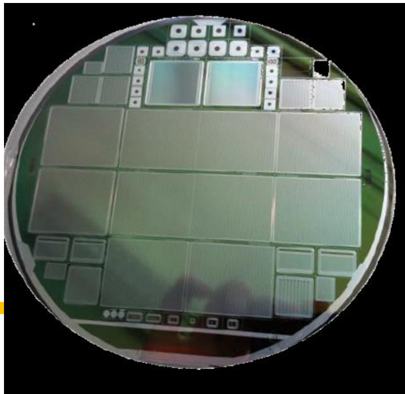
Optimiser les Zones d'efficacité

- Performances
- Tests en faisceaux
- Irradiations

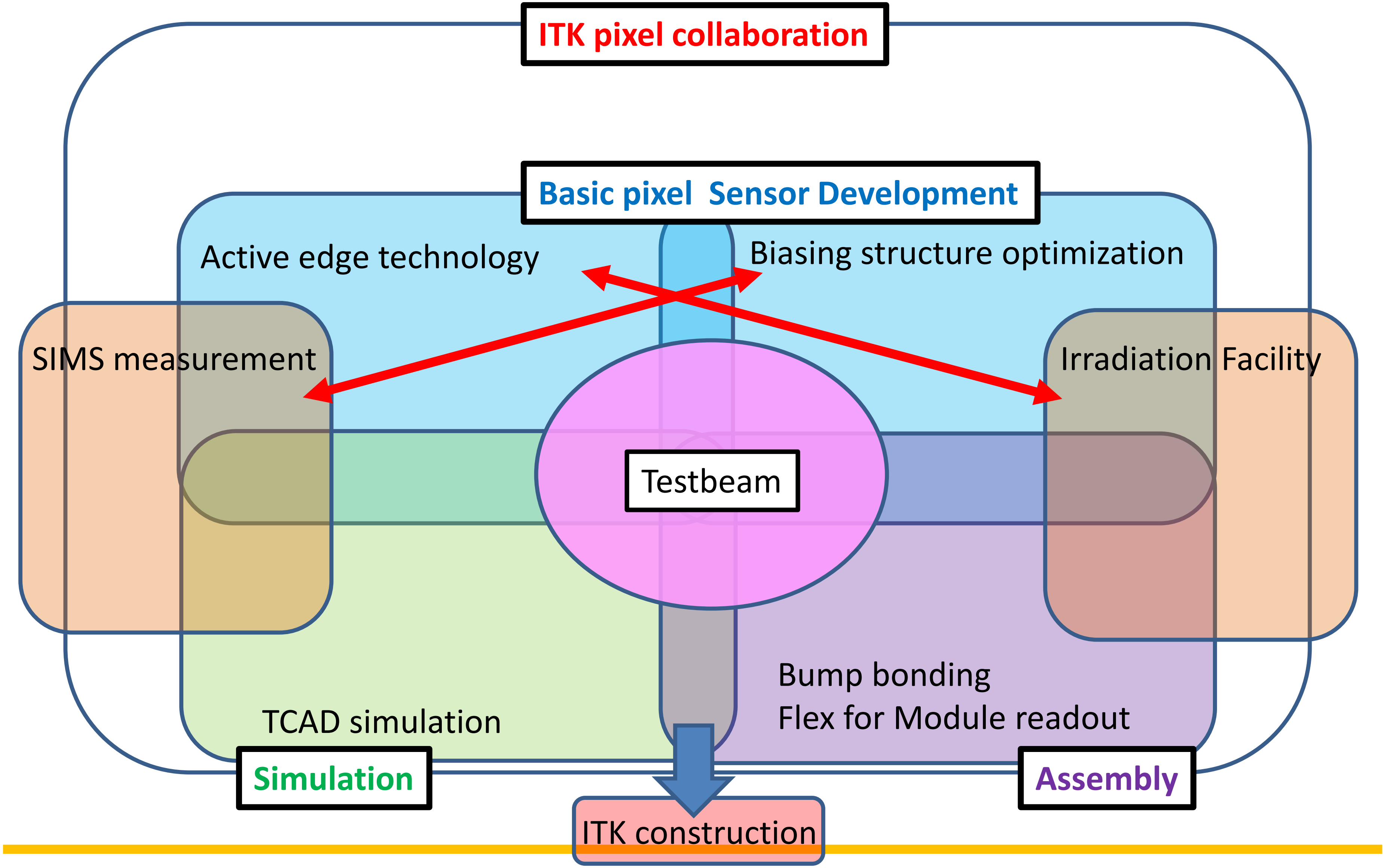
CERN, Genève
DESY Hambourg,
PSI, Zurich
Karlsruhe,



- CONCEPTS INNOVATION PIXEL



Overall R&D items for Tracker construction



ITK pixel collaboration

Basic pixel Sensor Development

Active edge technology

Biasing structure optimization

SIMS measurement

Irradiation Facility

Testbeam

Bump bonding

Flex for Module readout

TCAD simulation

Simulation

Assembly

ITK construction

Conclusions

- **Our group is committed in an ambitious R&D program inside the ATLAS ITK effort for HL-LHC, where we will face challenging issues:**

  We developed an efficient strategy for the major issue to Built an innovative granular thin pixel planar detector.

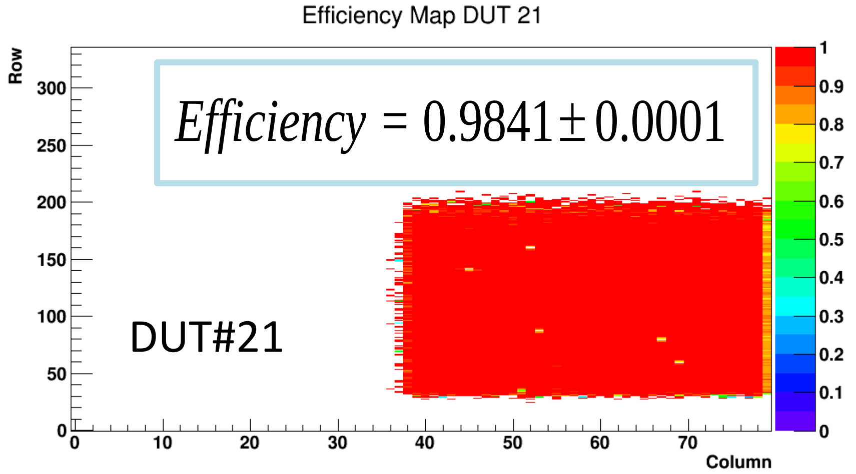
  - Find the best sensor layout ingredients for high charge collection efficiency.
  - Explore productions with active edge and optimized biasing structure which will exhibit the best performance.
  - Develop robust radiation hard solutions to cope with HL-LHC irradiation fluences.

- **Thus our aim is to enhance our expertise to built the future P bulk Planar Pixel Sensors for ATLAS tracker for HL-LHC. We intend to get more expertise in terms of:**
  - P bulk sensor design, characterization and testing (Clean room, Test-Beam, irradiation facility)
  - Understand the behavior of heavily irradiated Planar Pixel Sensors
  - increase expertise and efforts (TCAD simulation, SIMS, Irradiation etc…)
  - Improve our relations with industrial foundries (sensor design, production, bump bonding)
  - Accelerate educational level of young people (Masters, Phd Programs)

Efficiency map

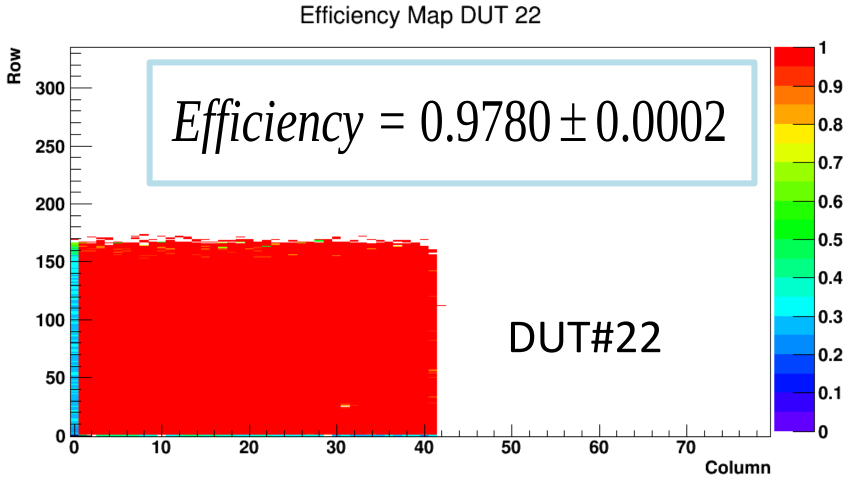
- *Overall sensor efficiency*

$$Efficiency = \frac{Number\ of\ Matched\ Tracks}{Number\ of\ Total\ Tracks}$$


Efficiency Map DUT 21

$$Efficiency = 0.9841 \pm 0.0001$$

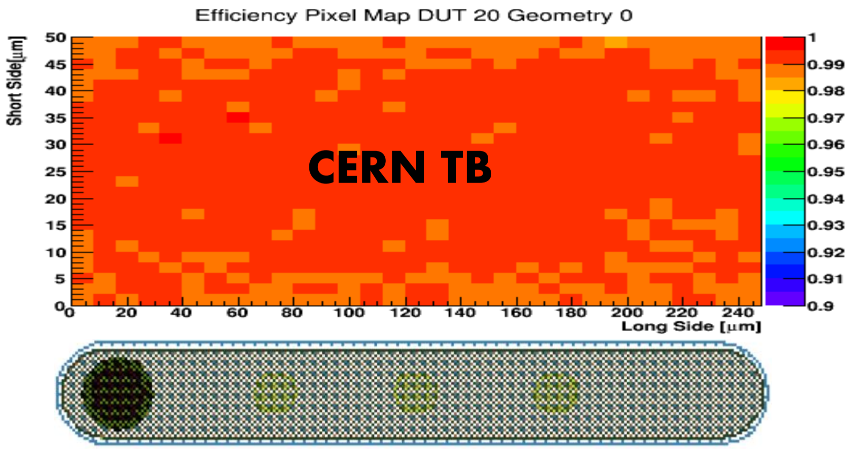
DUT#21


Efficiency Map DUT 22

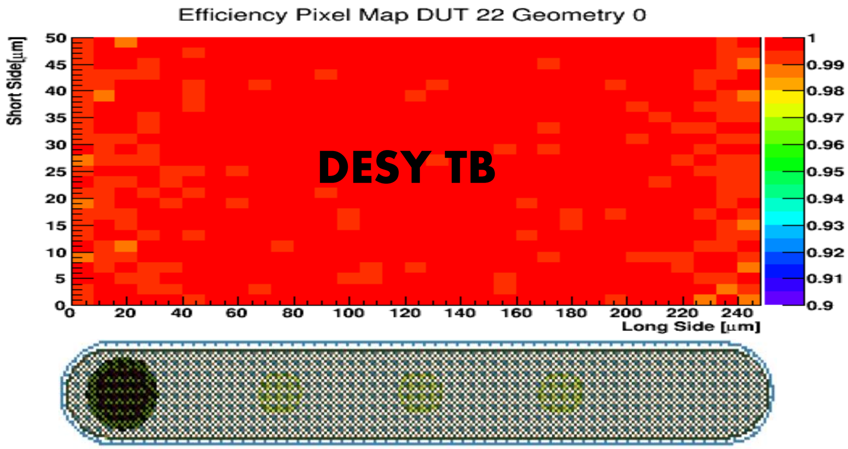
$$Efficiency = 0.9780 \pm 0.0002$$

DUT#22

- *In-pixel efficiency map* (active edge DUT#22)


Efficiency Pixel Map DUT 20 Geometry 0

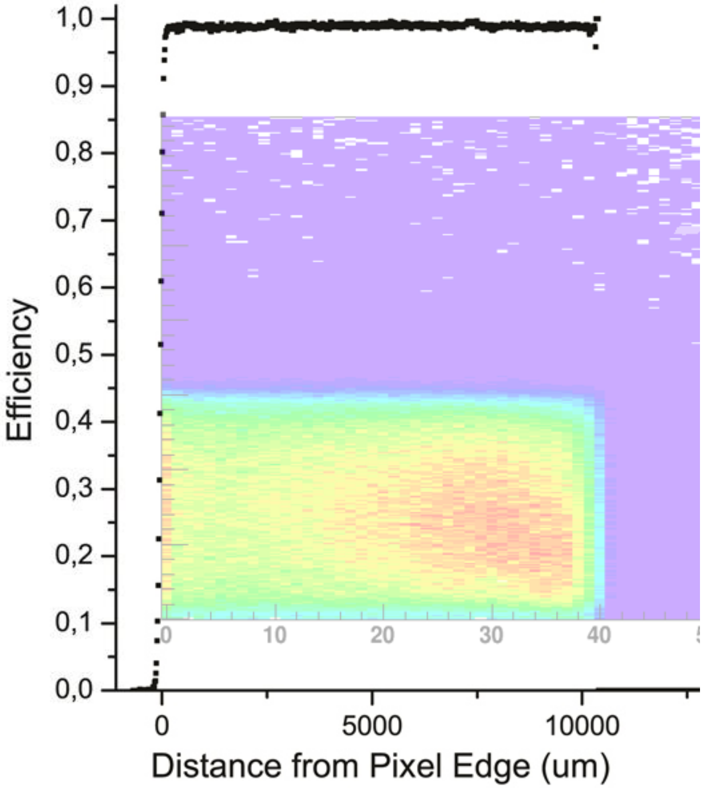
CERN TB

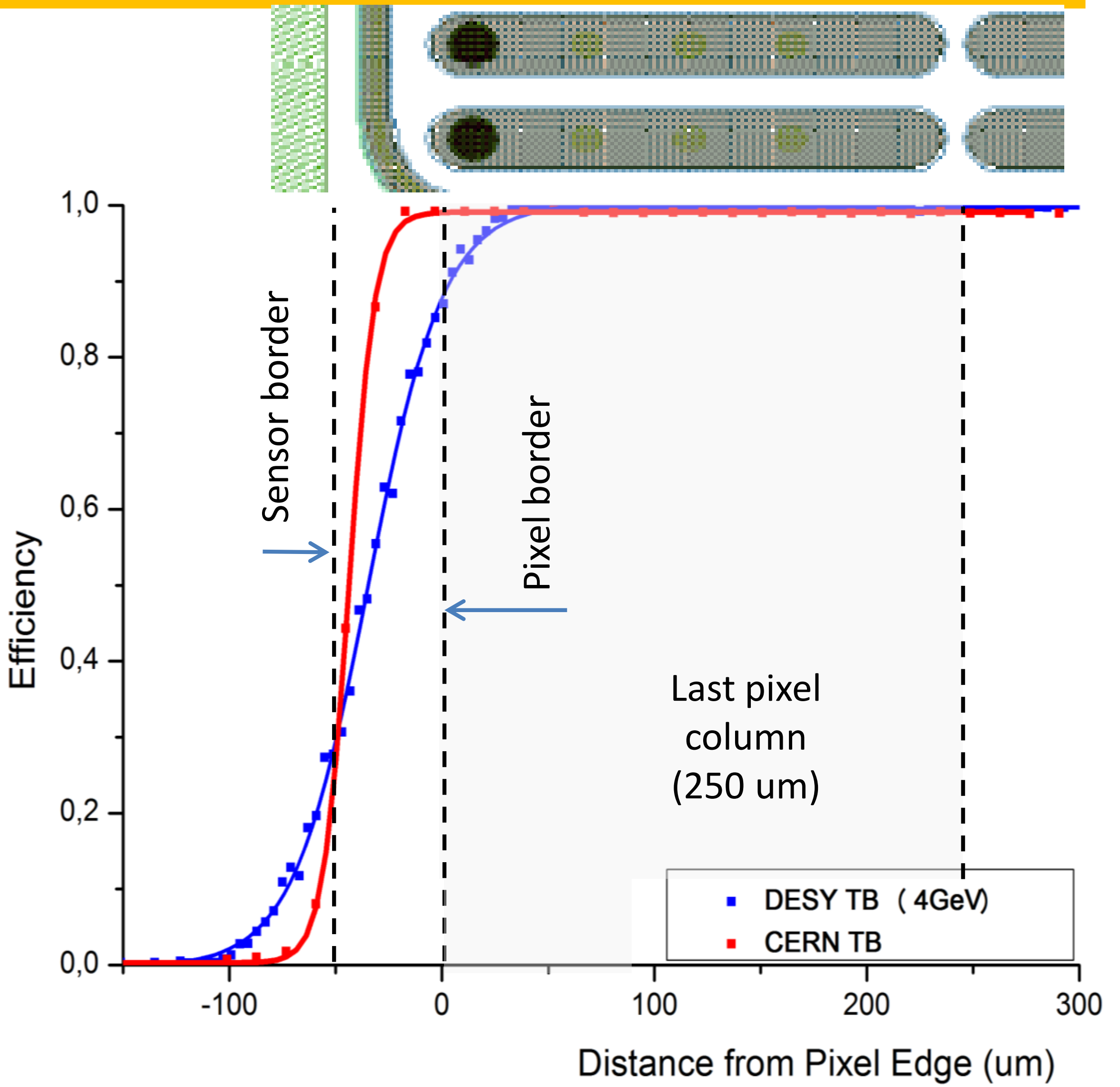

Efficiency Pixel Map DUT 22 Geometry 0

DESY TB

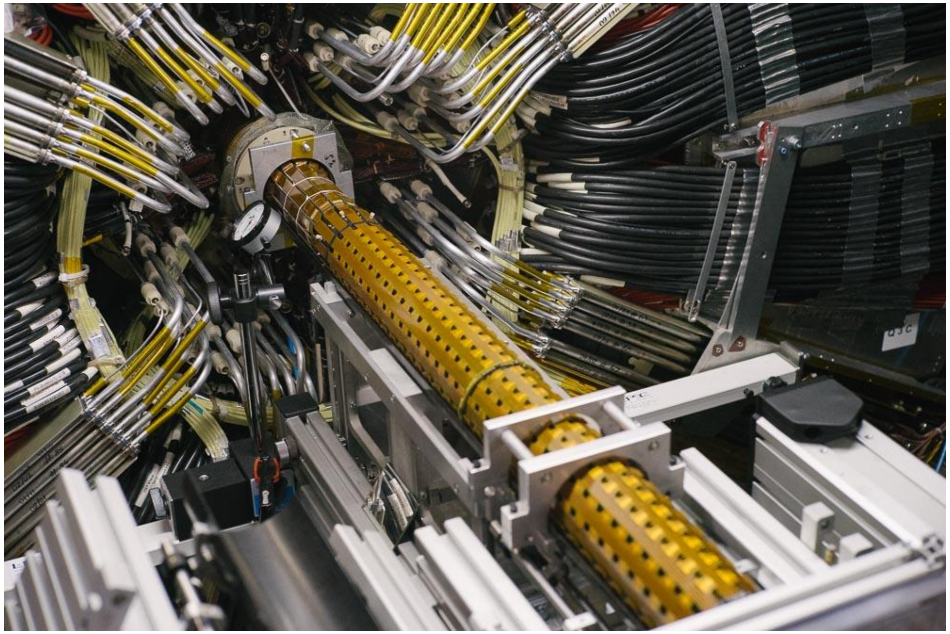
Results – batch 3

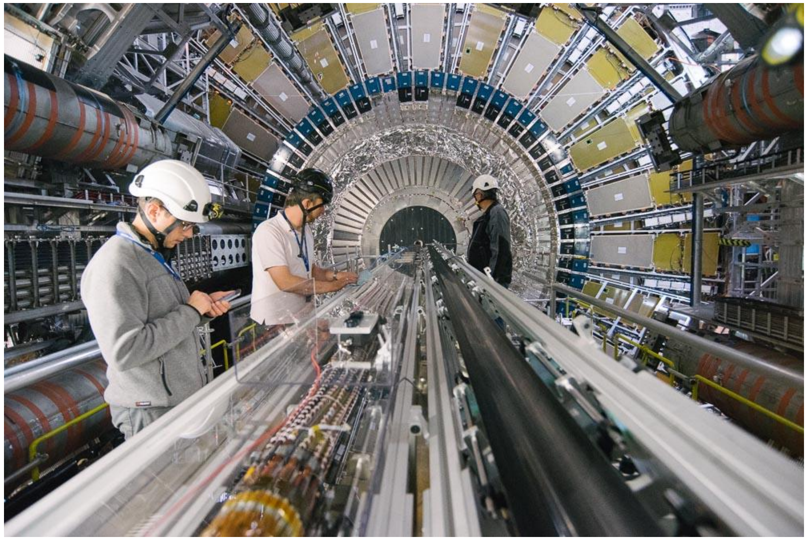
- *Efficiency vs track impact position DUT#22*





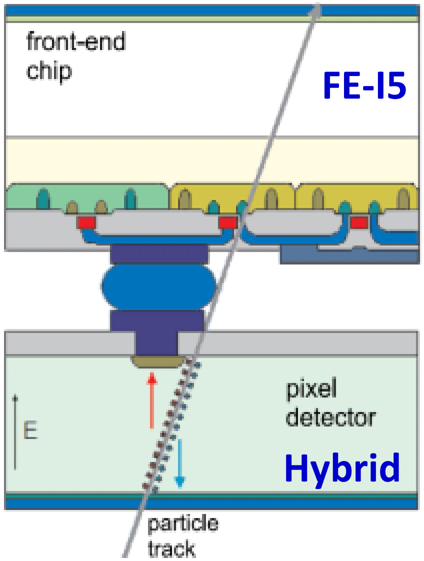
backup





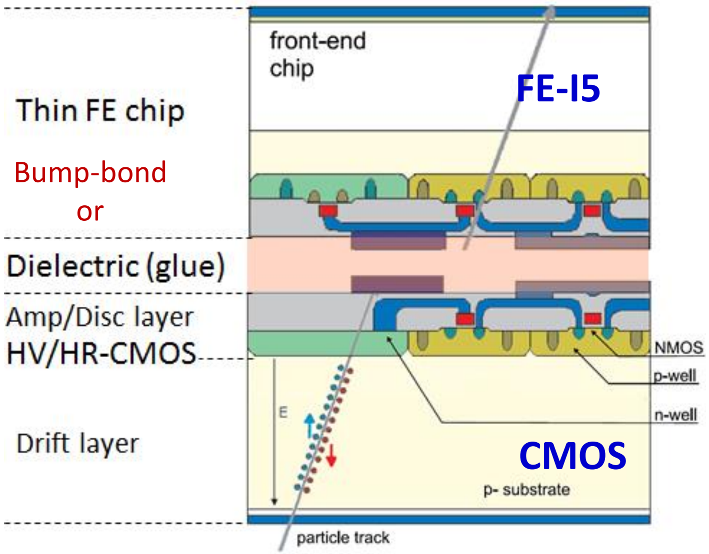
Silicon-based tracking

'Standard' Hybrid Pixels + FE-I5



- Rad hardness
- Fast readout
- Thick, Low granularity
- High Cost

HV-(HR)CMOS + FE-I5


Thin FE chip

Bump-bond
or

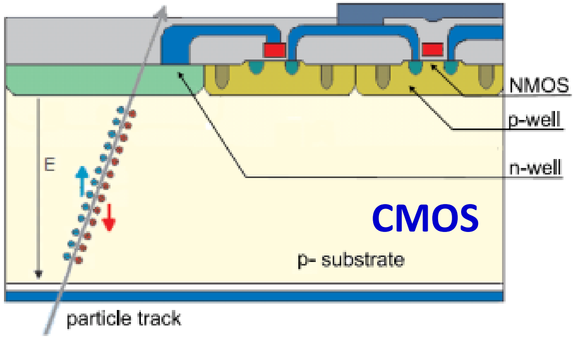
Dielectric (glue)

Amp/Disc layer
HV/HR-CMOS

Drift layer

- More granular
- Less expensive (cheaper bonding process)
- Thinner
- Low power, low noise
- Rad hardness

HV-(HR)MAPS (full monolithic)



- Highest granularity
- Thinnest (material budget ↘)
- Lower cost (intelligent detector)
- Low power, low noise
- Rad hardness, fast readout

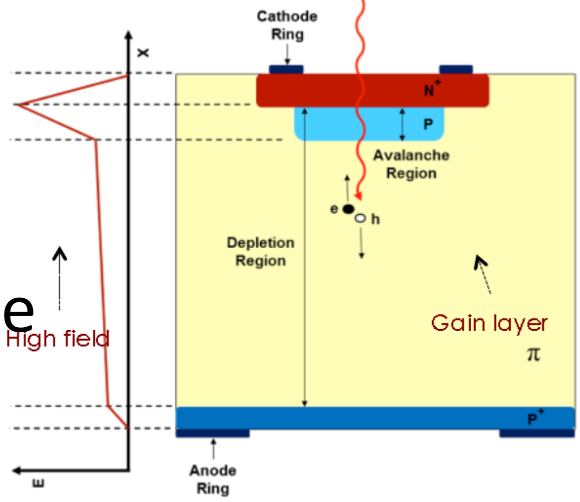
All three technologies are addressed within THINK

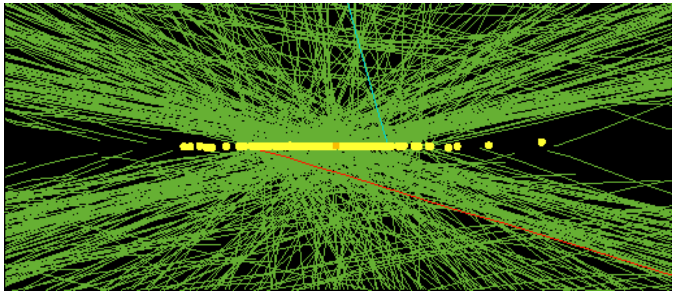
Another layer of Collaboration? : LGAD

Low Gain Avalanche Detectors

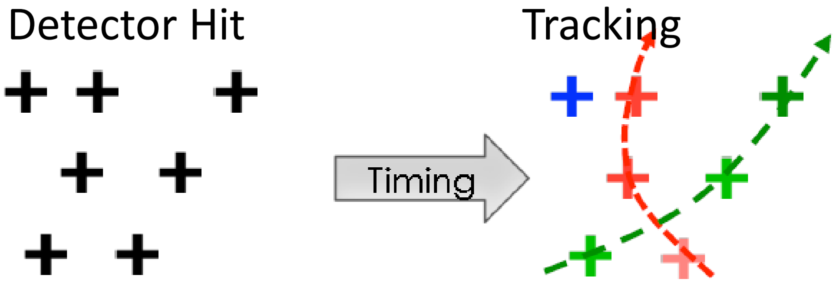
- To solve pileup issue in future high luminosity hadron collider, good time resolution detector is important.
- The **~50ps** time resolution makes it possible to identify each collision in an event.

Gain in Avalanche mode





- Time resolution
  - Smaller time walk (higher field)
  - Smaller time jitter (low noise)
- p+ layer beneath n+ implant creates ~300kV/cm electric field (Gain ~ 10)



CNM/FBK/HPK produced devices

- **LAL group : Simulation&Testing CNM device**
- **Tsukuba group : Testing HPK device**