

# **Studies for the Phase-2 ATLAS ITk pixel upgrade**

Shohei Shirabe

# Brief self-introduction

- Kyushu University



- Summer 2013: MEG Experiment @ PSI
- 2013-2014: muon g-2/EDM Experiment @ J-PARC
- 2015 - : ATLAS @ CERN
  - SCT Operation
  - Displaced heavy neutral lepton analysis

- Tokyo Institute of Technology, University of Geneva

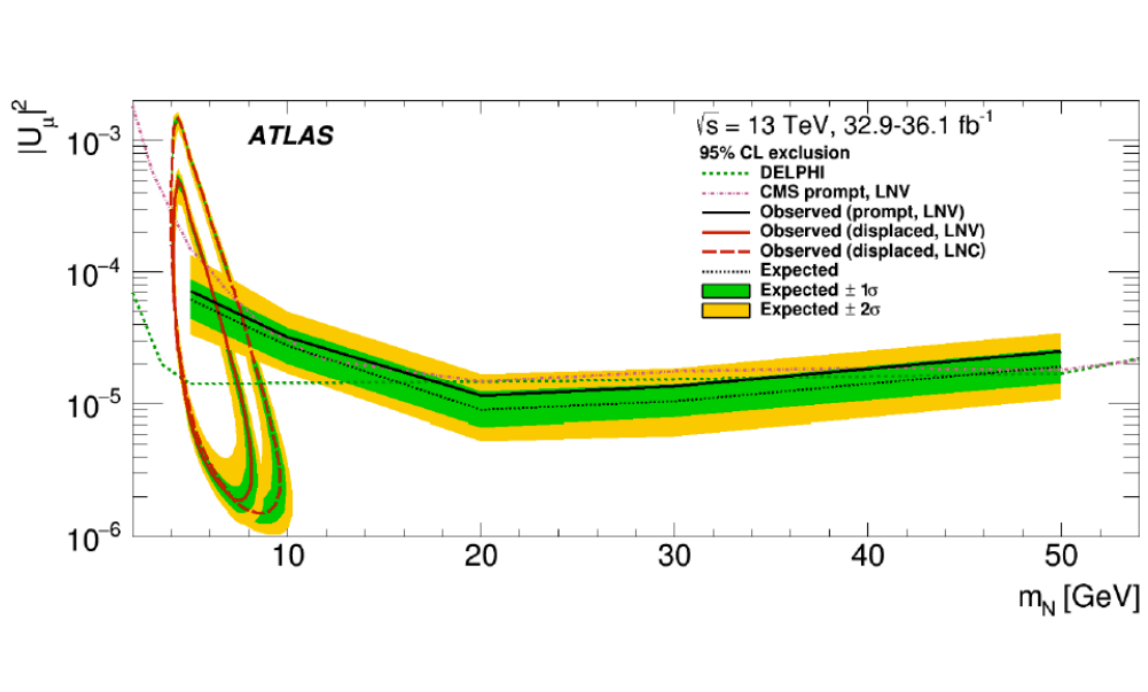
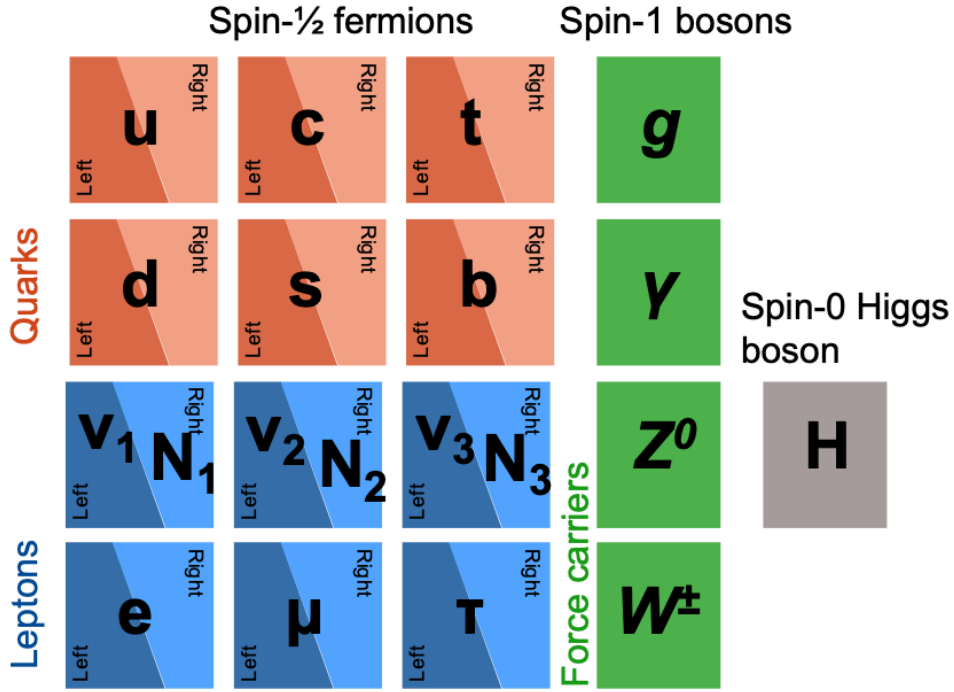
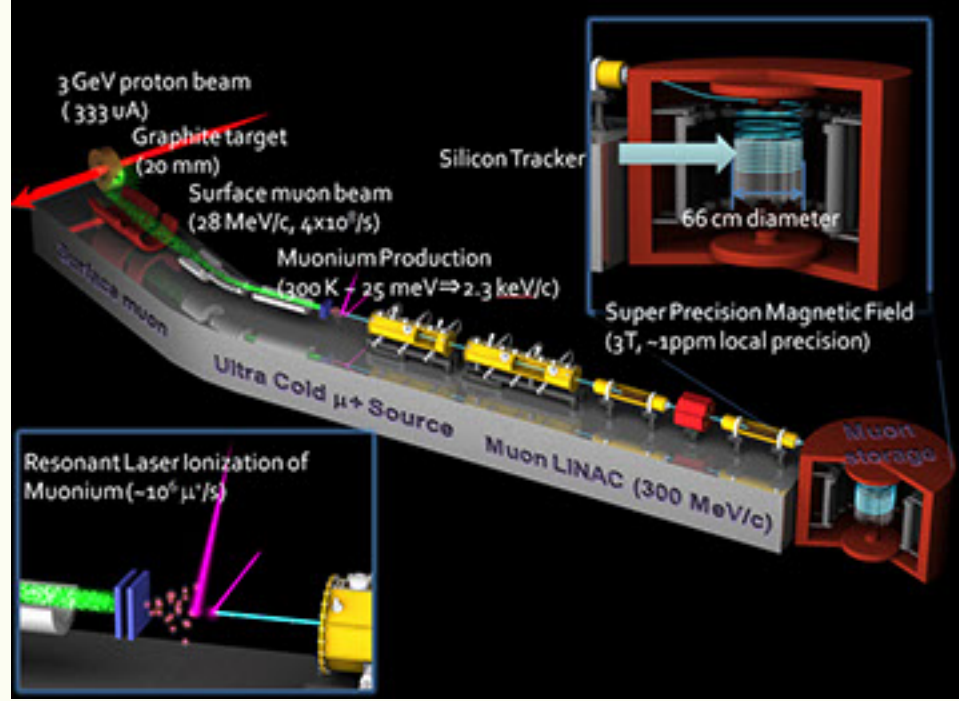
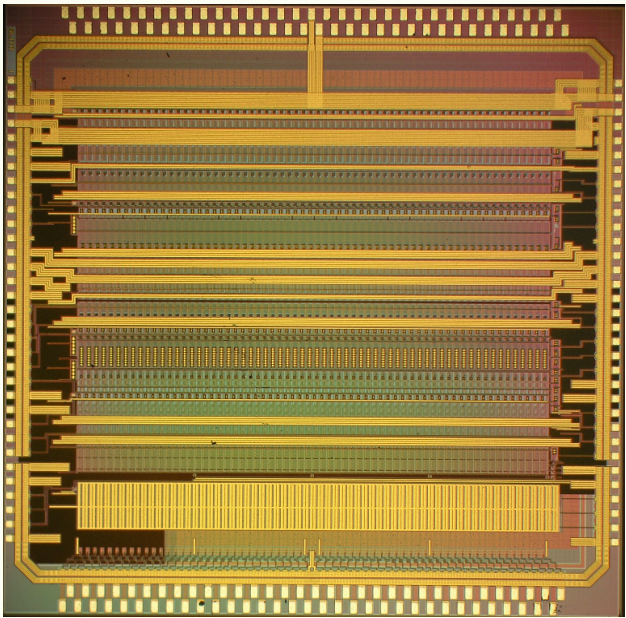
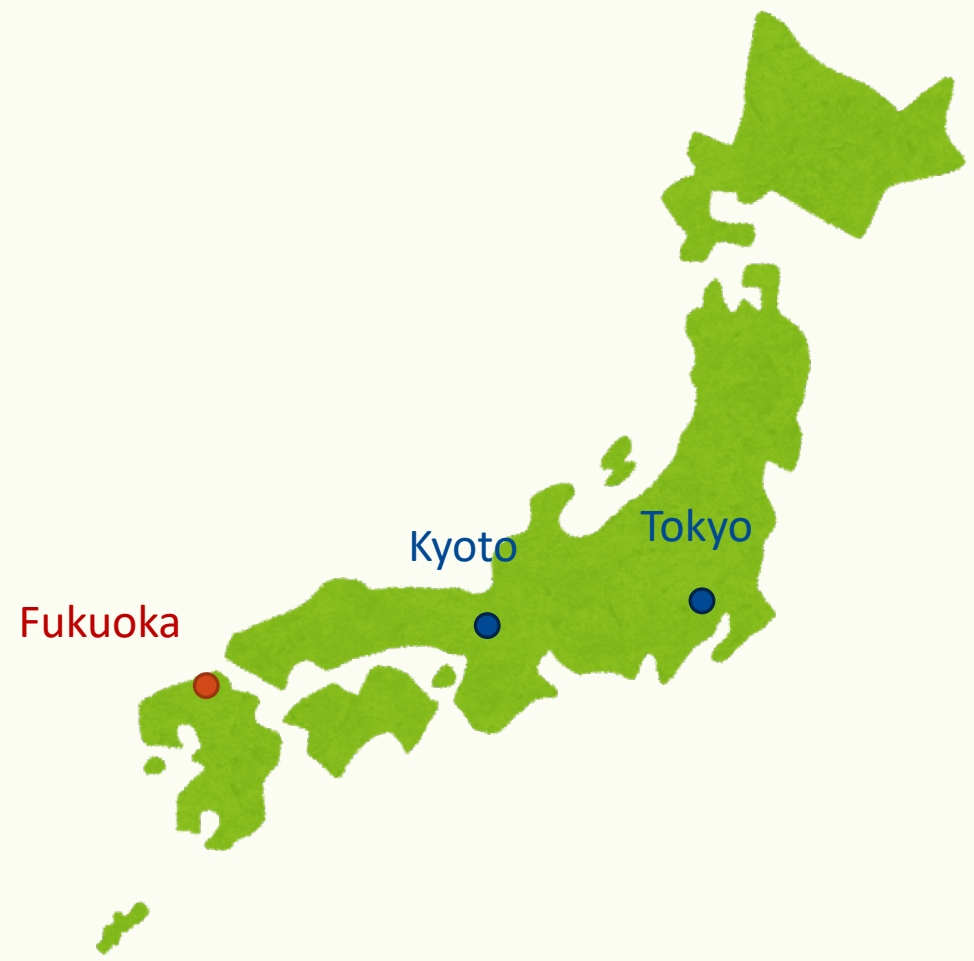
- 2019 - : ATLAS @ CERN
  - ITk Upgrade



- LPSC



- 2022 - 2023 : ITk Upgrade

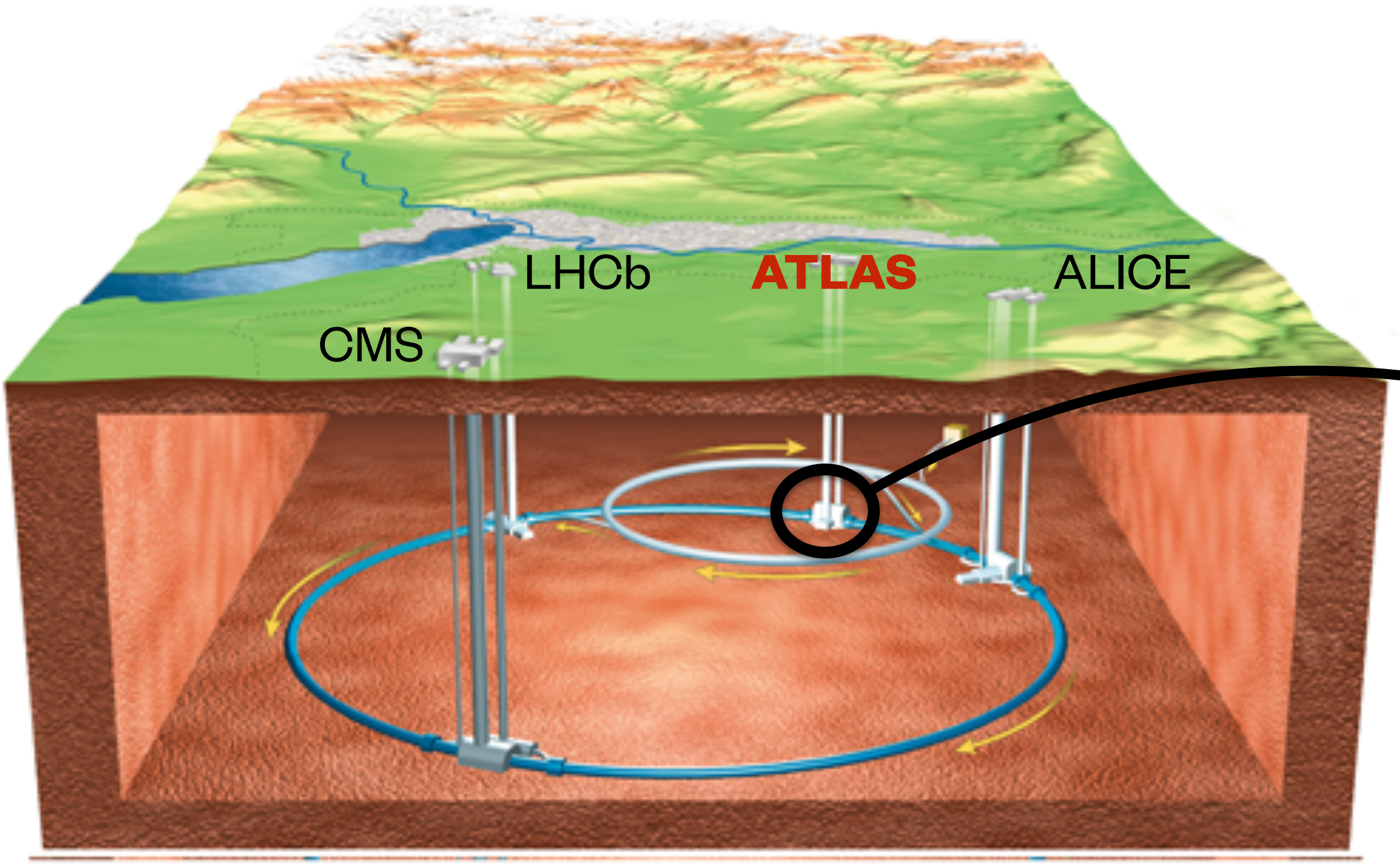




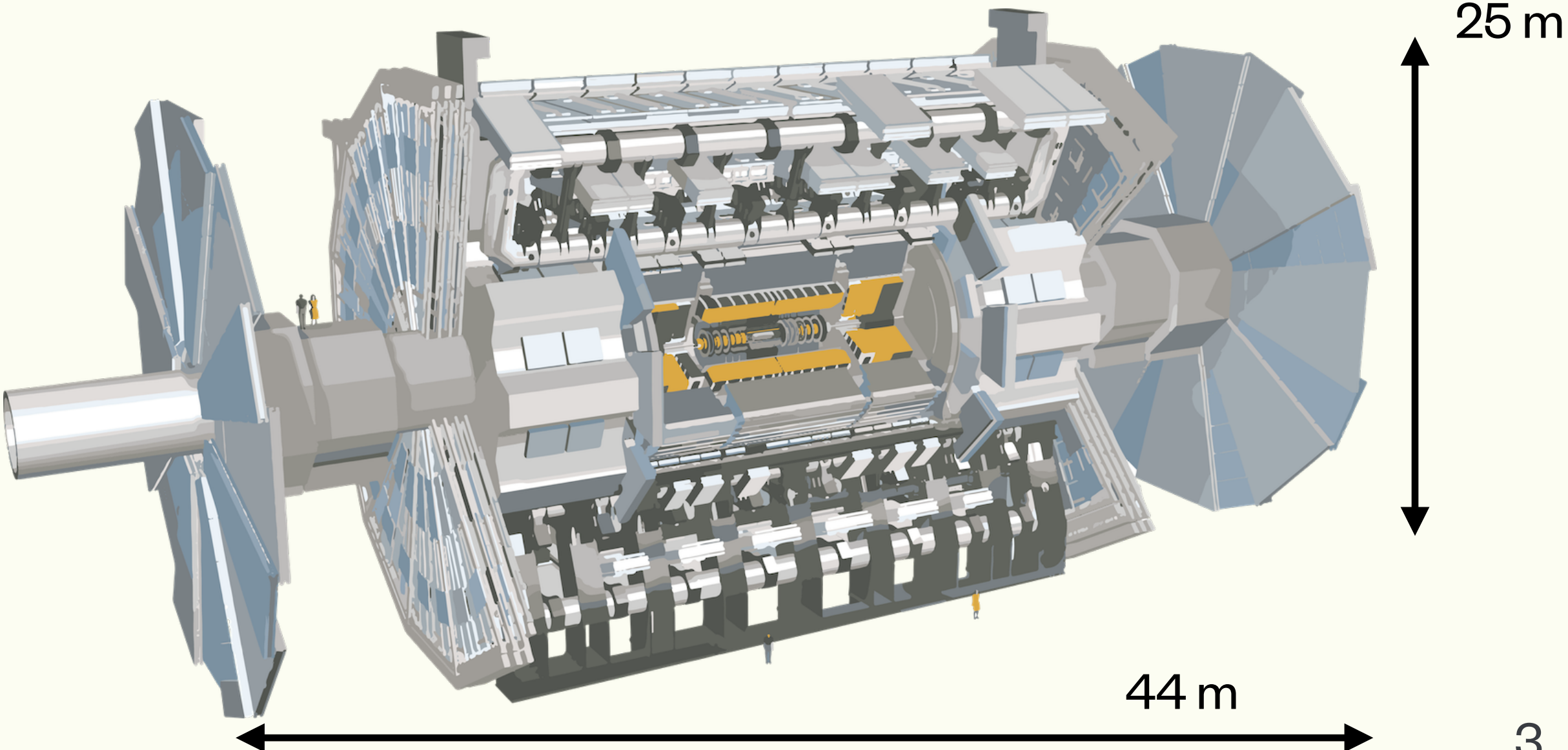
# LHC and ATLAS

## LHC

- 2008 - 2025
- $\langle \mu \rangle \sim 30$
- $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- $400 \text{ fb}^{-1}$  ( $190 \text{ fb}^{-1}$  so far)



## ATLAS Detector



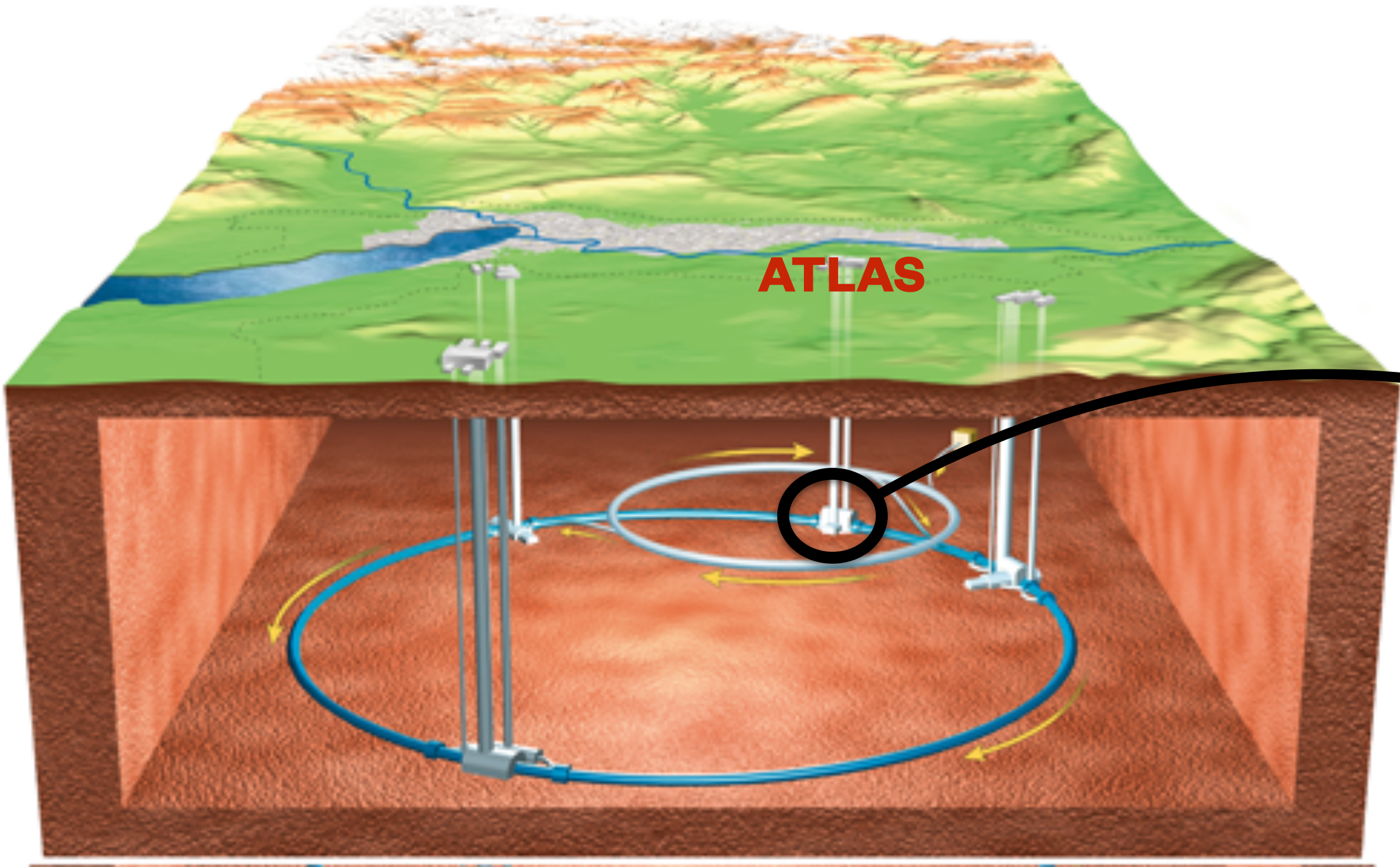
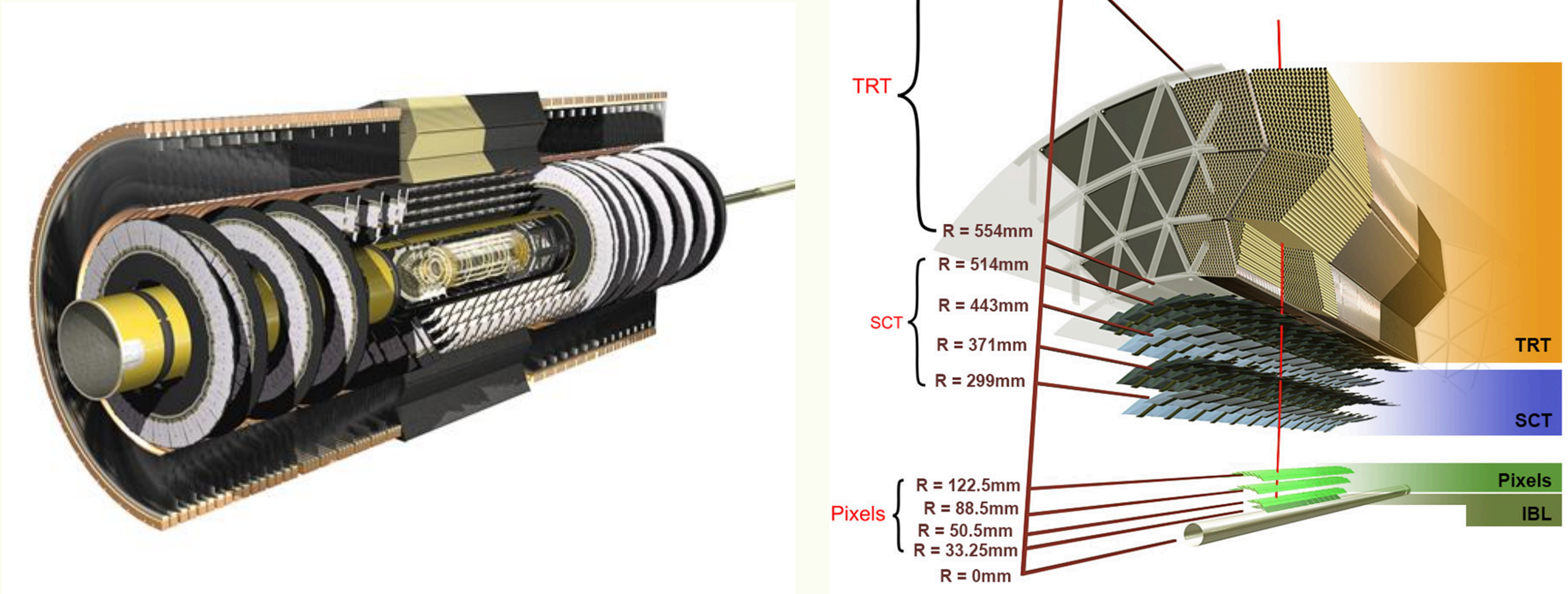


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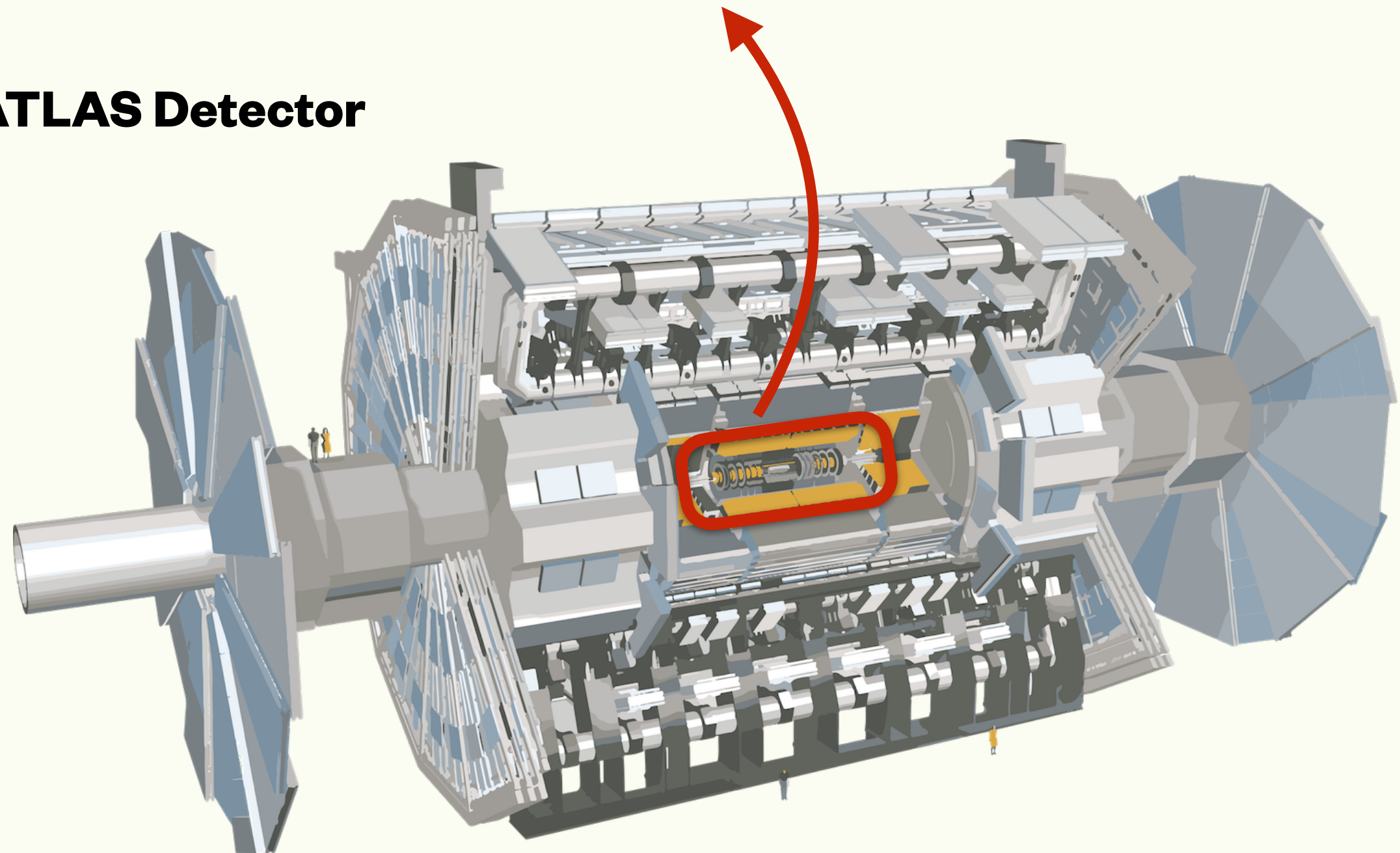
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## ATLAS "Current" Inner Detector



## ATLAS Detector





# High Luminosity LHC

**LHC**

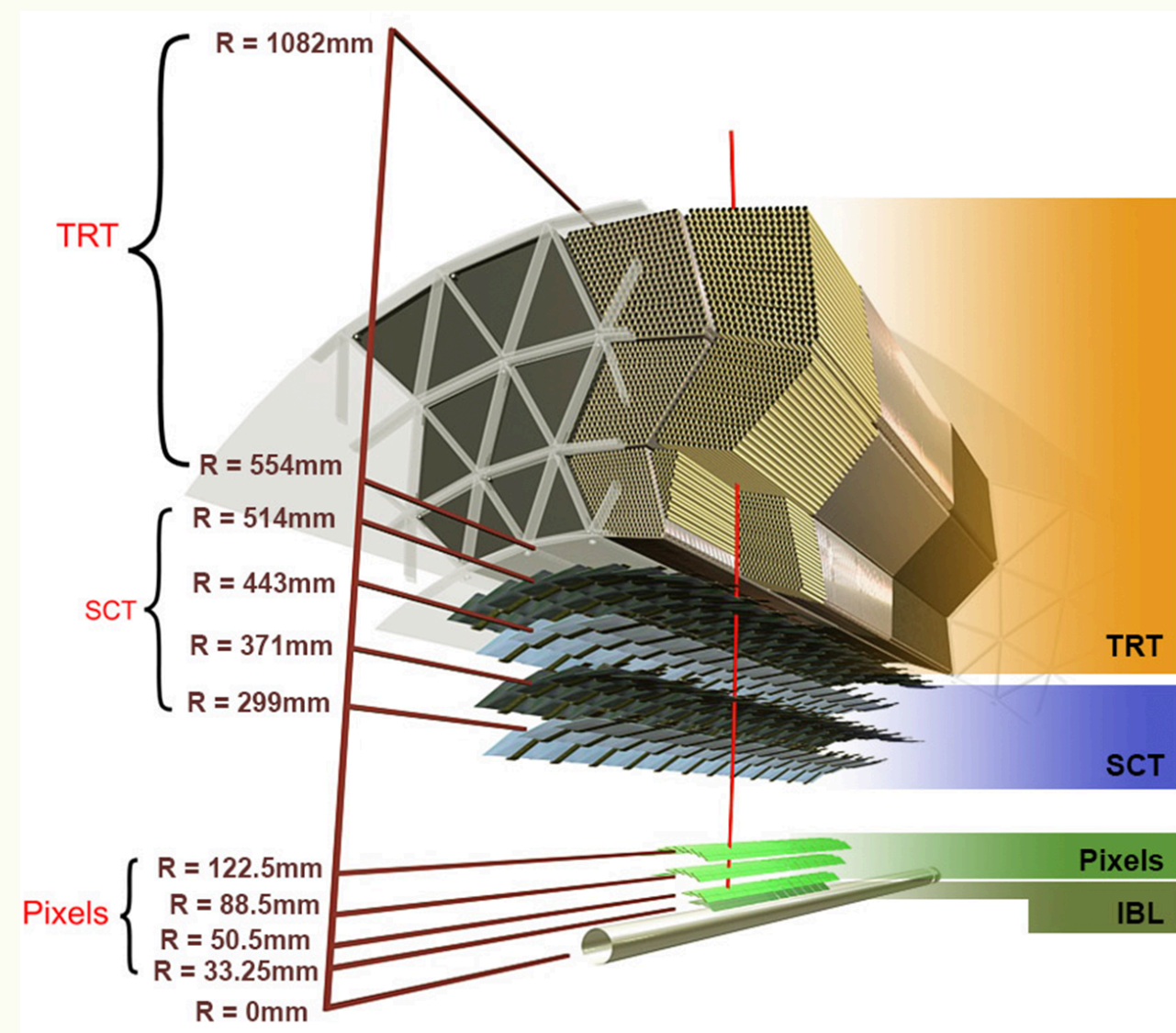
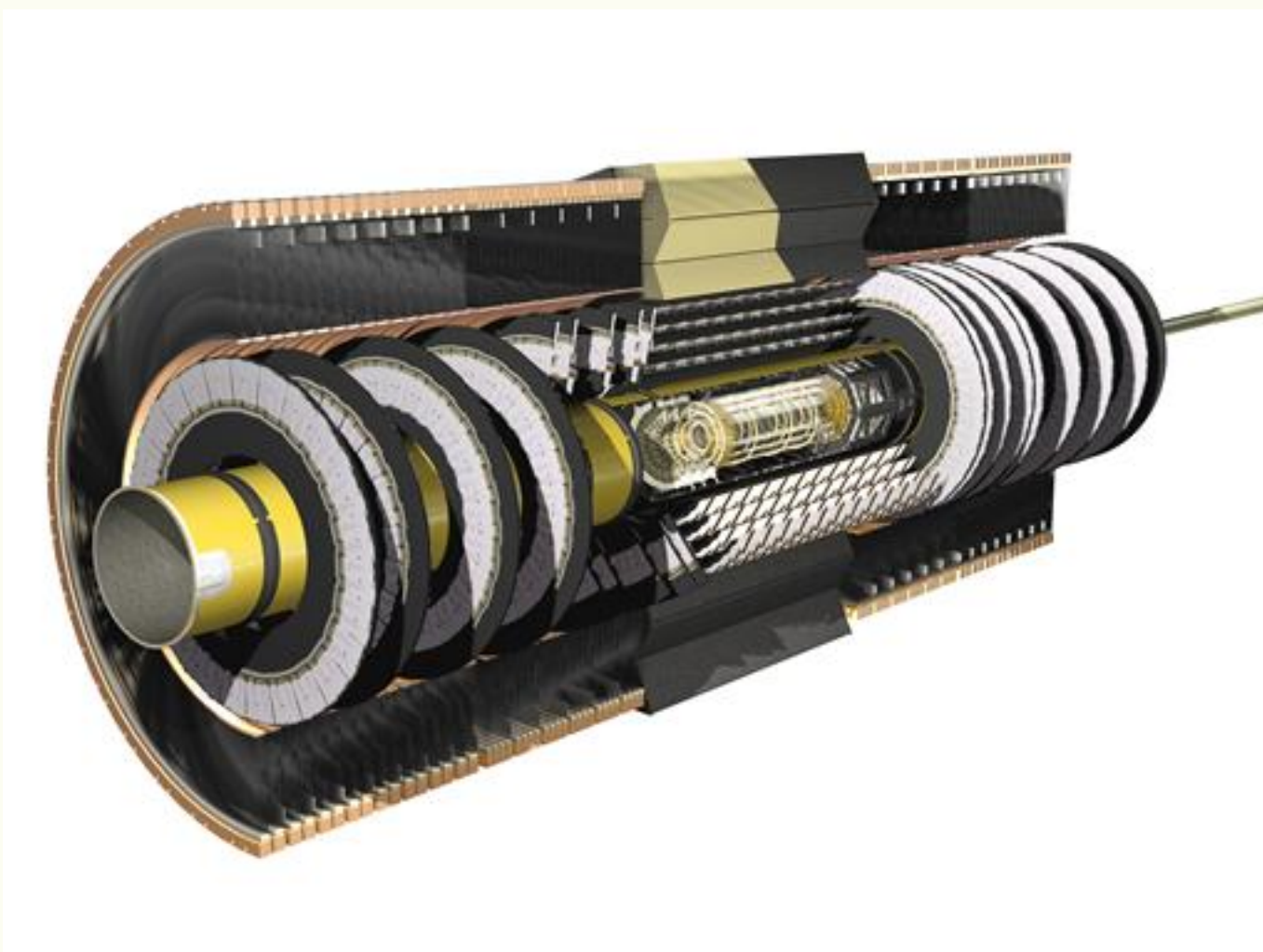


**HL-LHC**

- 2008 - 2025
- $\langle \mu \rangle \sim 30$
- $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- $400 \text{ fb}^{-1}$  ( $190 \text{ fb}^{-1}$  so far)

- 2028 ~
- $\langle \mu \rangle \sim 200$
- $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- $4000 \text{ fb}^{-1}$

## ATLAS "Current" Inner Detector



## Requirement for the pixel detector and its readout becomes demanding

- **Radiation tolerance**
  - Current ID Pixel designed for  $\sim 400 \text{ fb}^{-1}$
- **Bandwidth saturation**
  - Current ID designed to accommodate  $\langle \mu \rangle \sim 50$  at  $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$



# High Luminosity LHC

**LHC**

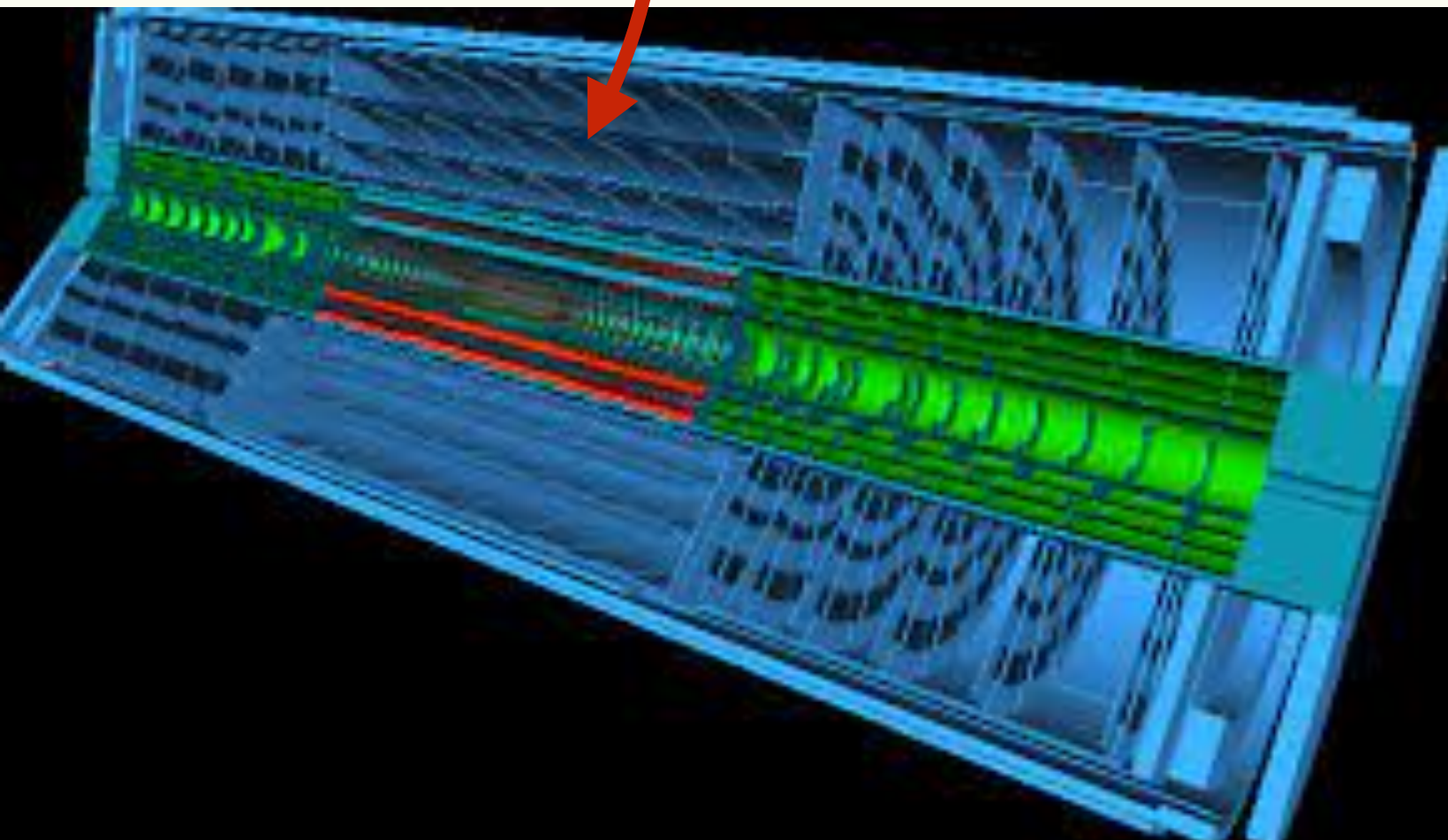
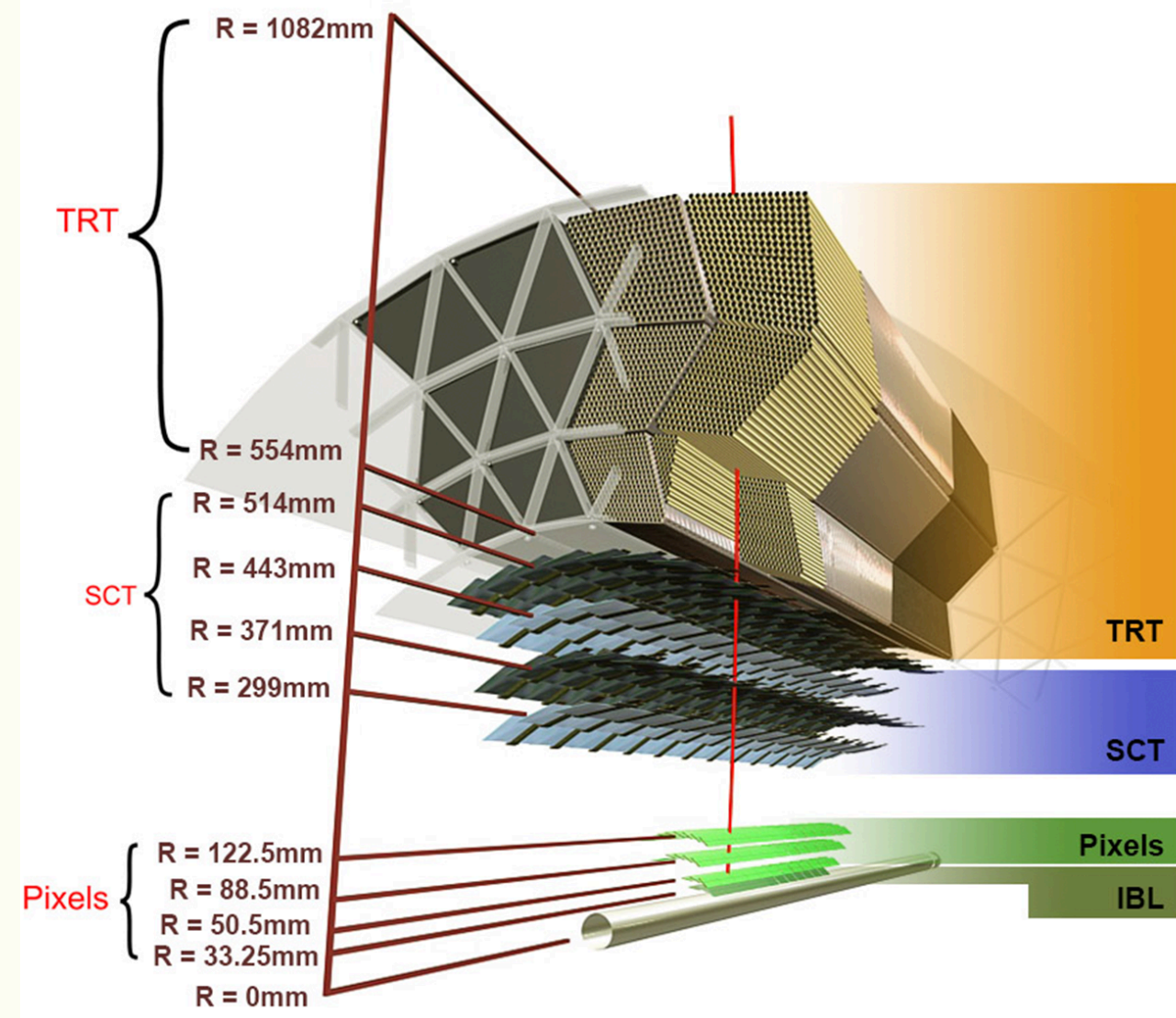
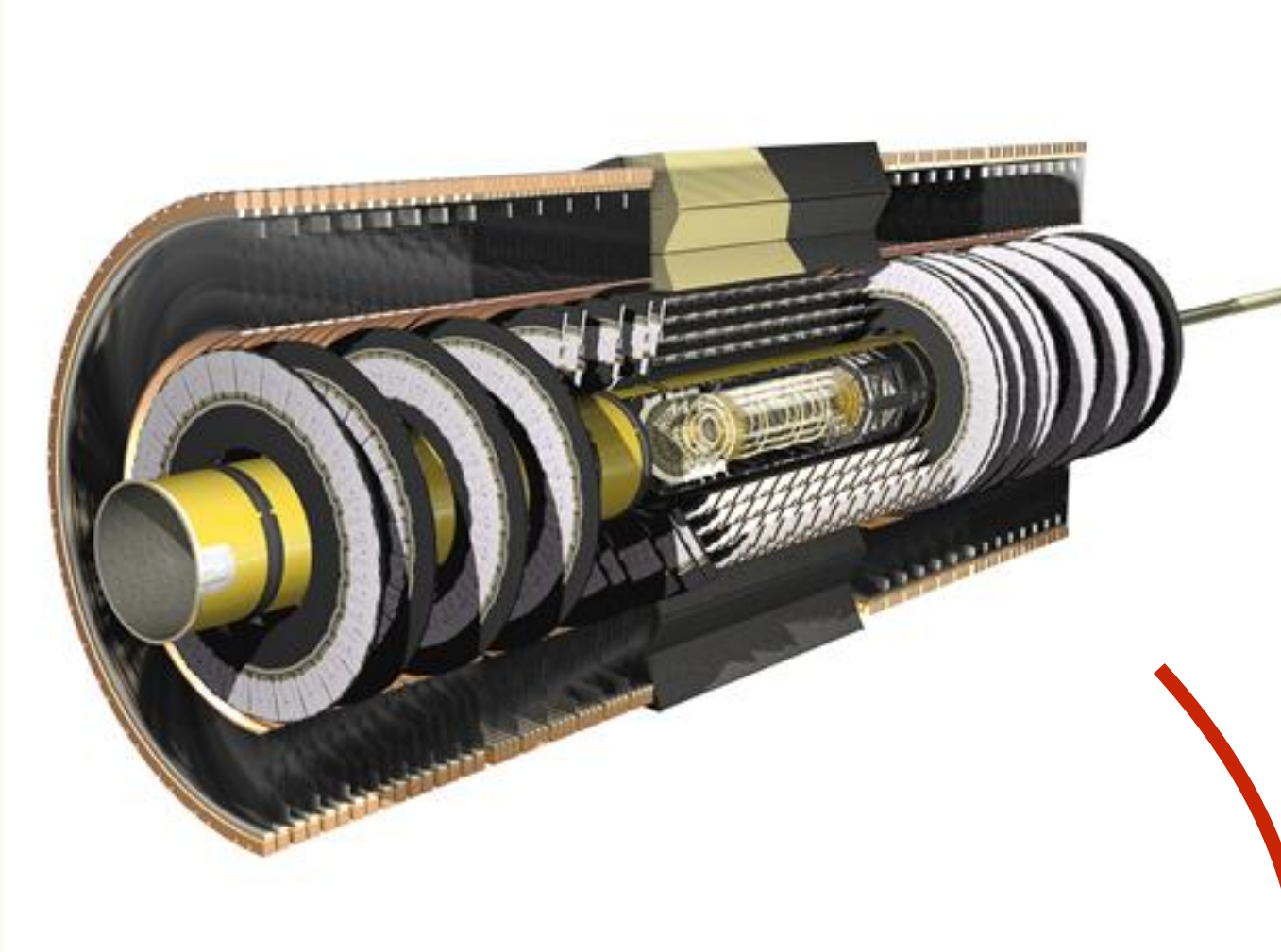


**HL-LHC**

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## ATLAS "Current" Inner Detector

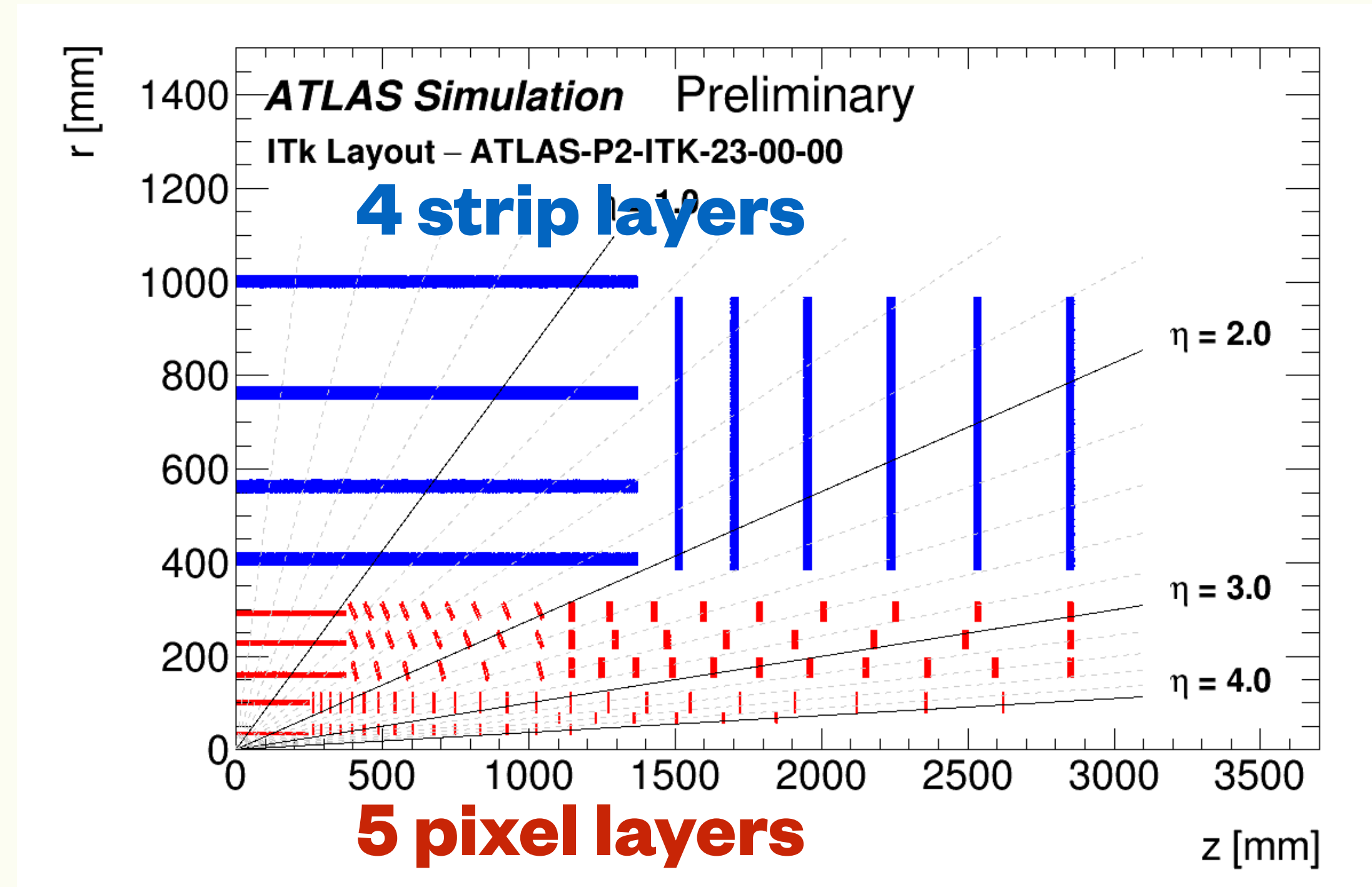


**The current Inner Detector will be replaced by an all silicon Inner Tracker**



# ATLAS Inner Tracker Upgrade

- New Inner detector have to cope with the HL-LHC environment
  - **Better radiation tolerance**
    - Fluence of  $2 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ , 4000 fb<sup>-1</sup>
  - **Faster readout**
    - 5 Gbit/s per data link
  - **Finer granularity**
    - keep  $\sim 1\%$  occupancy



	Current ID	ITk
Covered area (Pix) [m <sup>2</sup> ]	1.9	13
Covered area (Strip) [m <sup>2</sup> ]	60	160
Readout channels (Pix)	$\sim 9.2 \times 10^6$	$5 \times 10^9$
Readout channels (Strip)	$\sim 6 \times 10^6$	$\sim 50 \times 10^6$
$ \eta $ coverage	2.5	4.0
Pixel size [ $\mu\text{m}^2$ ]	50 x 400, 50 x 250	50 x 50, 25 x 100
L1 Trigger [kHz]	100	1000

# ITk Pixel Detector

- Key Concepts

- Inner 2 layers are replaceable
- Inclined modules
  - Minimise material and maximise acceptance

- Larger covered area:  $13 \text{ m}^2, |\eta| < 4$

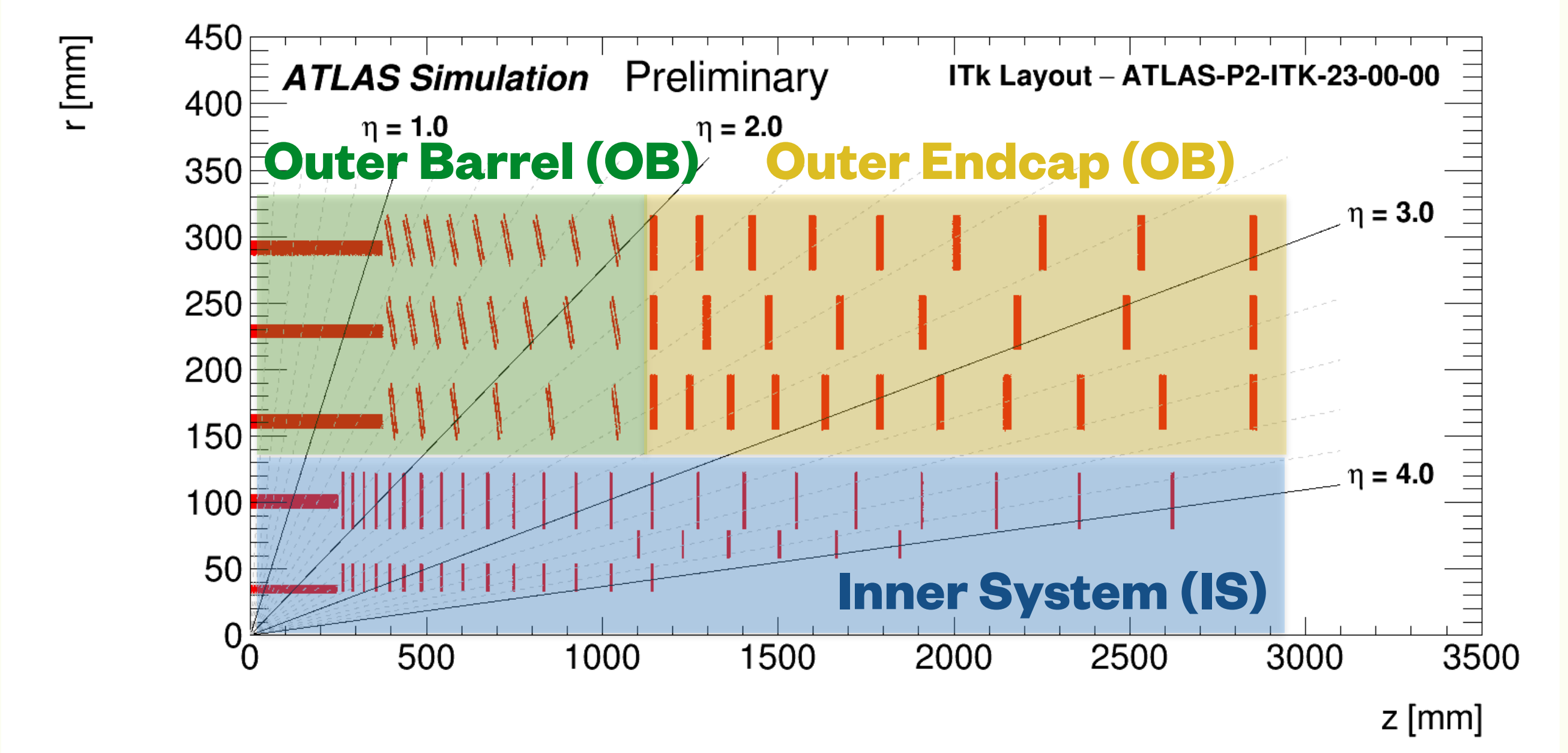
- Consists of ~ 10000 modules

- Low material budget

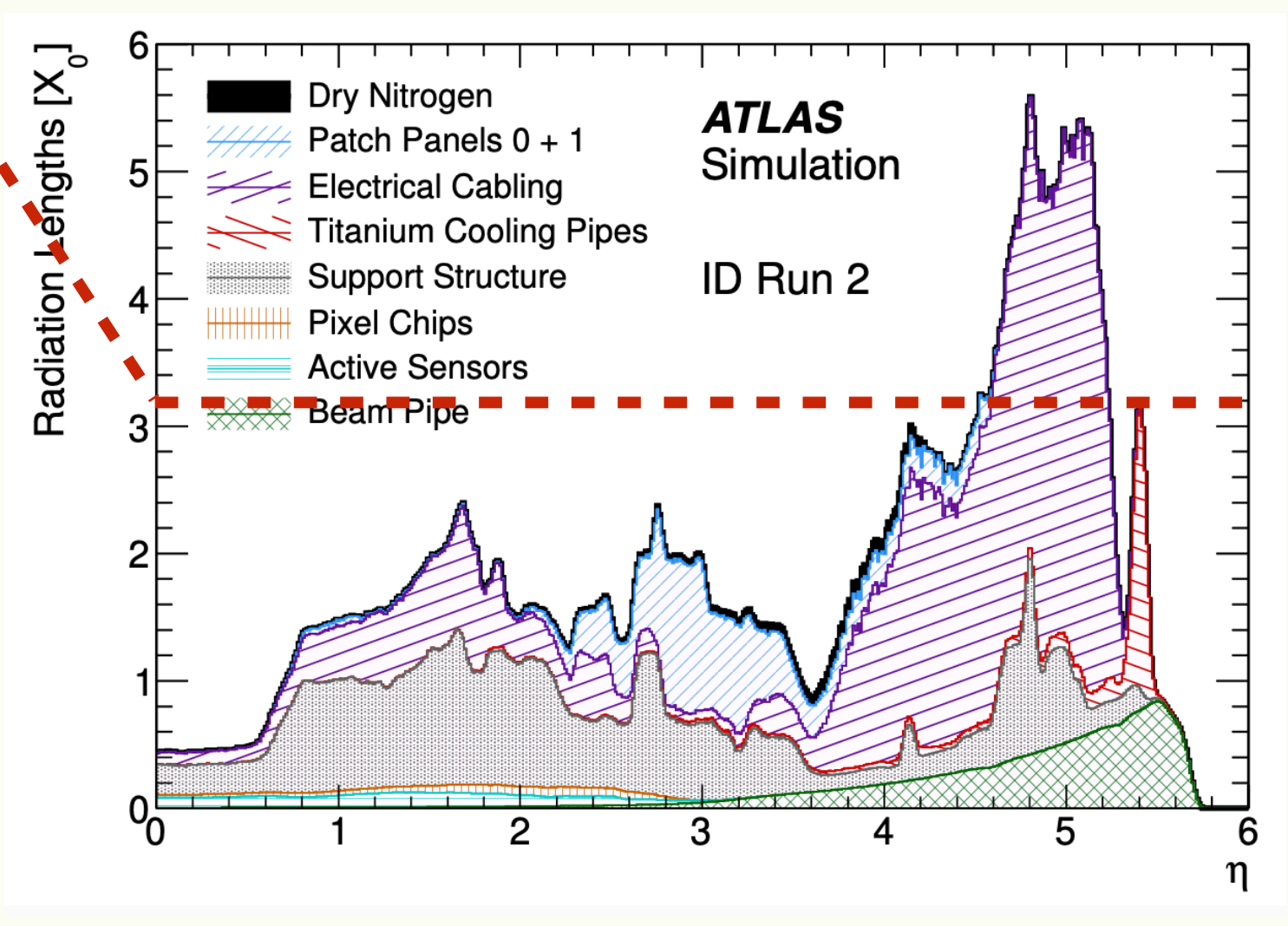
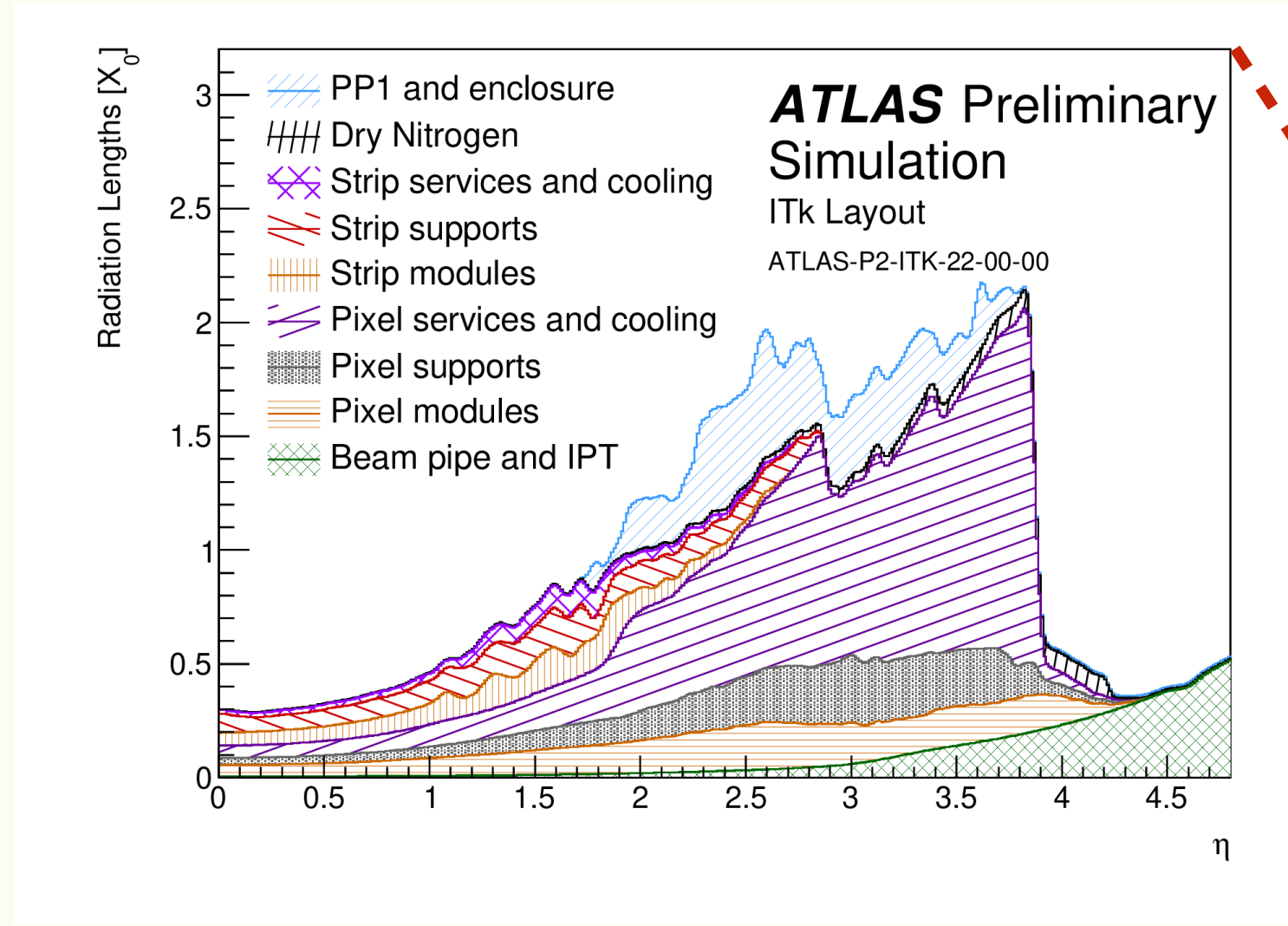
- 3D and planar sensors

- Serial powering

- Common front-end chip for all layers



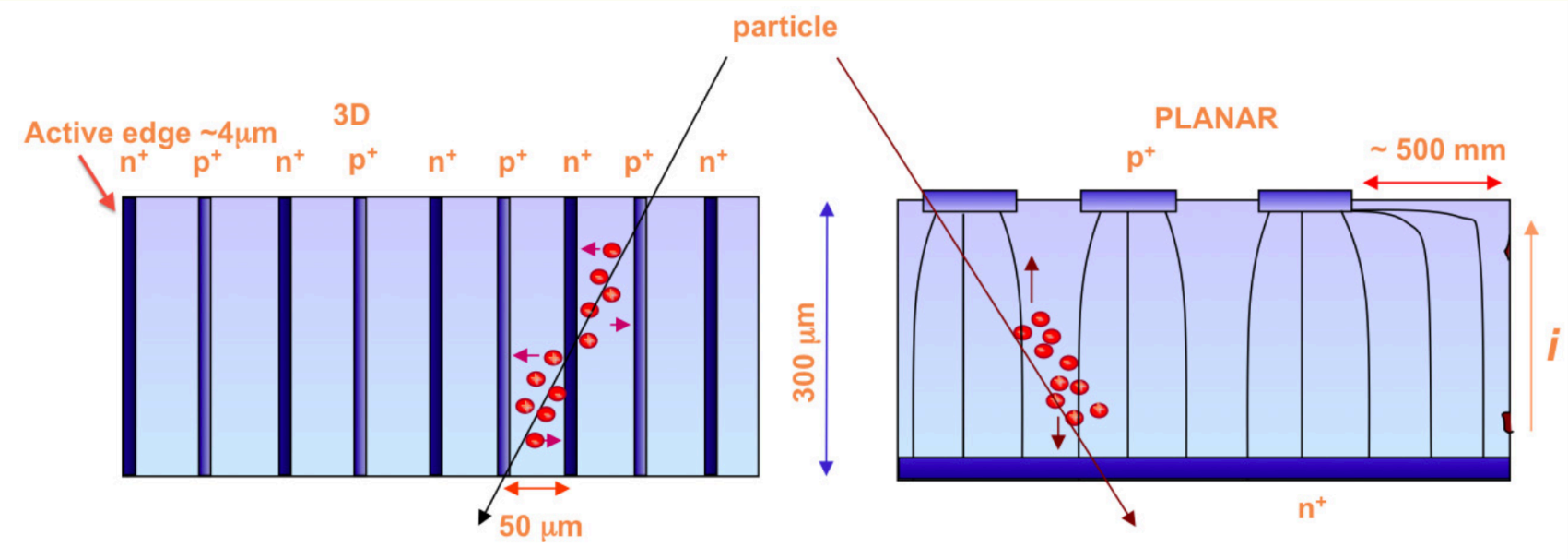
## Radiation length





# ITk Pixel Sensor

- Main change in sensor technology is the increase in the required level of tolerance to radiation



- 3D sensors: radiation hardness, low power dissipation

- At the innermost layer (L0)
- in the triplet modules

- Planar sensors: high fabrication yield and lower costs

- In all other layers (L1-L4)
- In the quad modules

Luminosity	Layer	Location	R (cm)	z (cm)	Fluence ( $10^{14} n_{eq}/cm^2$ )	Dose (MGy)
2000 fb <sup>-1</sup>	0	flat barrel	3.9	0.0	131	-
		inclined barrel	4.0	24.3	-	7.2
			3.7	25.9	123	-
		end-cap	3.7	110.0	-	9.9
2000 fb <sup>-1</sup>	1	flat barrel	5.1	123.8	68	6.3
		flat barrel	9.9	24.3	27	1.5
		inclined barrel	8.1	110.0	35	2.9
4000 fb <sup>-1</sup>	2-4	end-cap	7.9	299.2	38	3.2
		flat barrel	16.0	44.6	28	1.6
		inclined barrel	15.6	110.0	30	2.0
4000 fb <sup>-1</sup>	2-4	end-cap	15.3	299.2	38	3.5

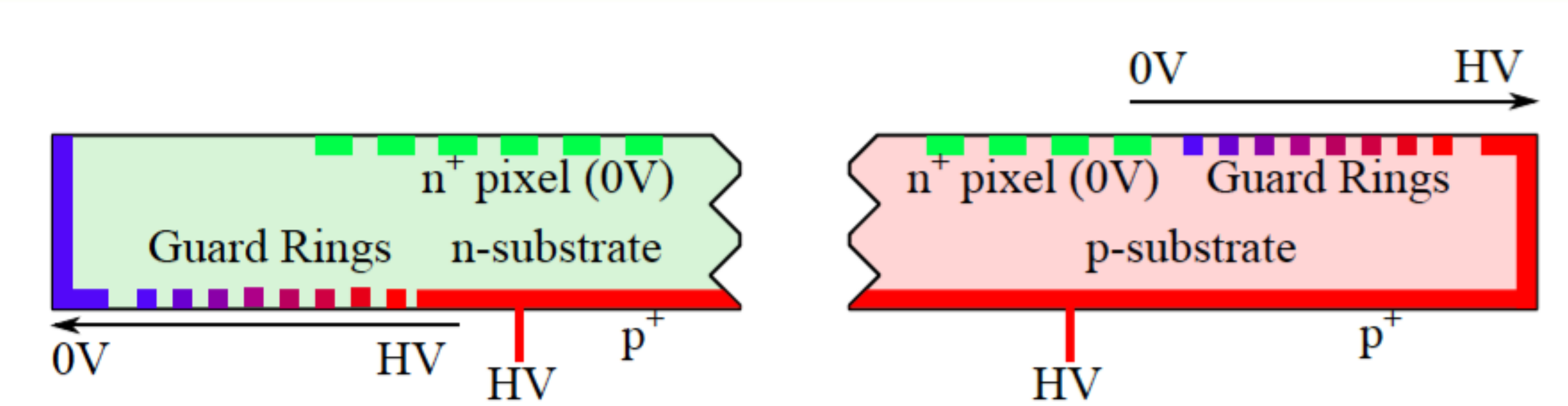
# Planar Sensor

## IBL

- Thickness of 200  $\mu\text{m}$
- 50 x 250  $\mu\text{m}^2$  pixel cells
- n-in-n

## ITk

- Thickness of 100, 150  $\mu\text{m}$
- 50 x 50  $\mu\text{m}^2$  pixel cells
- n-in-p

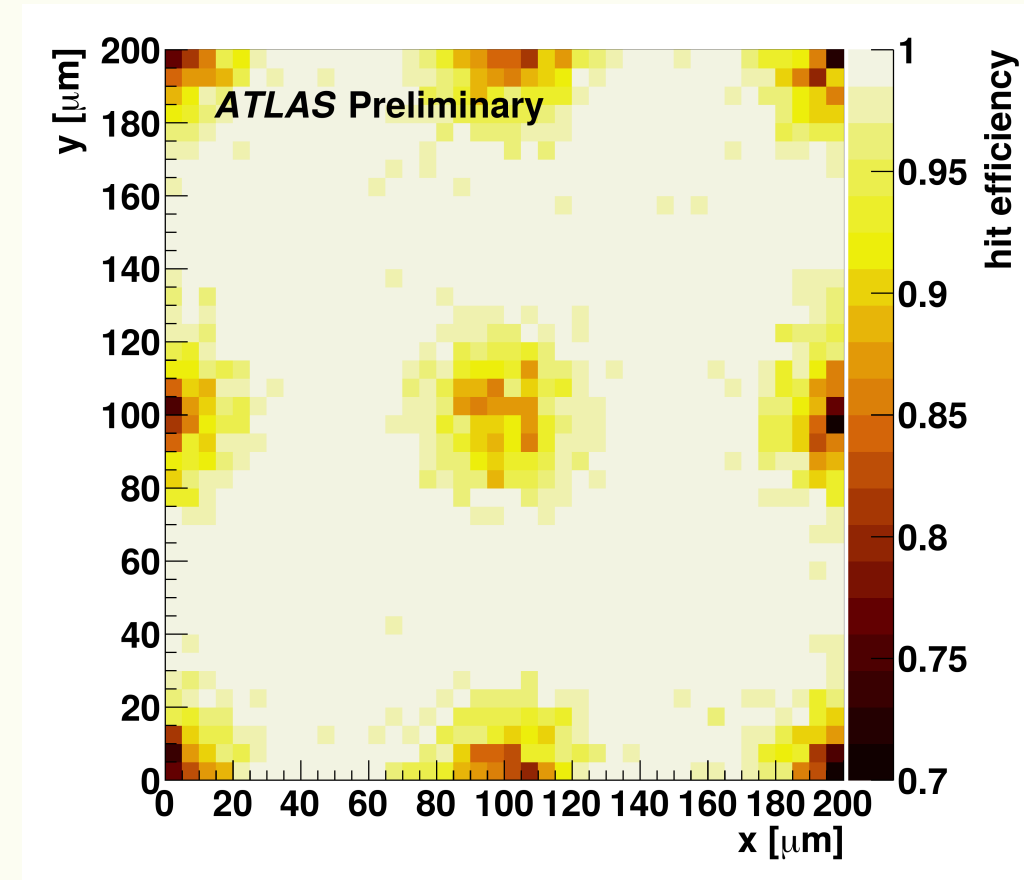
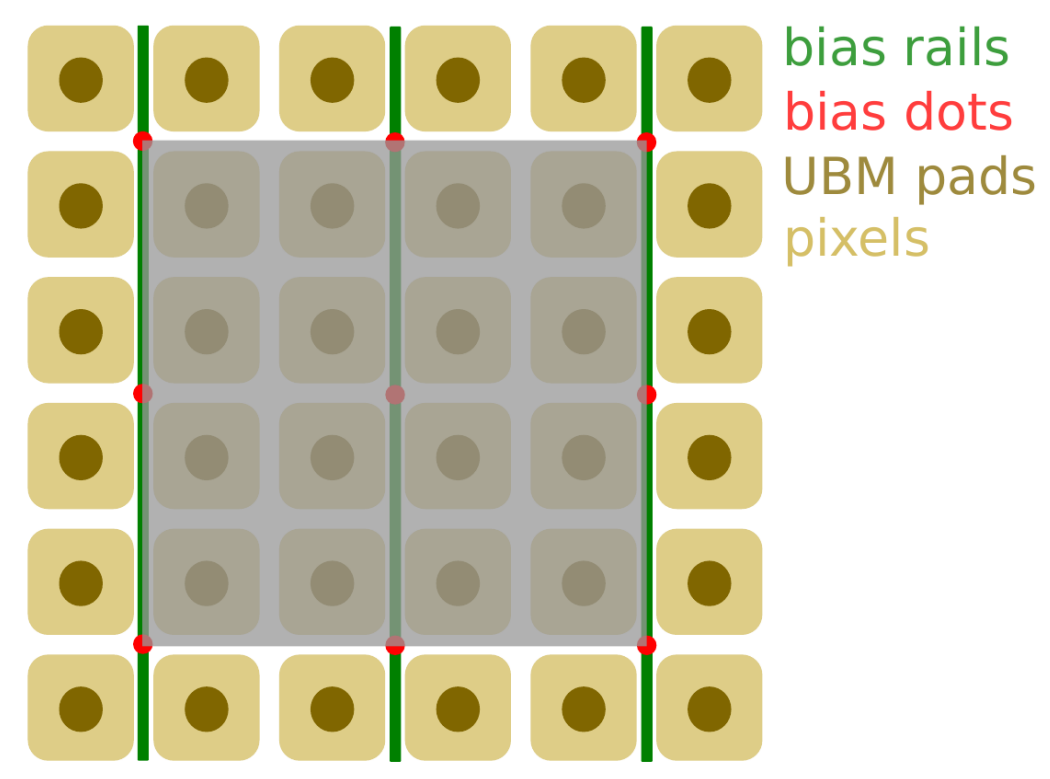


## n-in-p technology

- Well proven and understood technique
- Single sided process (simple production, low cost)

## Required Performance

- Hit efficiency > 97% (after irradiation)
- Bias voltage at end of life up to:
  - 600 V for 150  $\mu\text{m}$  sensor
  - 400 V for 100  $\mu\text{m}$  sensor



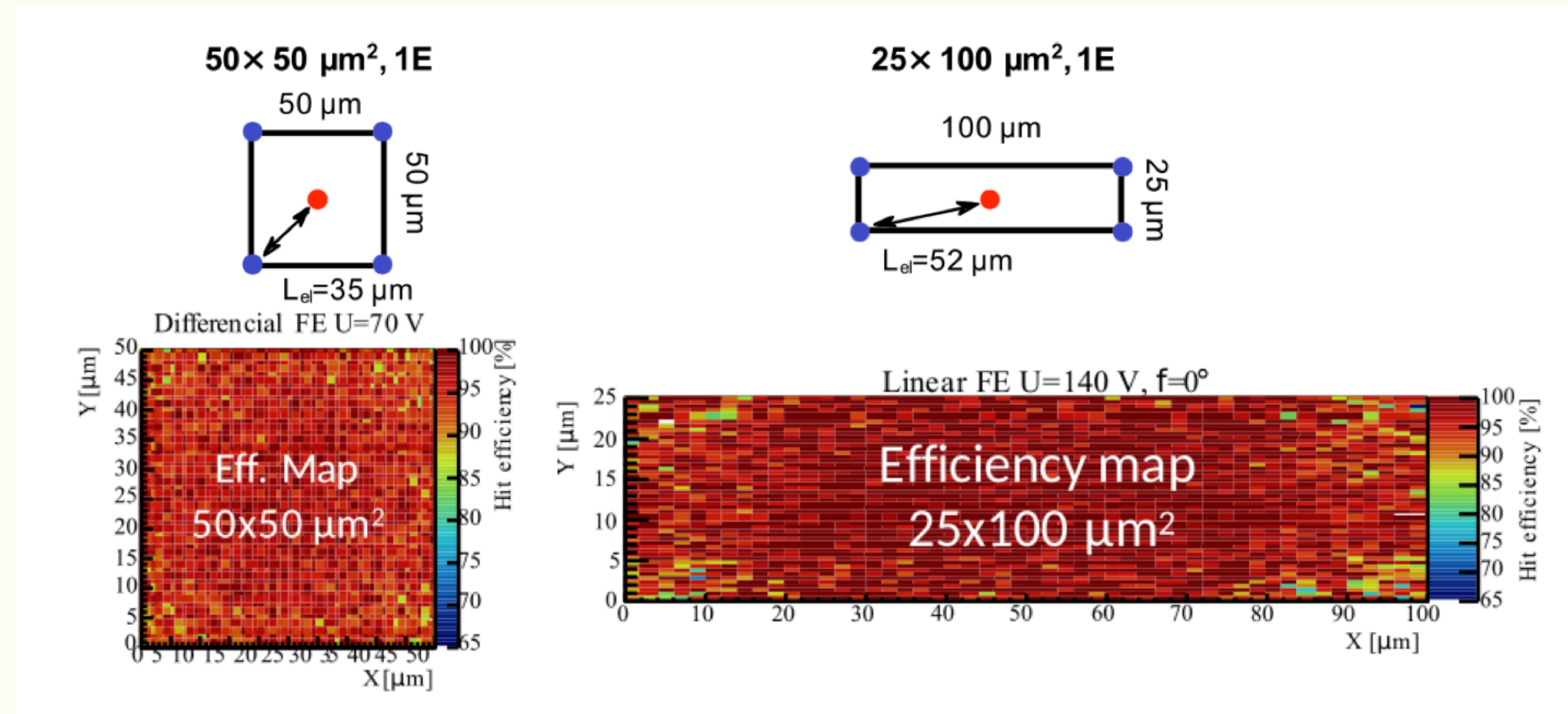


# 3D Sensor

- 3D sensor used in the innermost layer
  - 150  $\mu\text{m}$  active thickness + 100  $\mu\text{m}$  support wafer
  - 50 x 50  $\mu\text{m}^2$  (endcap region)
  - 25 x 100  $\mu\text{m}^2$  (barrel region)
  - More radiation tolerant

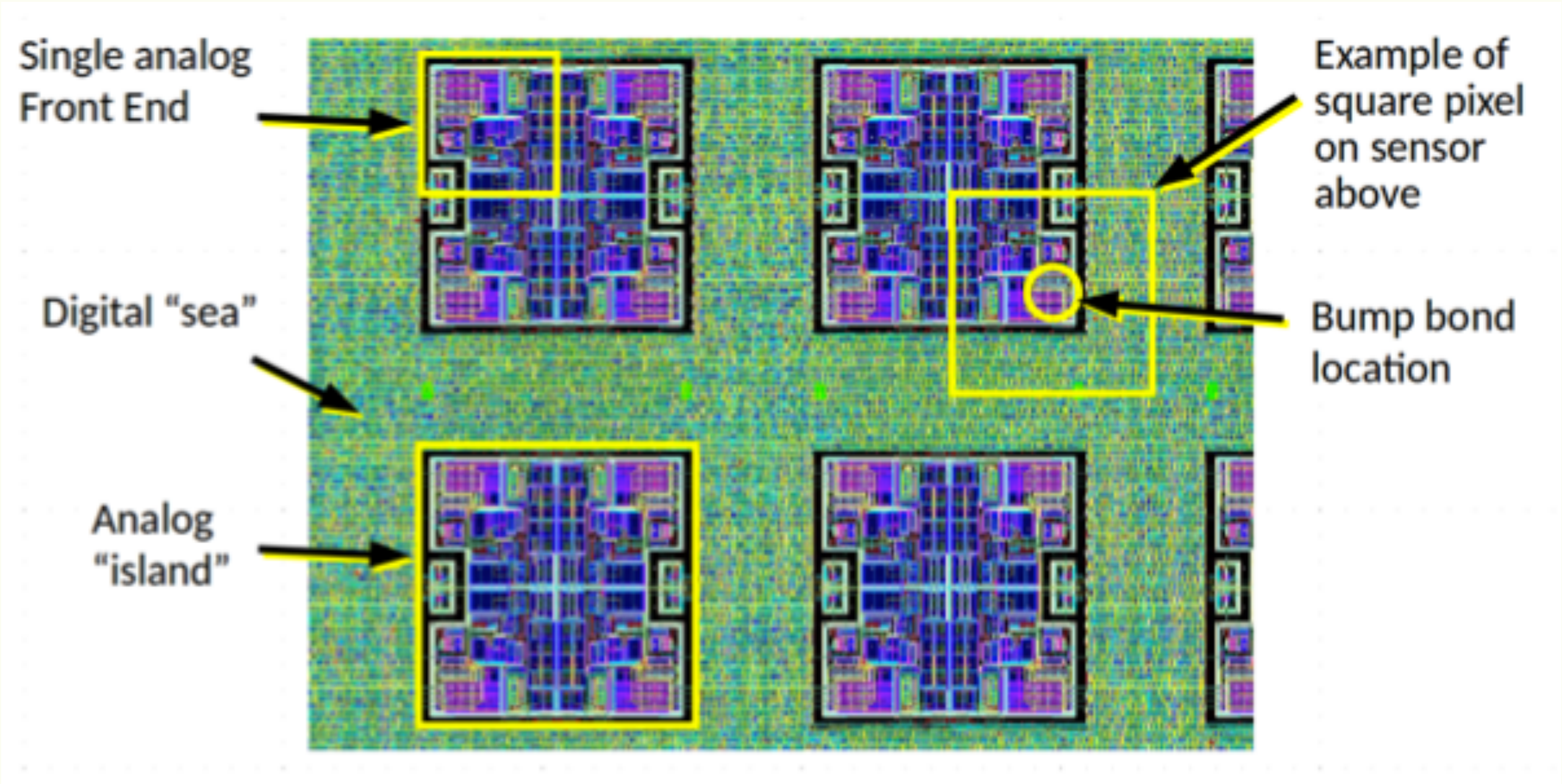
## Required Performance

- Hit efficiency  $> 97\%$  (after irradiation)
- Low operational bias voltage: 80-140 V
- Low power dissipation





# ITk Front-End Chip

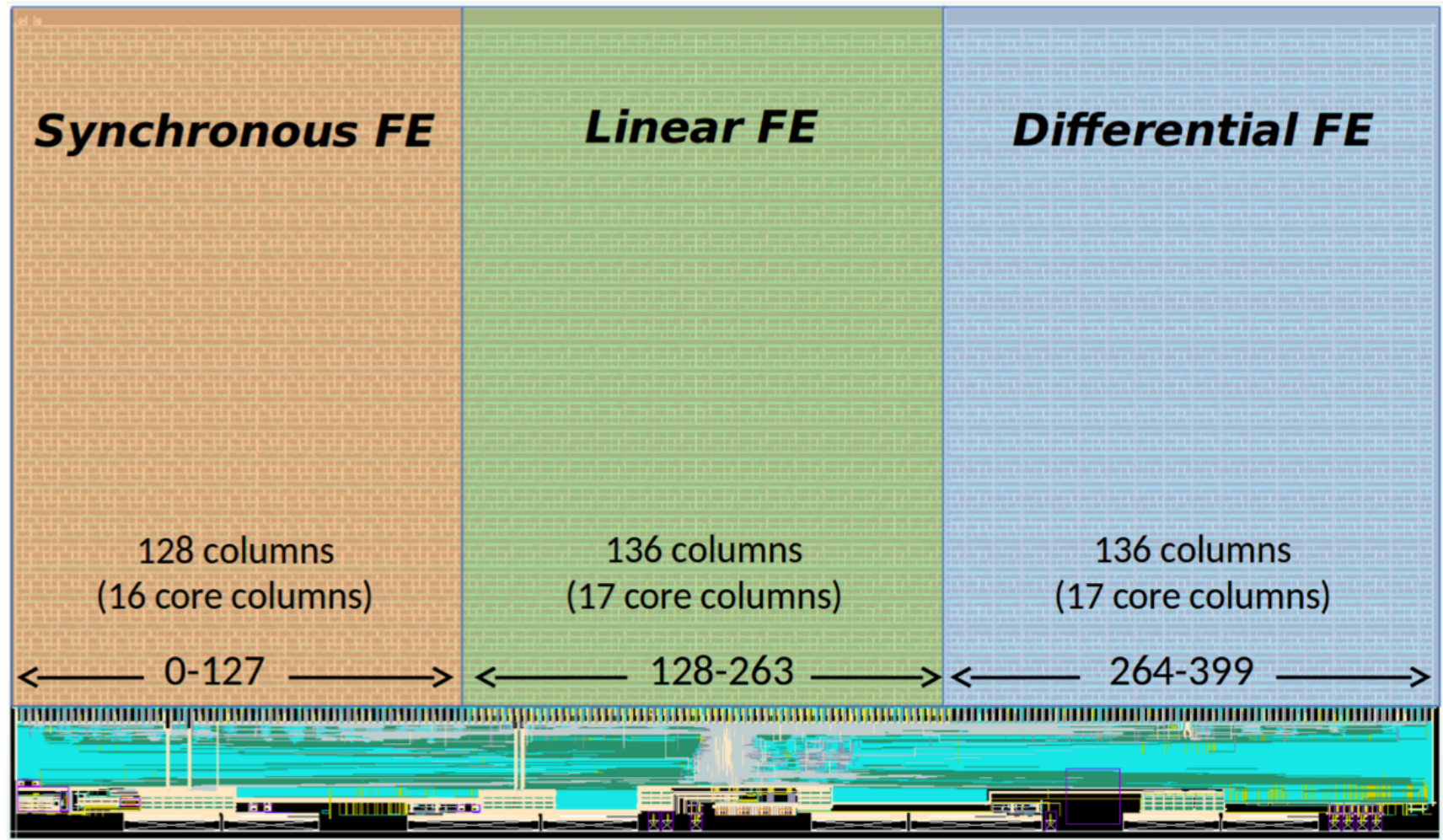


## RD53A Prototype

- 3 different type FEs are on a single chip
- 400 x 192 pixels
- 50 x 50  $\mu\text{m}^2$

## RD53 Collaboration

- ATLAS and CMS
- 65 nm TSMC technology (130 nm for IBL)
- 50  $\mu\text{m}$  minimum pitch
- Shunt LDO implementation for compatibility with Serial Powering





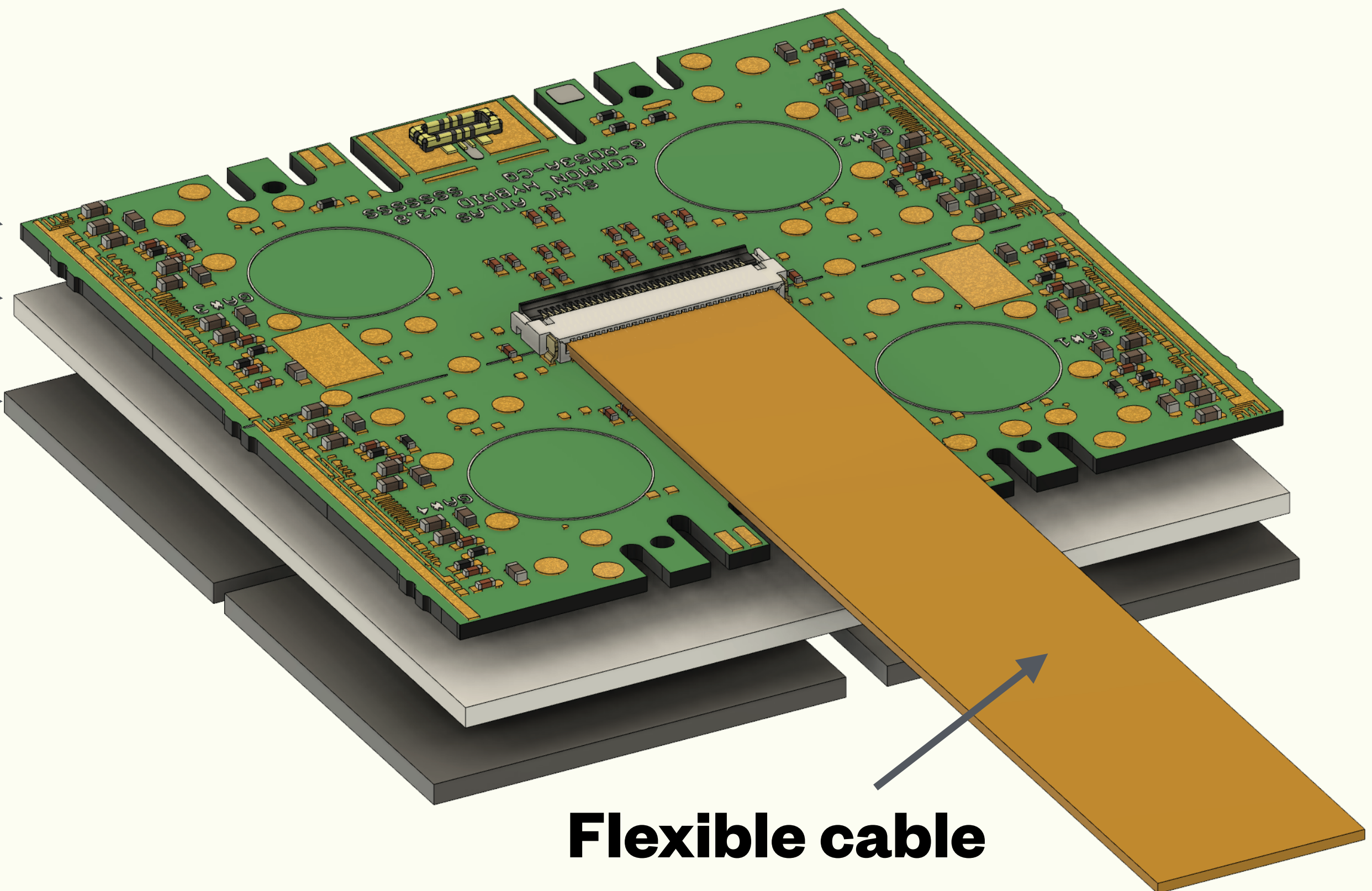
# ITk Pixel Module

Quad module (40 x 40 mm<sup>2</sup>)

Flexible PCB

Silicon Sensor

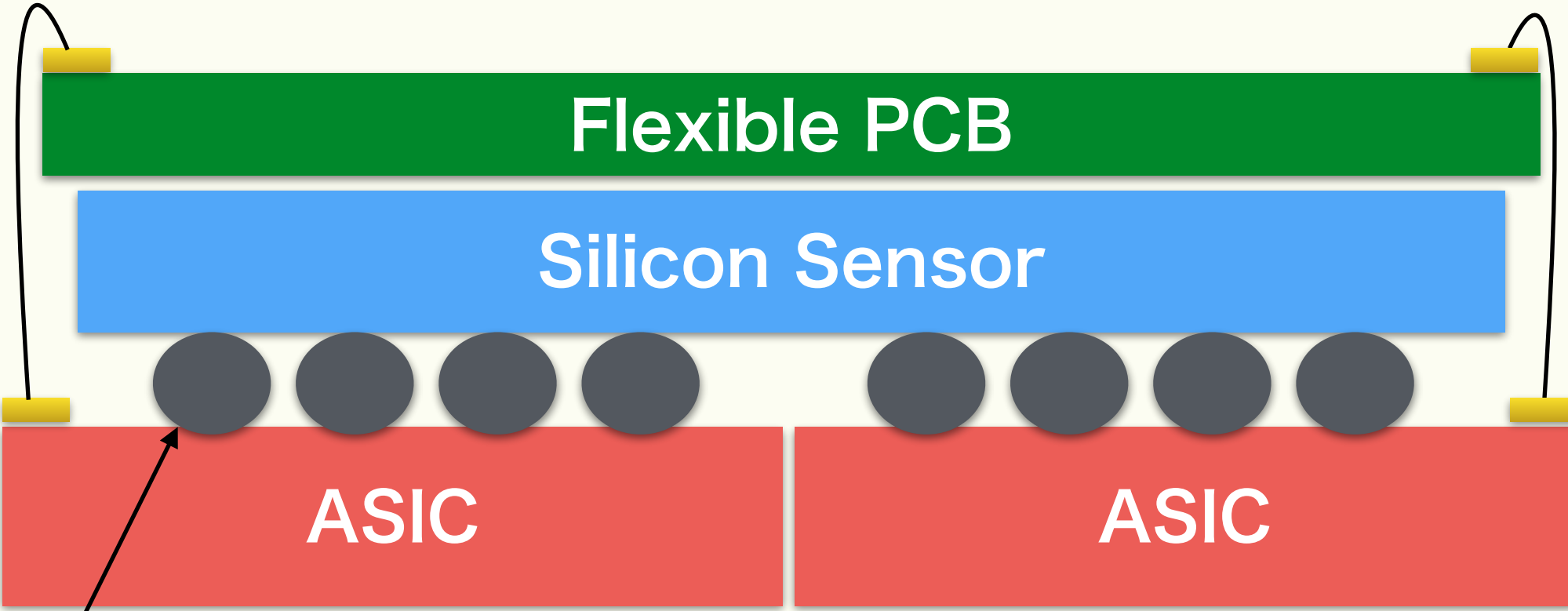
ASIC



## Hybridization

- Fine-pitch bump-bonding
- Bump deposition, UBM, flip chip

Wire-bond



Bump-bond

Flexible cable

- 50 x 50 μm<sup>2</sup> pixel
- 1.28 Gb/s per lane

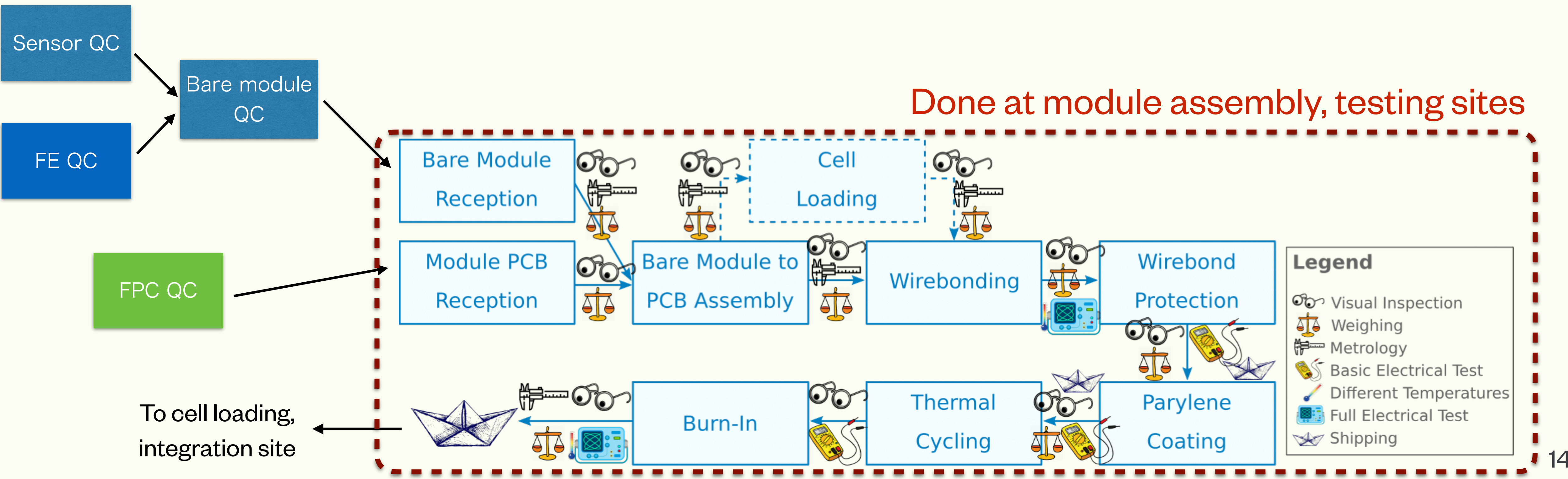


# Module QC

- All modules have to pass "module QC"
  - Many institutes (> 20) are joining in the Production

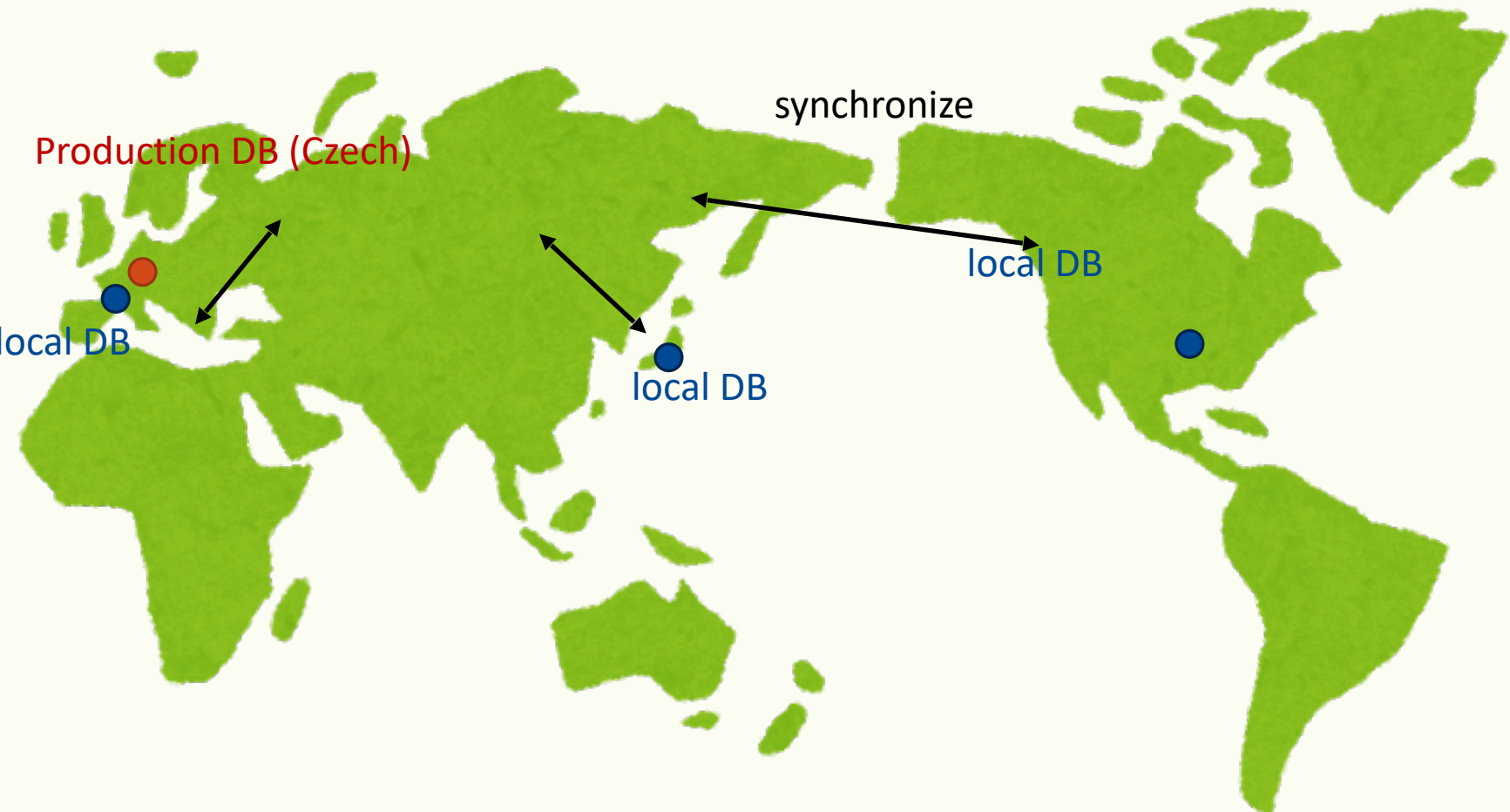
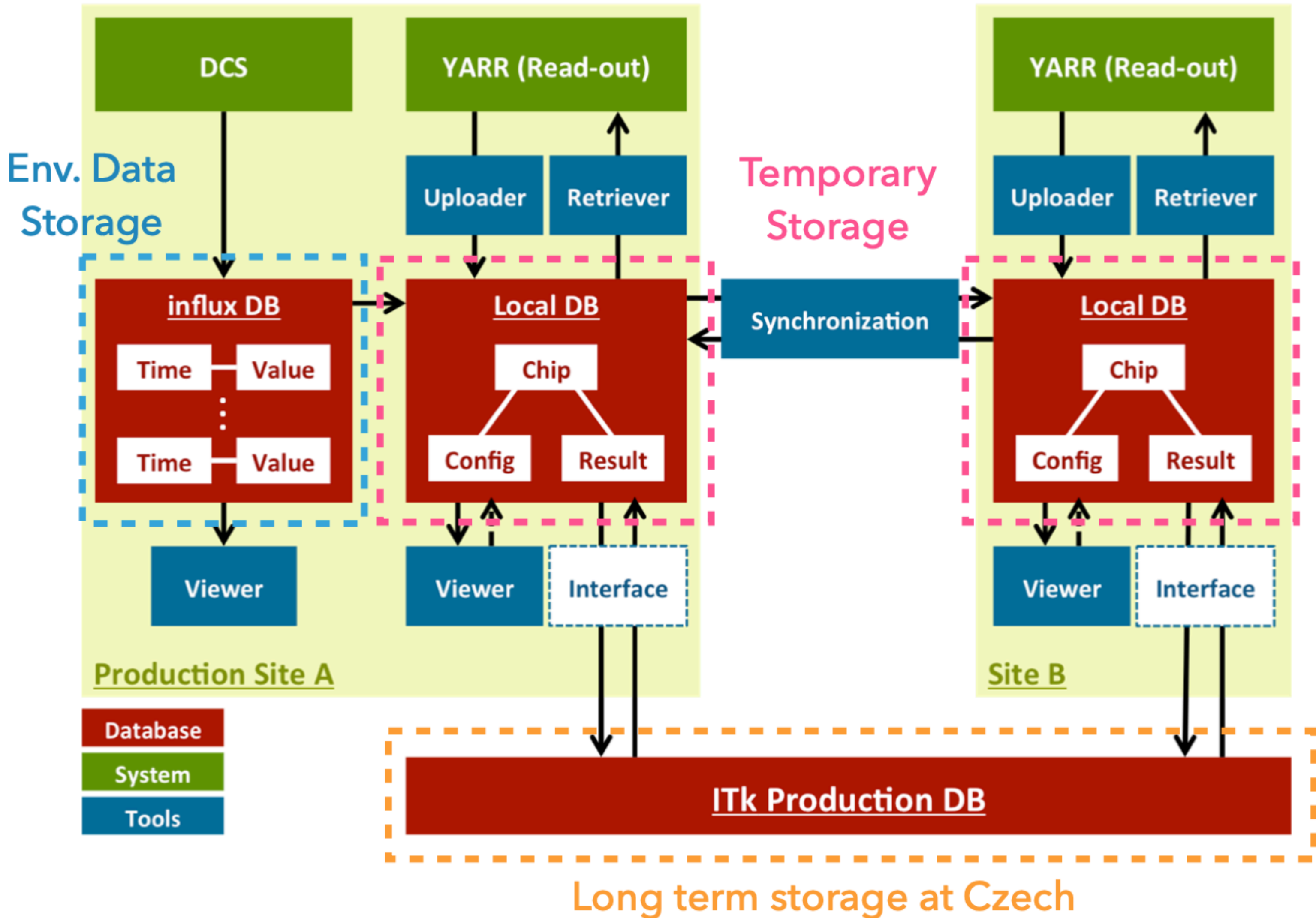
## Difficulty for QC tests

- Perform comparable tests with variety of testing setup
- Properly handle testing data to compare between different stage/sites





# Database

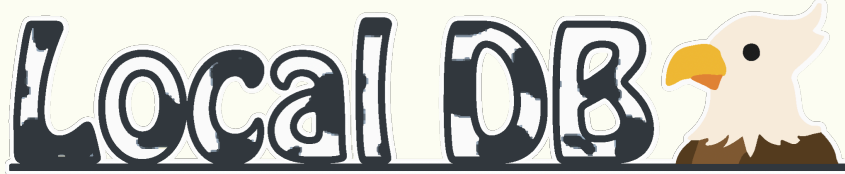


## Central DB: ITk Production DB

- Storage for all data of ITk

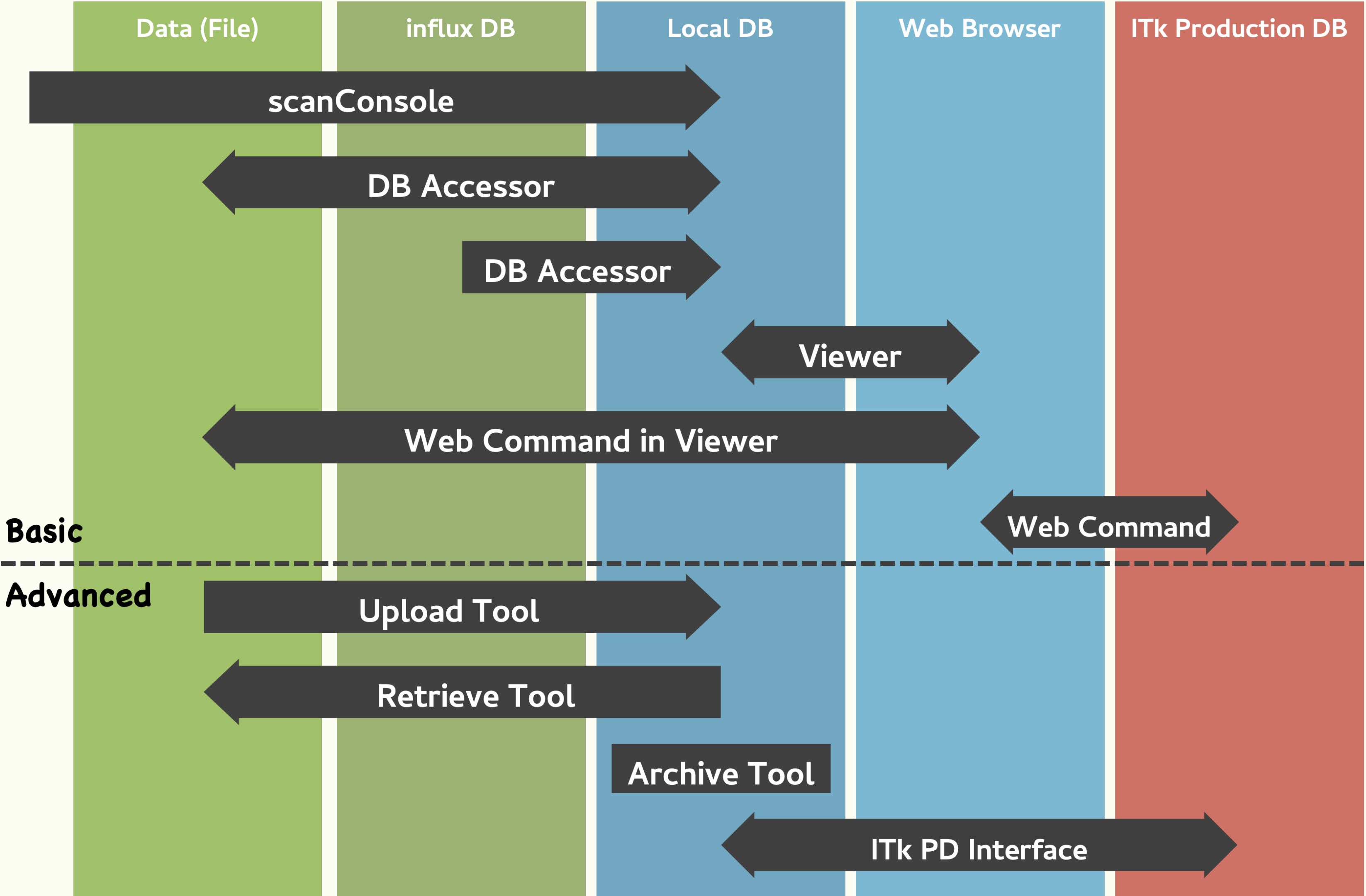
## Local DB:

- Temporary storage of each site





# Data Flow





# Local Data Base

## NoSQL Database

- Favoured due to its flexibility compared to SQL DB
- Data is stored as a “json” format (“document”)

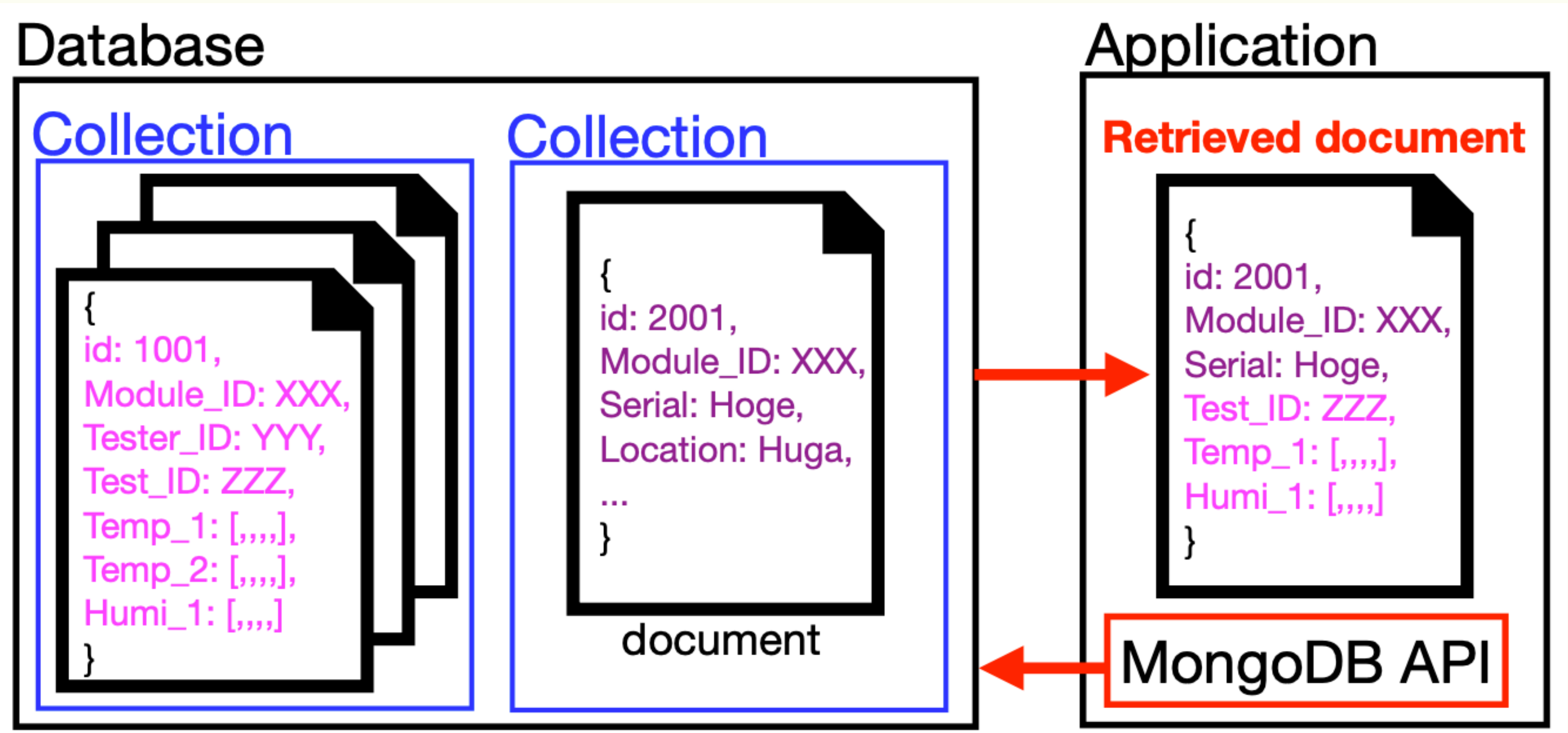


## SQL

- Relational
- Structured data
- Vertically scalable
- Table based

## NoSQL

- Non-relational
- Unstructured data
- Horizontally scalable
- Document, key-value, graph, or wide-column

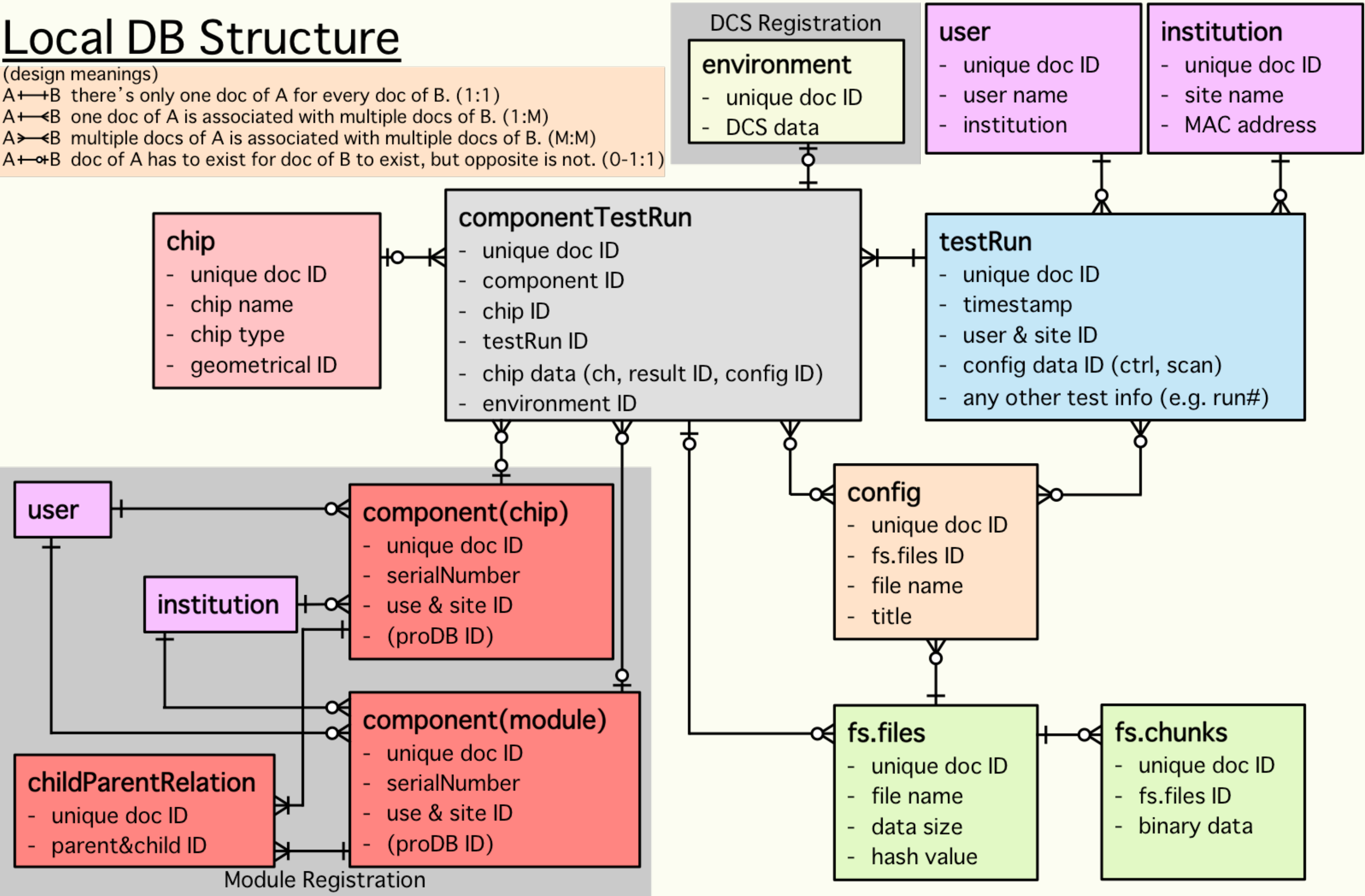




# Structure of LocalDB

## Local DB Structure

(design meanings)  
 A → B there's only one doc of A for every doc of B. (1:1)  
 A ← B one doc of A is associated with multiple docs of B. (1:M)  
 A ↔ B multiple docs of A is associated with multiple docs of B. (M:M)  
 A → B doc of A has to exist for doc of B to exist, but opposite is not. (0-1:1)





# Local DB Viewer

## Custom Web application based on Flask

LocalDB | TOP | COMPONENTS | SCANS | Asia/Tokyo | Sign in

Top Page > Scan List

### Scan List

Input keywords  Partial match  Perfect match

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 >>

Module Name	Chip Name	Test Data				Link	Tags
		Test Type	User	Site	Date		
KEKQ07	chip1 chip2 chip3 chip4	std_analogscan	atlasj	atlaspc9.kek.jp	2021/08/19 18:07:25	<a href="#">result page</a>	hoge
KEKQ07	chip1 chip2 chip3 chip4	std_digitalscan	atlasj	atlaspc9.kek.jp	2021/08/19 18:06:54	<a href="#">result page</a>	
KEKQ07	chip1 chip2 chip3 chip4	std_analogscan	atlasj	atlaspc9.kek.jp	2021/08/19 13:07:26	<a href="#">result page</a>	
KEKQ07	chip1 chip2 chip3 chip4	std_digitalscan	atlasj	atlaspc9.kek.jp	2021/08/19 13:07:04	<a href="#">result page</a>	
KEKQ07	chip1 chip2 chip3 chip4	std_analogscan	atlasj	atlaspc9.kek.jp	2021/08/19 12:53:58	<a href="#">result page</a>	
KEKQ07	chip1 chip2 chip3 chip4	std_digitalscan	atlasj	atlaspc9.kek.jp	2021/08/19 12:53:35	<a href="#">result page</a>	
KEKQ07	chip1 chip2 chip3 chip4	std_analogscan	atlasj	atlaspc9.kek.jp	2021/08/19 12:46:57	<a href="#">result page</a>	

LocalDB | TOP | COMPONENTS | SCANS | Asia/Tokyo | Sign in

Top Page > Component List > Scan List > Component > Scan Result

### Component: 20UPGR10099999 [Component page of ITkPD](#)

Current Stage: MODULEWIREBONDPROTECTION

Result: 133

#### Information

Item	Value
Serial Number	20UPGR10099999
Component Type	module
FE type	RD53A
Children	<a href="#">20UPGFC9999995</a> <a href="#">20UPGFC9999996</a> <a href="#">20UPGFC9999997</a> <a href="#">20UPGFC9999998</a>

#### Result

Key	Data
runNumber	133
testType	std_analogscan
stage	MODULEWIREBONDING
component	<a href="#">20UPGR10099990</a> <a href="#">20UPGFC9999995</a> <a href="#">20UPGFC9999996</a> <a href="#">20UPGFC9999997</a> <a href="#">20UPGFC9999998</a>
startTime	2021/08/05 00:48:14
finishTime	2021/08/05 00:49:09
user	kinoshita
site	gemin
targetCharge	-1
targetTot	-1
exec	-r configs/controller/emuCfg_rd53a.json -c db-data/connectivity.json -s configs/scans/rd53a/std_analogscan.json -W
stopwatch	analysis: 548 config: 533 processing: 2 scan: 49035
QC	False
environment	False
plots	OccupancyMap L1Dist EnMask
passed	True
qcTest	False
qaTest	False
summary	False

#### Output Data

Data	Type	Format	Chip	Display	Download
ctrlCfg	json			<input checked="" type="checkbox"/>	<a href="#">^</a>
dbCfg	json			<input checked="" type="checkbox"/>	<a href="#">^</a>
siteCfg	json			<input checked="" type="checkbox"/>	<a href="#">^</a>
userCfg	json			<input checked="" type="checkbox"/>	<a href="#">^</a>
scanCfg	json			<input checked="" type="checkbox"/>	<a href="#">^</a>
beforeCfg	json		<a href="#">20UPGFC9999995</a> <a href="#">20UPGFC9999996</a> <a href="#">20UPGFC9999997</a> <a href="#">20UPGFC9999998</a>	<input checked="" type="checkbox"/>	<a href="#">^</a>
afterCfg	json		<a href="#">20UPGFC9999995</a> <a href="#">20UPGFC9999996</a> <a href="#">20UPGFC9999997</a> <a href="#">20UPGFC9999998</a>	<input checked="" type="checkbox"/>	<a href="#">^</a>
OccupancyMap	json		<a href="#">20UPGFC9999995</a> <a href="#">20UPGFC9999996</a> <a href="#">20UPGFC9999997</a> <a href="#">20UPGFC9999998</a>	<input checked="" type="checkbox"/>	<a href="#">^</a>
L1Dist	json		<a href="#">20UPGFC9999995</a> <a href="#">20UPGFC9999996</a> <a href="#">20UPGFC9999997</a> <a href="#">20UPGFC9999998</a>	<input checked="" type="checkbox"/>	<a href="#">^</a>
EnMask	json		<a href="#">20UPGFC9999995</a> <a href="#">20UPGFC9999996</a> <a href="#">20UPGFC9999997</a> <a href="#">20UPGFC9999998</a>	<input checked="" type="checkbox"/>	<a href="#">^</a>

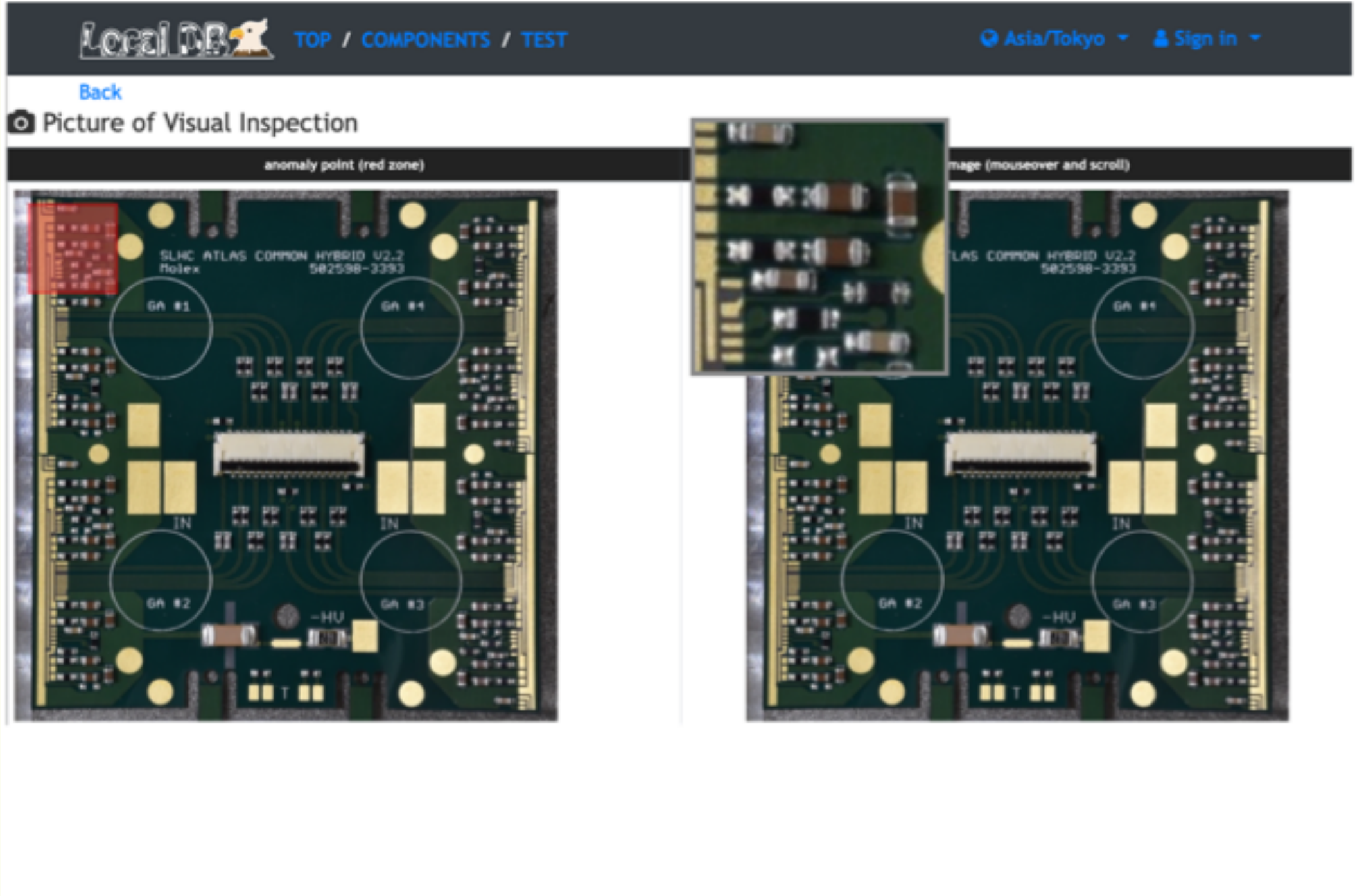
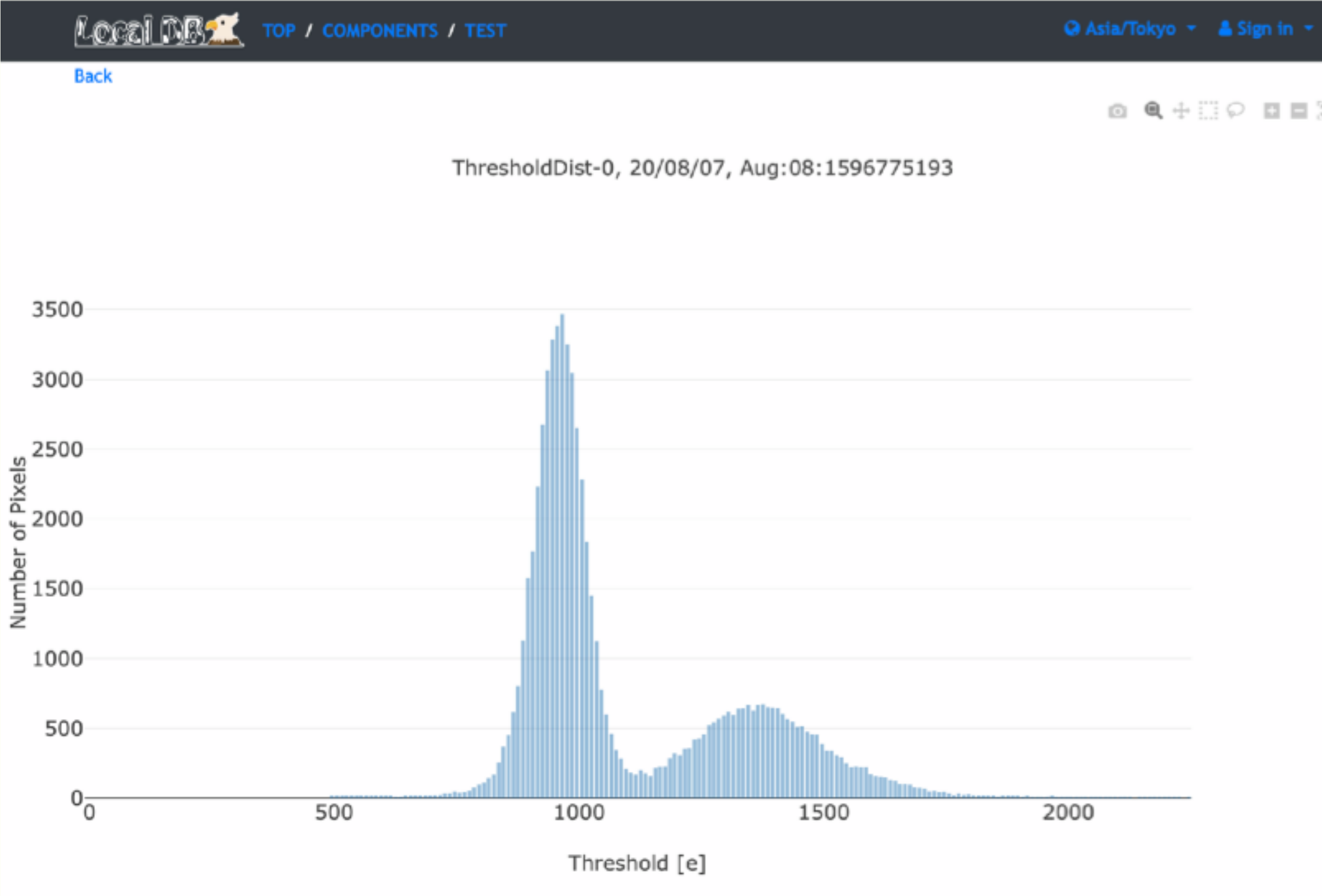
**PLOT JSROOT**

- L1Dist [plotly](#)
- OccupancyMap [plotly](#)



# Local DB Viewer

Dynamically generate plots by ploty





# Environmental Data

 **influxdb** : Time series database for environmental monitoring

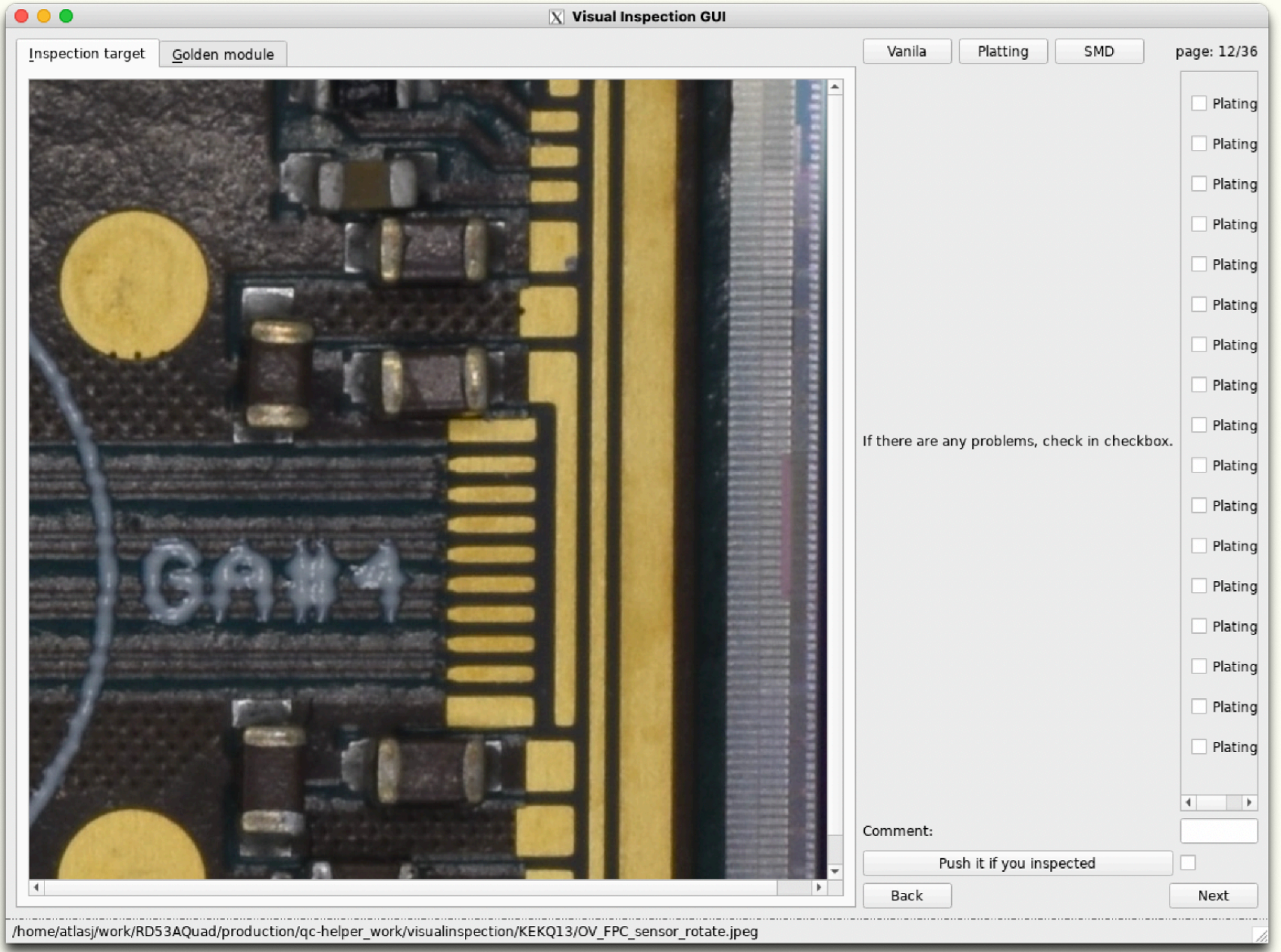
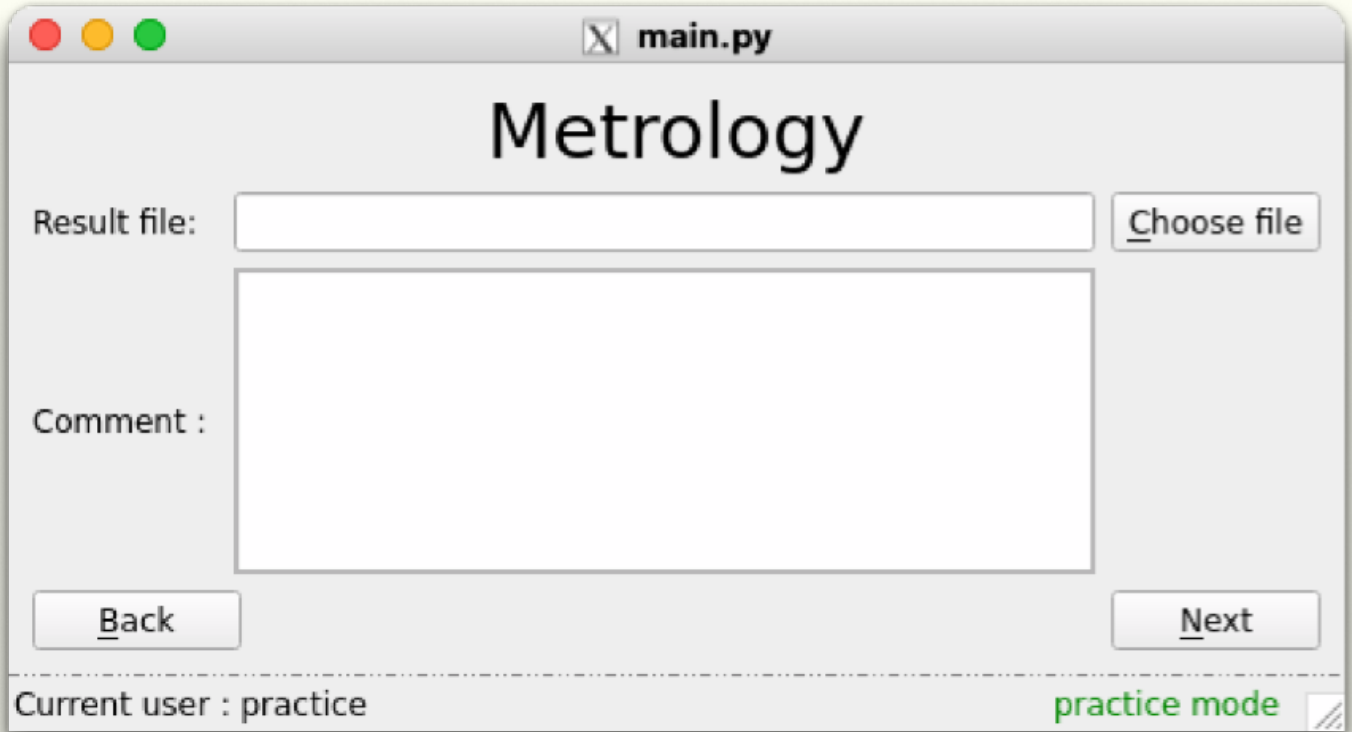
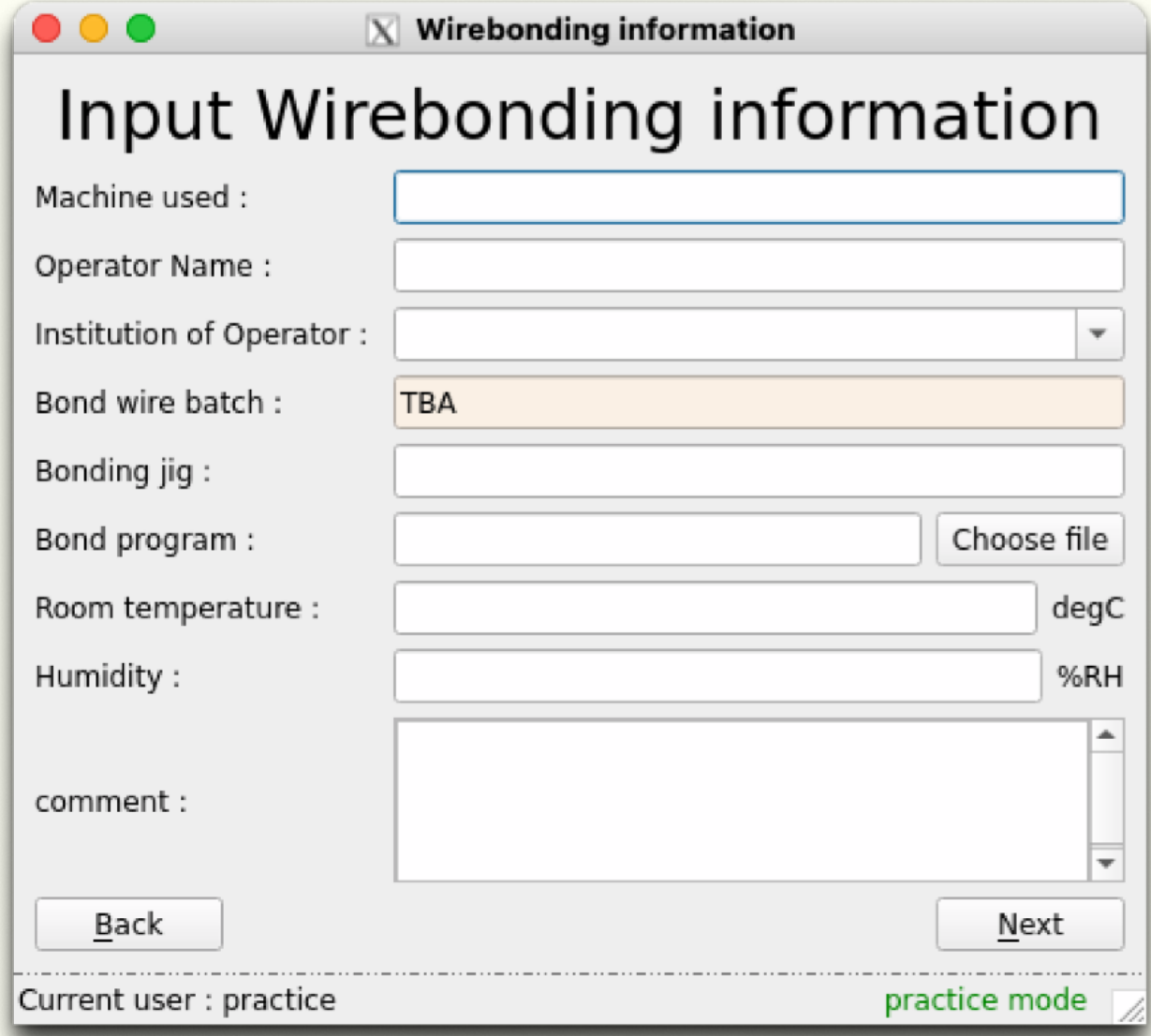
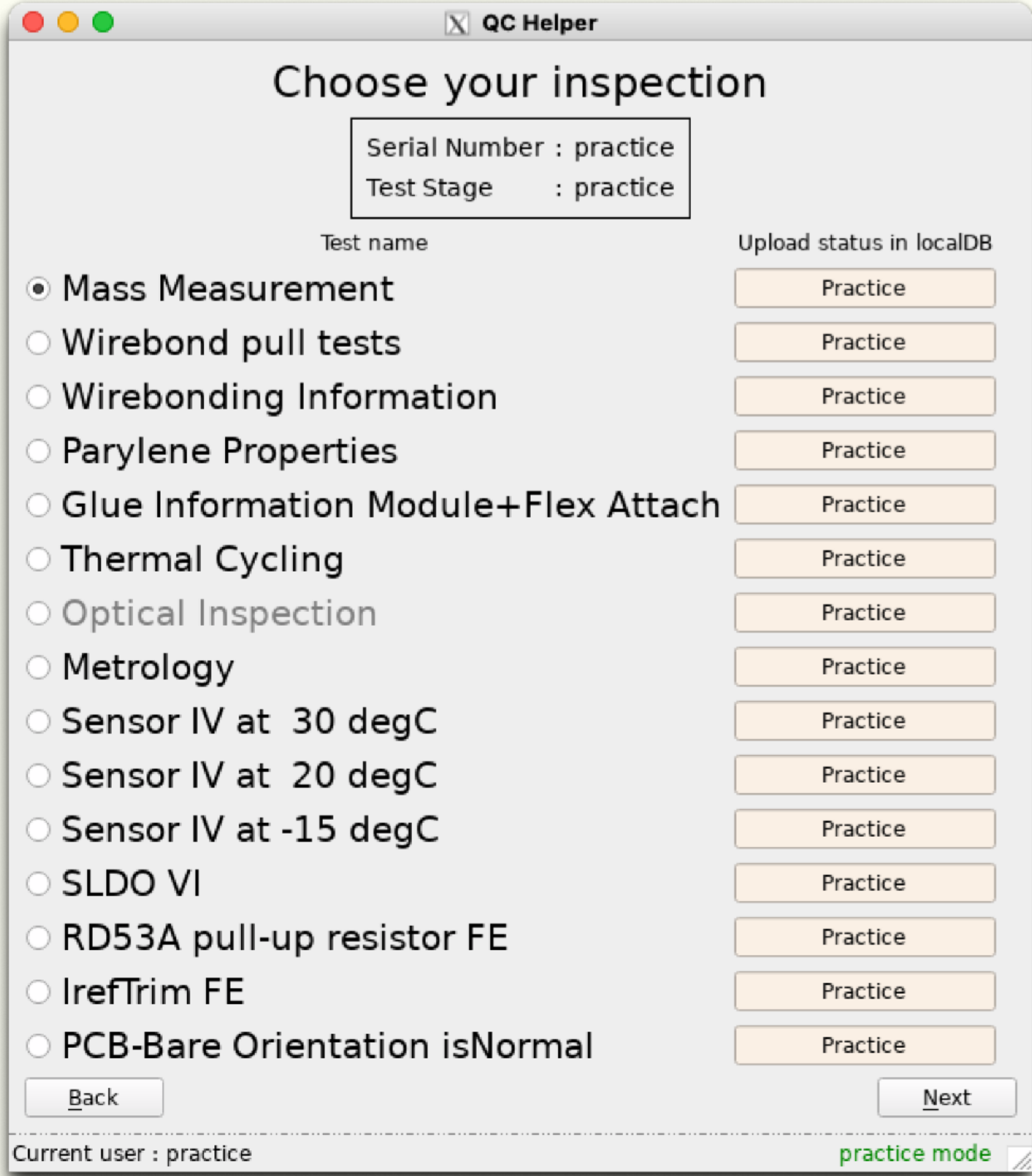
 **Grafana**: Open source analytics and interactive visualisation web application





# QC Helper

## Data uploader for non-electrical tests

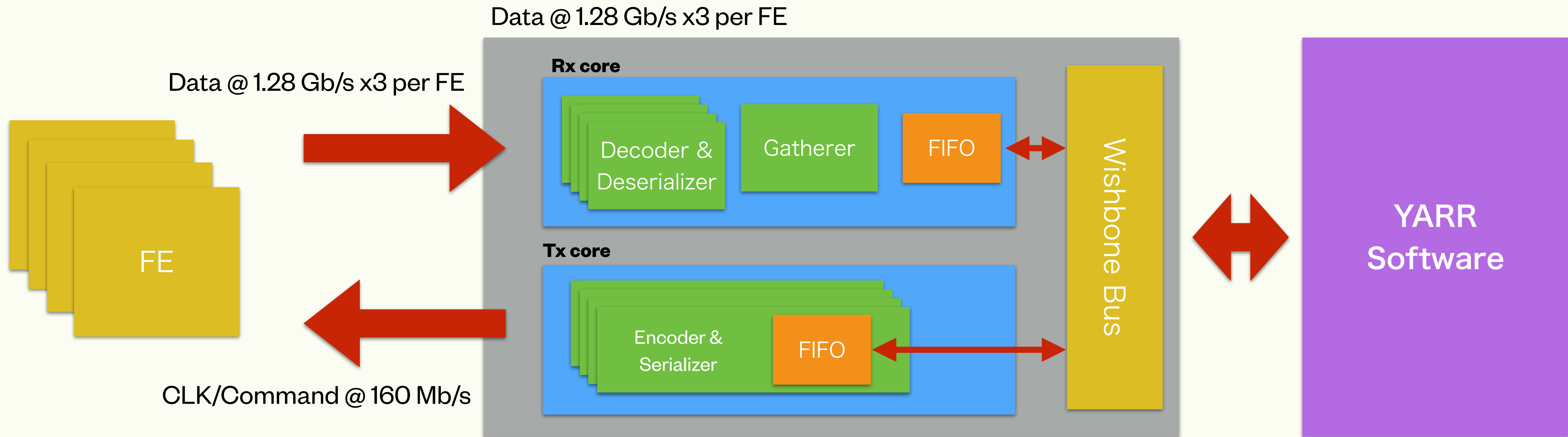


We're also trying to automatize visual inspection...



# YARR - DAQ system

- PCIe based high-speed DAQ system
  - FPGA just aggregates data from FE ASICs, everything sophisticated is done by its corresponding software

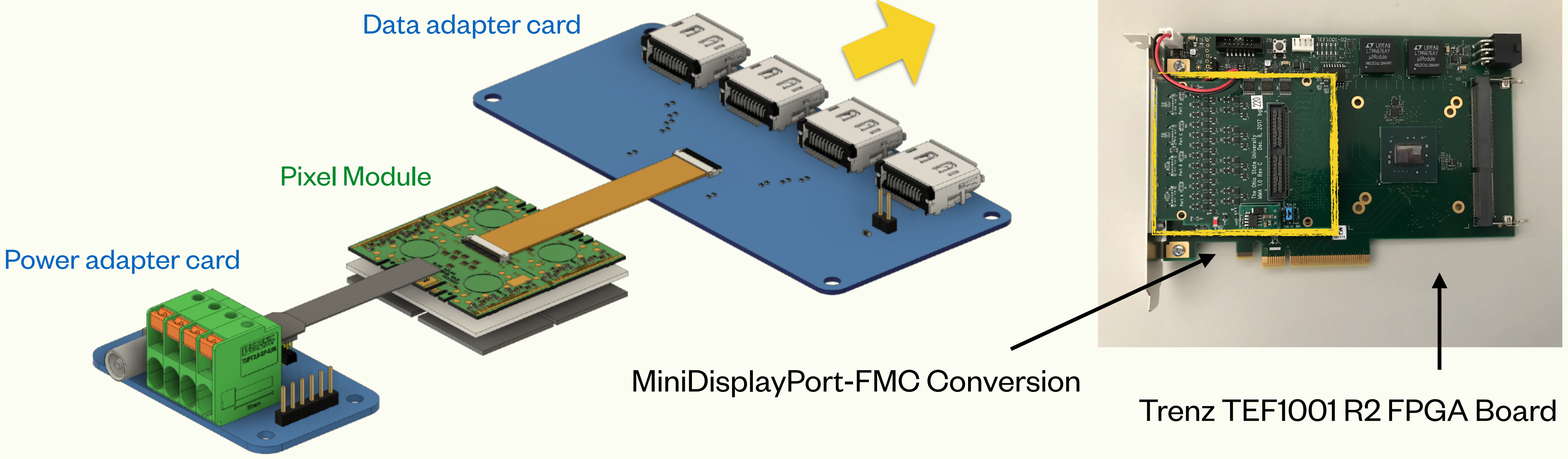




# RD53A Testing Setup



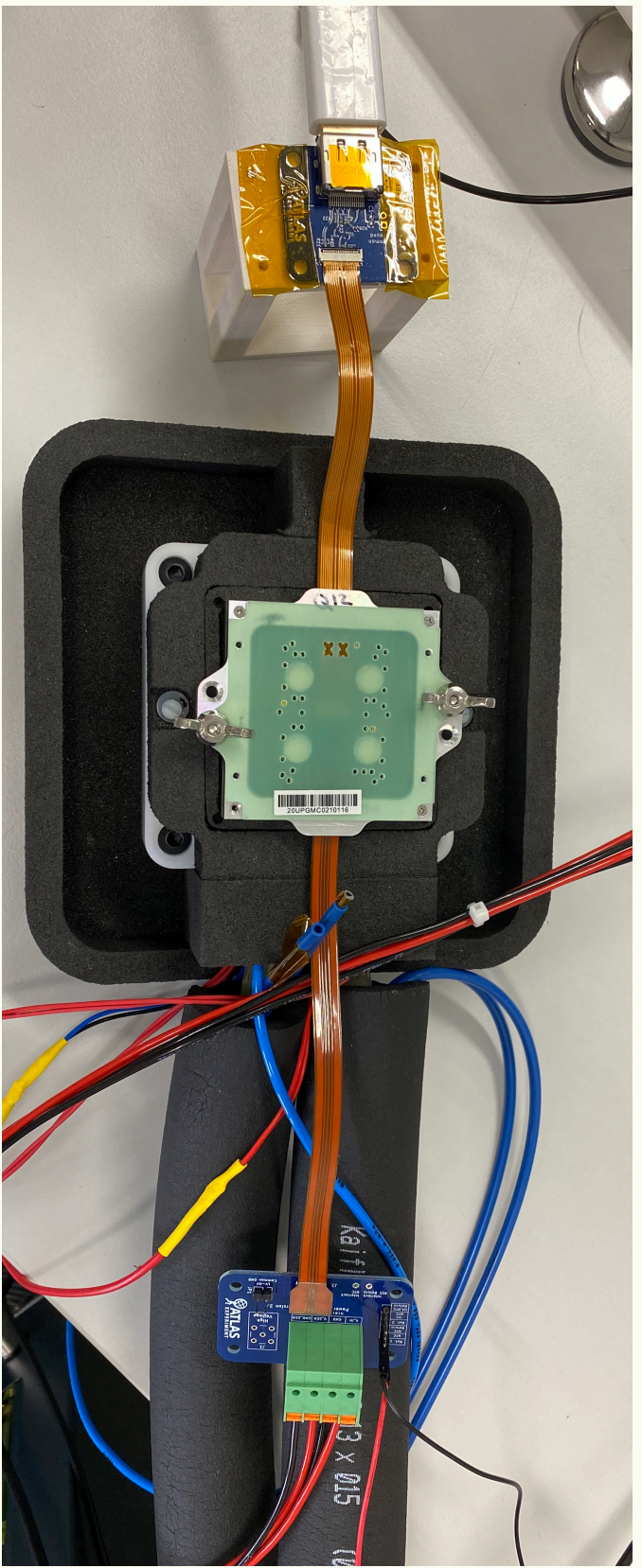
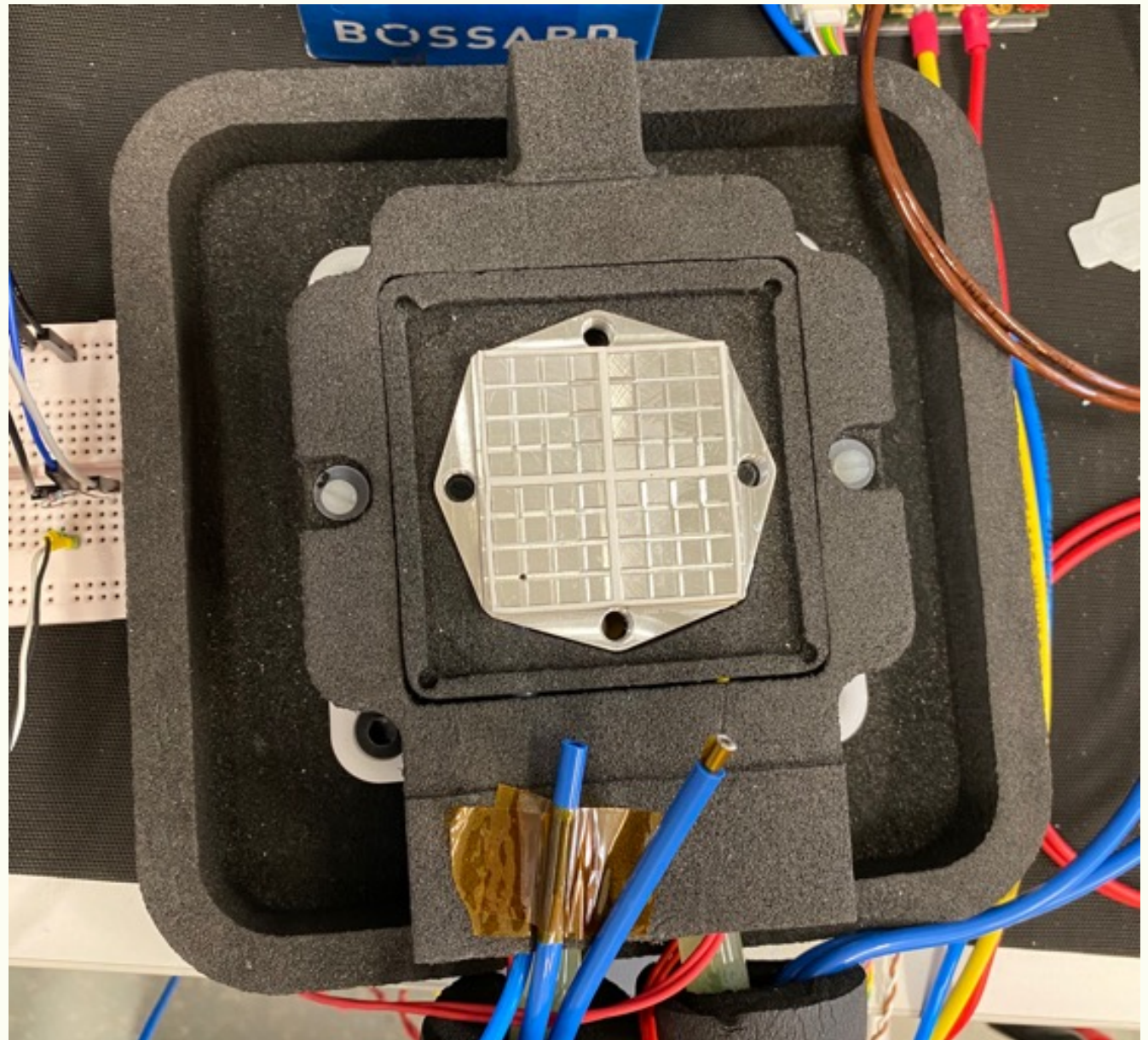
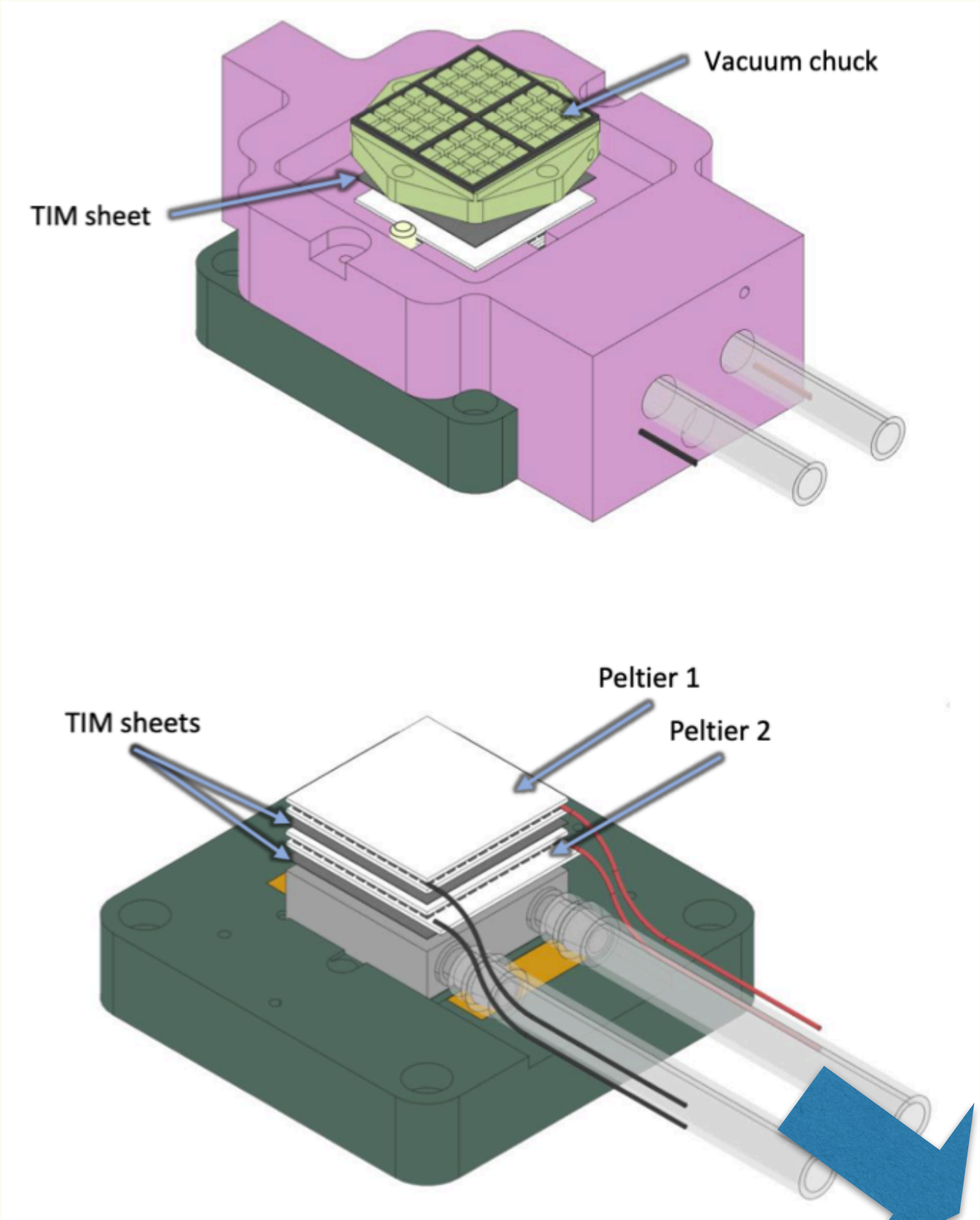
Data @ 1.28 Gb/s/lane





# RD53A Testing Setup

Cooling system for the quad module

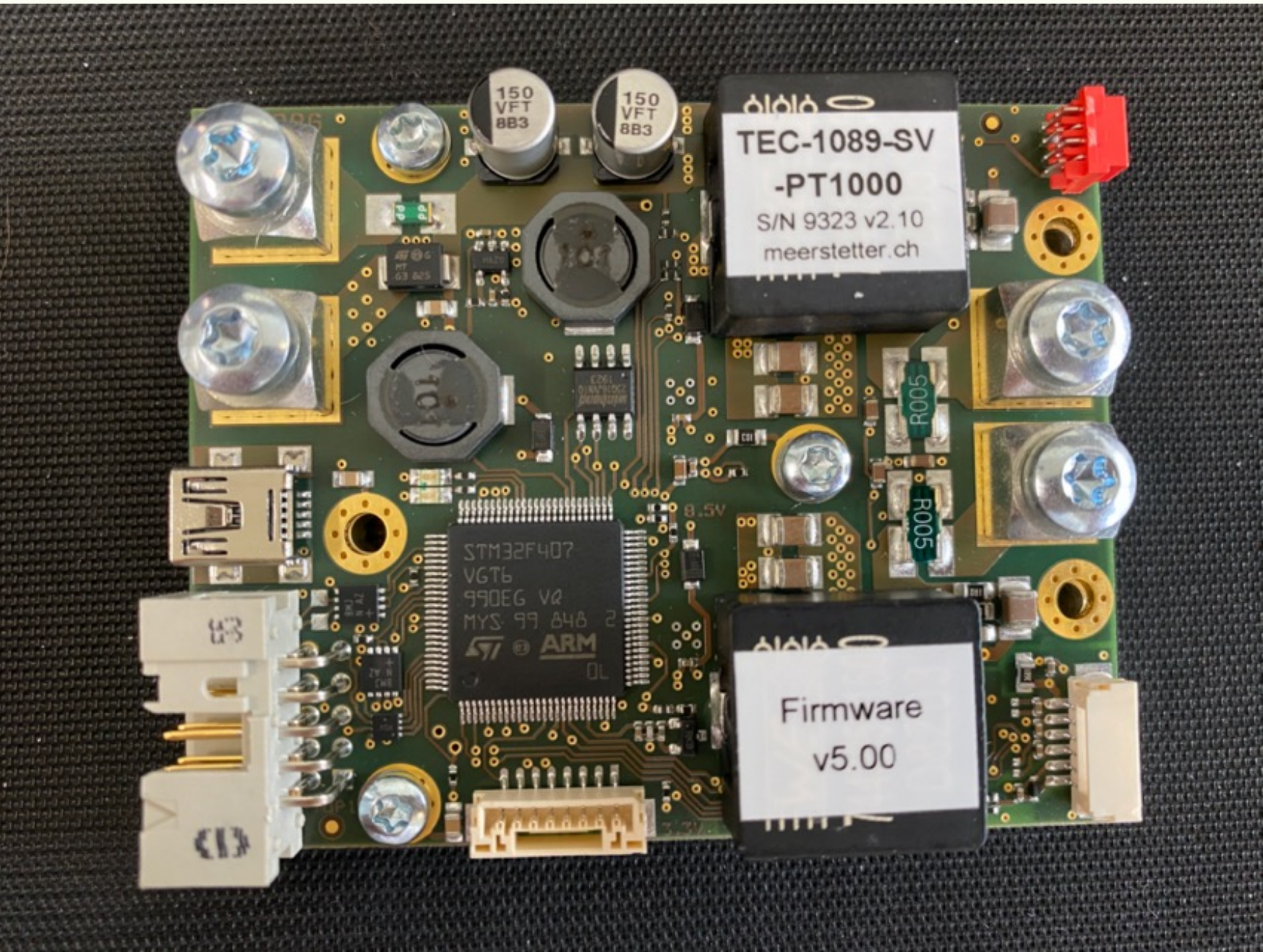


To Chiller



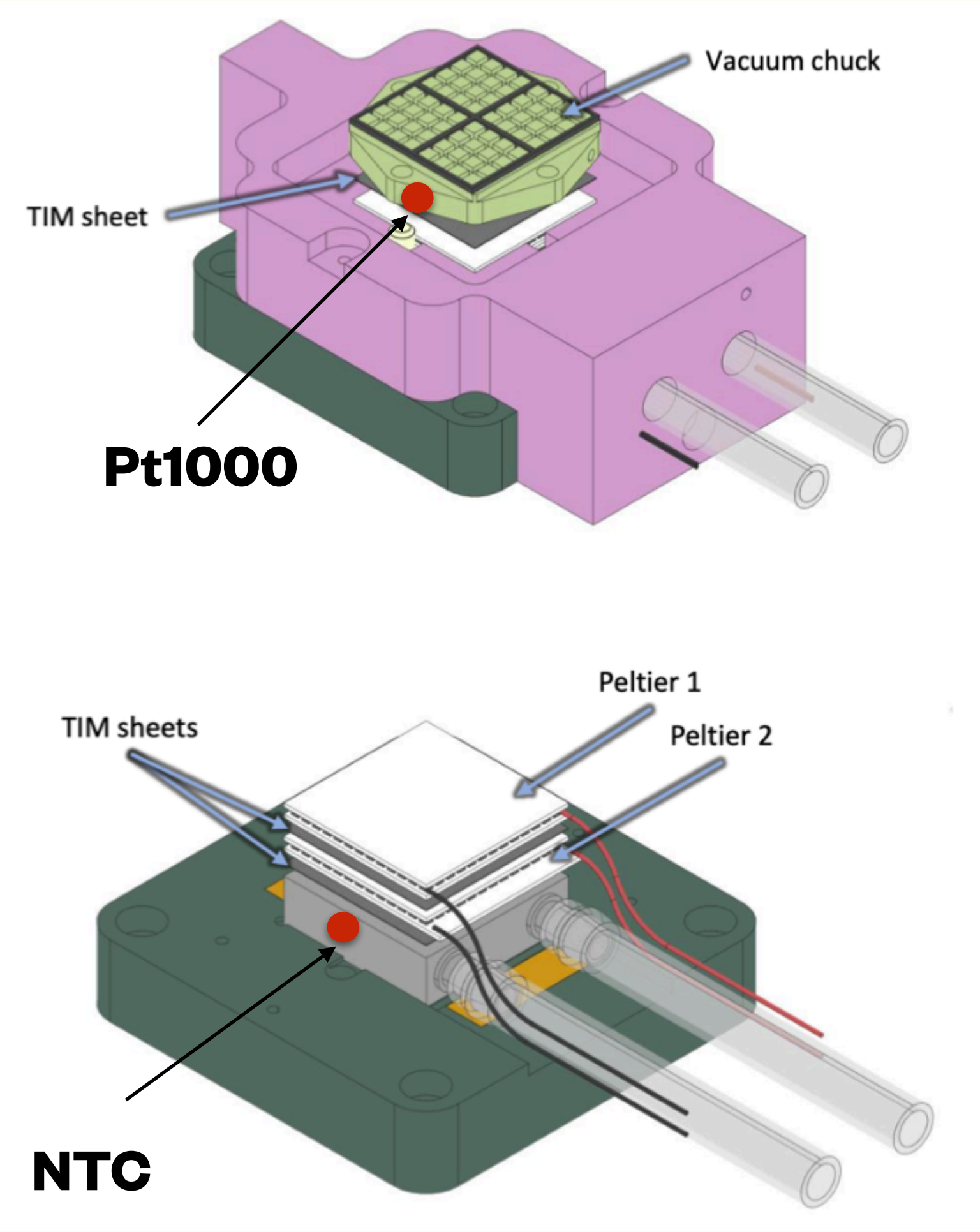
# Peltier Control and Temperature Monitoring

TEC-1089-SC-PT1000



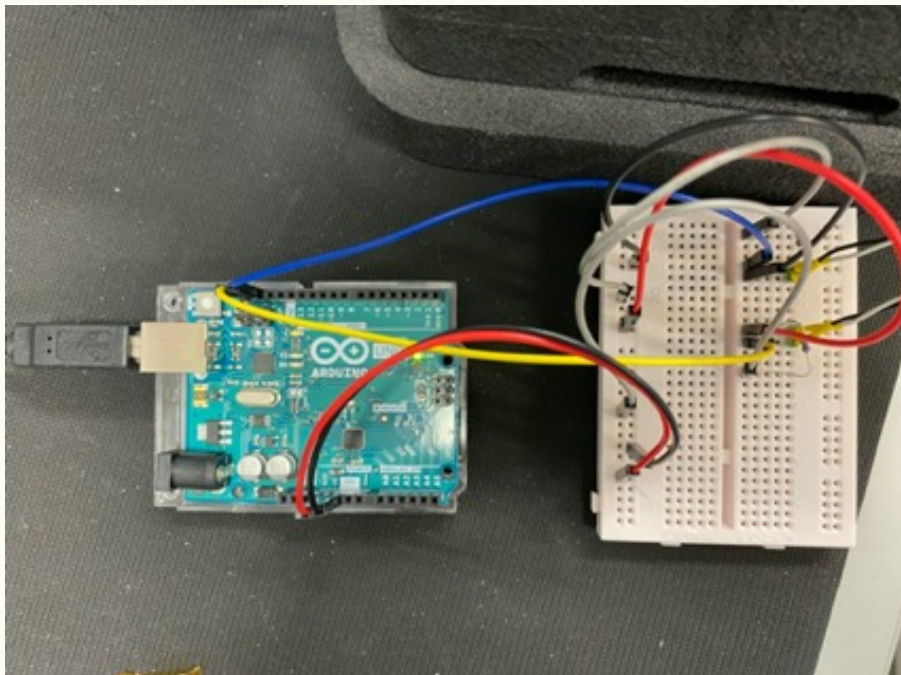
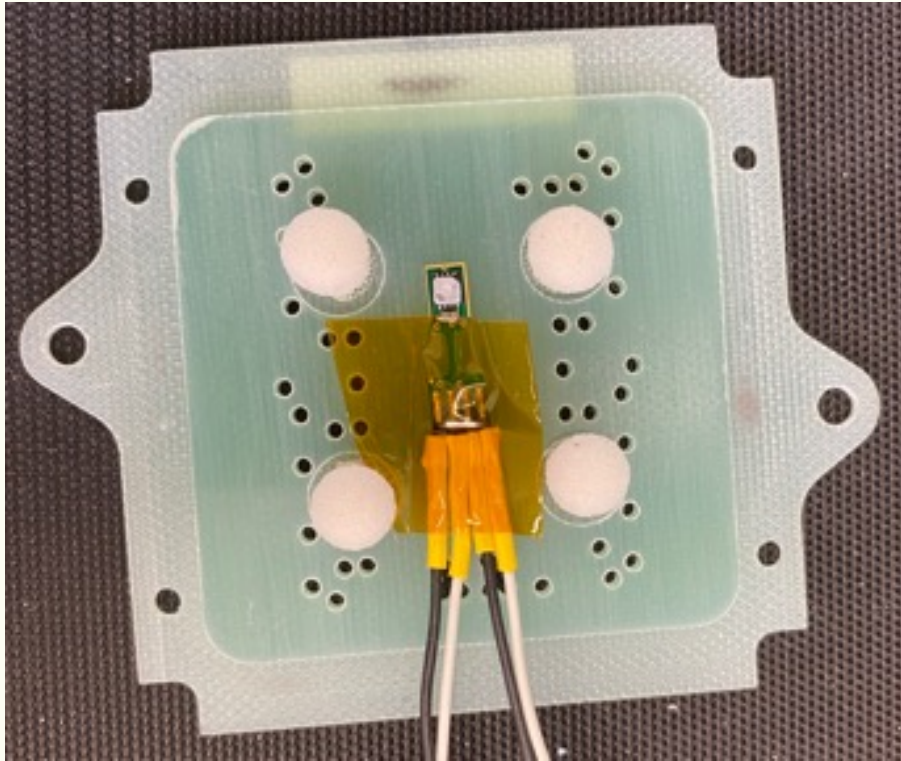
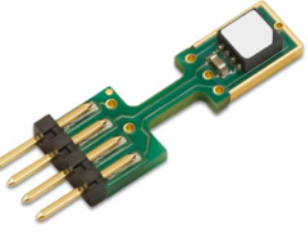
## PID Control

- Two temperature sensors as references
  - PT1000 for vacuum chuck
  - NTC for cold plate



SHT85

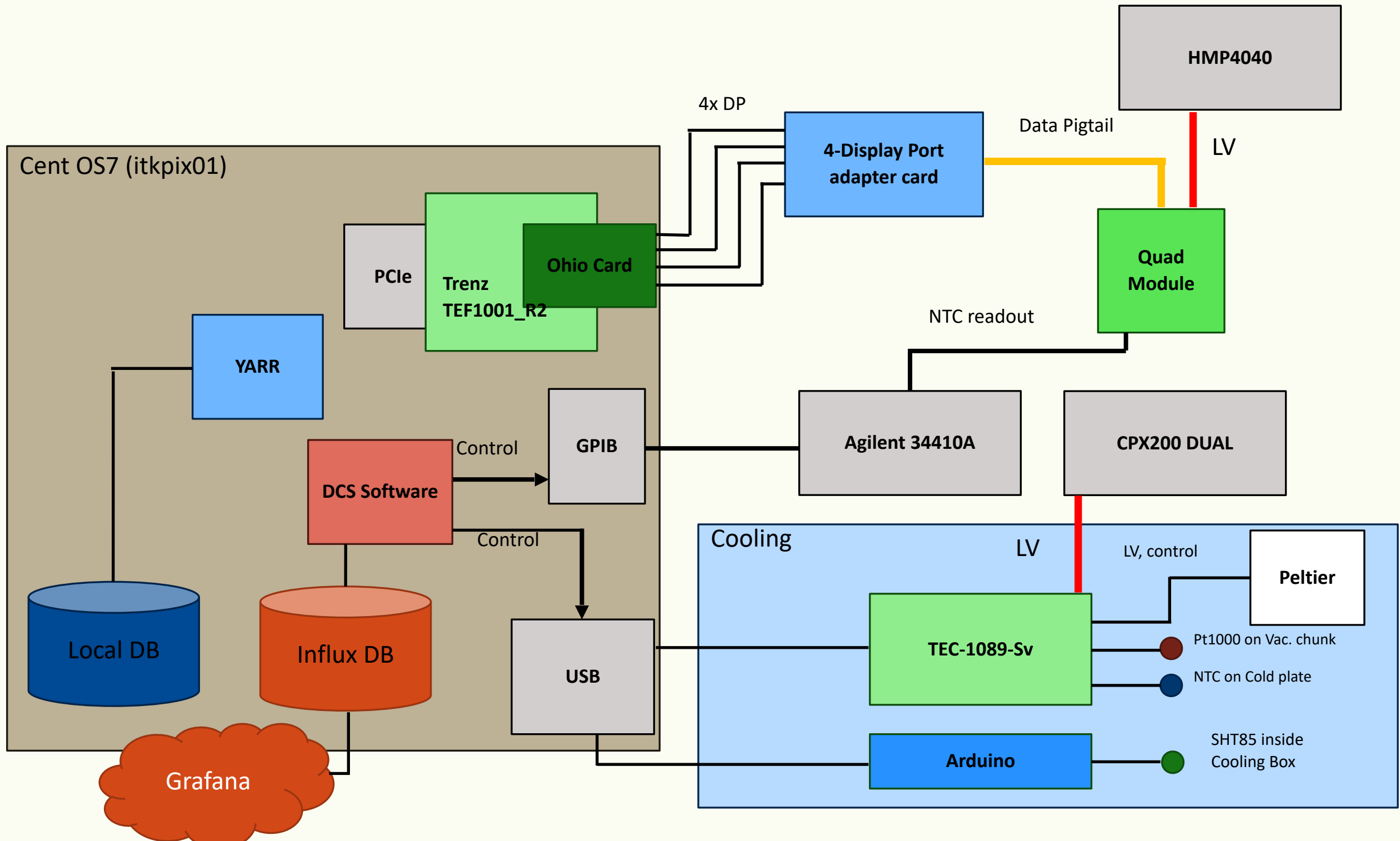
- High-accuracy RH&T sensor for demanding measurement & test applications
- Typical accuracy of  $\pm 1.5\%RH$  and  $\pm 0.1\text{ }^\circ C$
- Pin-type packaging for easy integration and replacement
- Fully calibrated, linearized, and temperature compensated digital output
- On-package membrane protected by exclusive license for several patents<sup>1</sup>



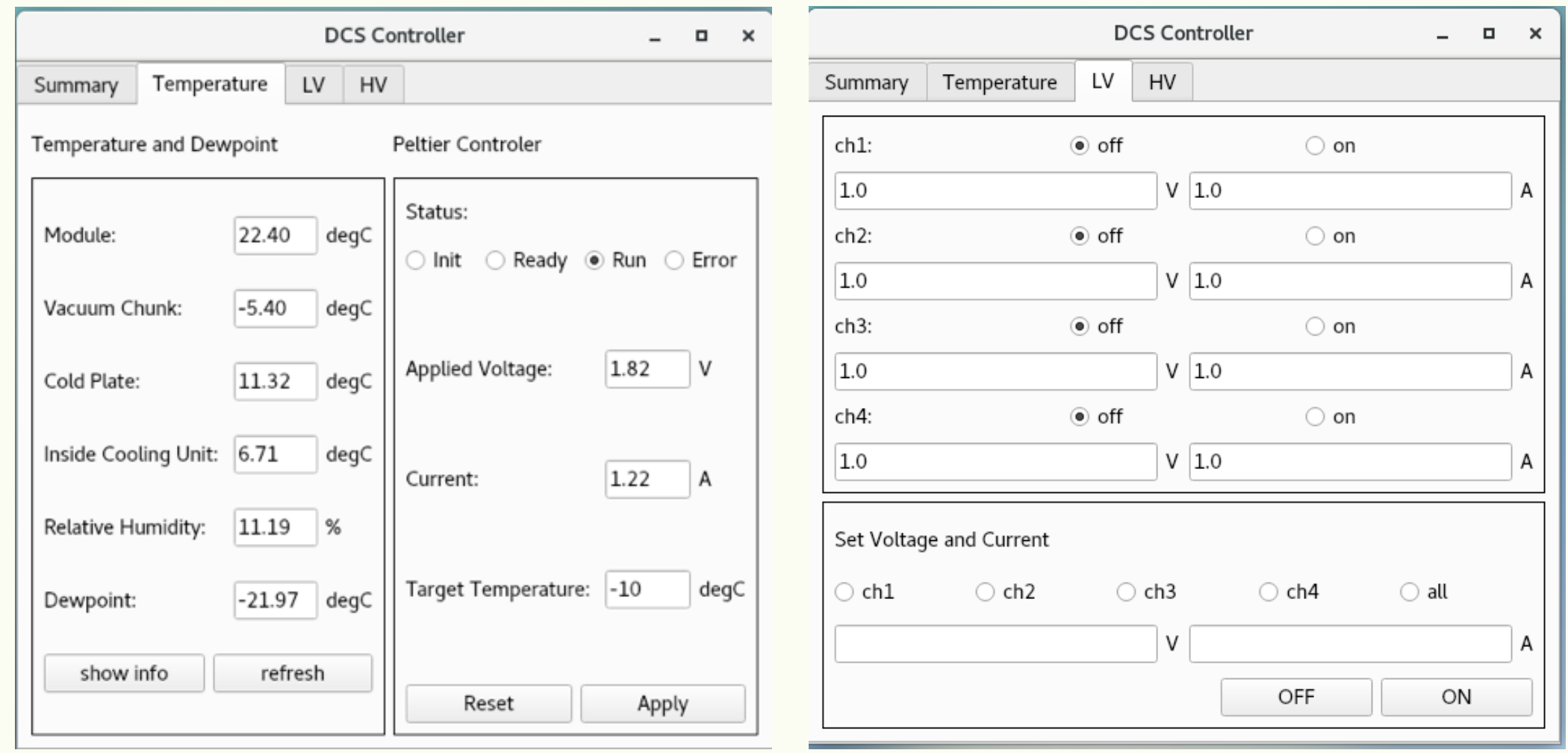


# Temperature Control and Monitoring

## Overview of testing setup @ UniGe



## Controlled by GUI

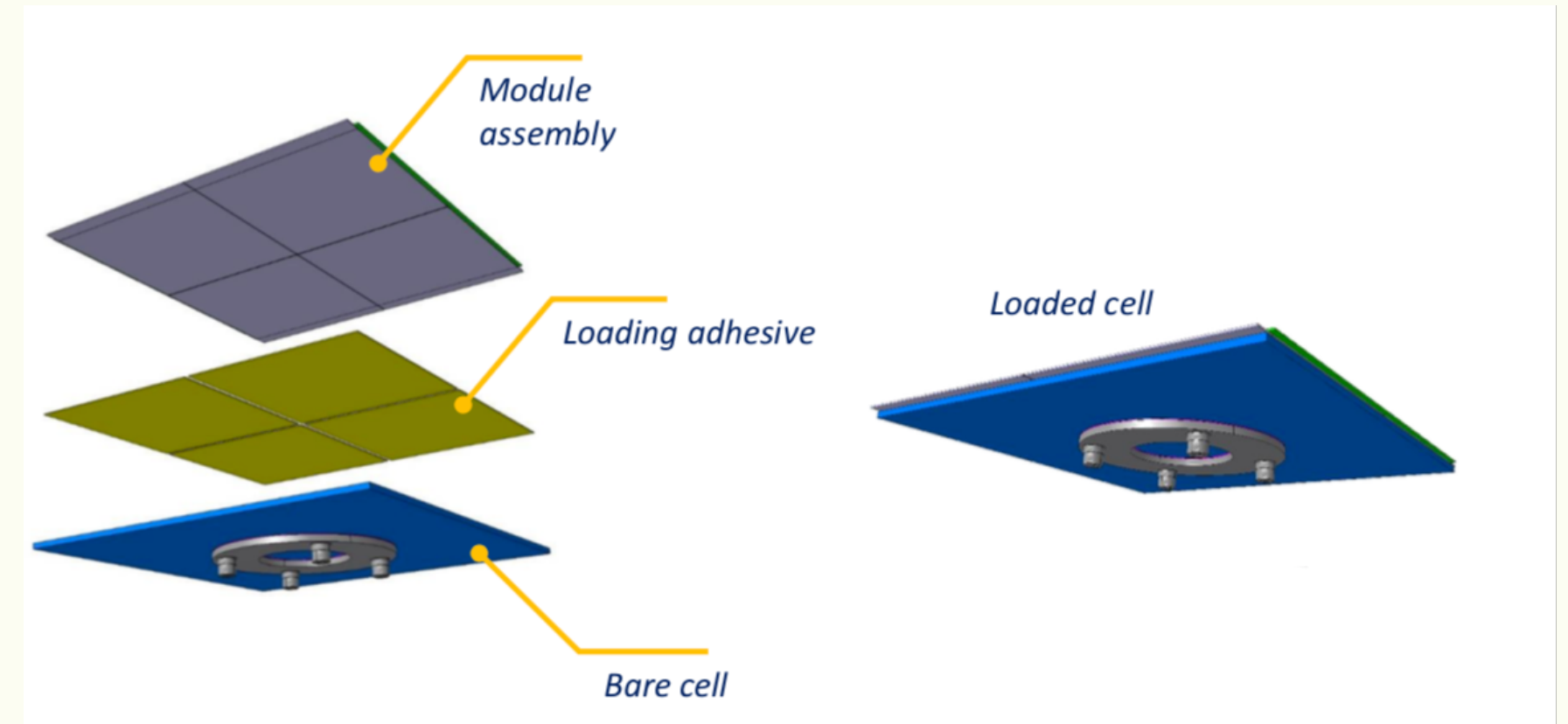
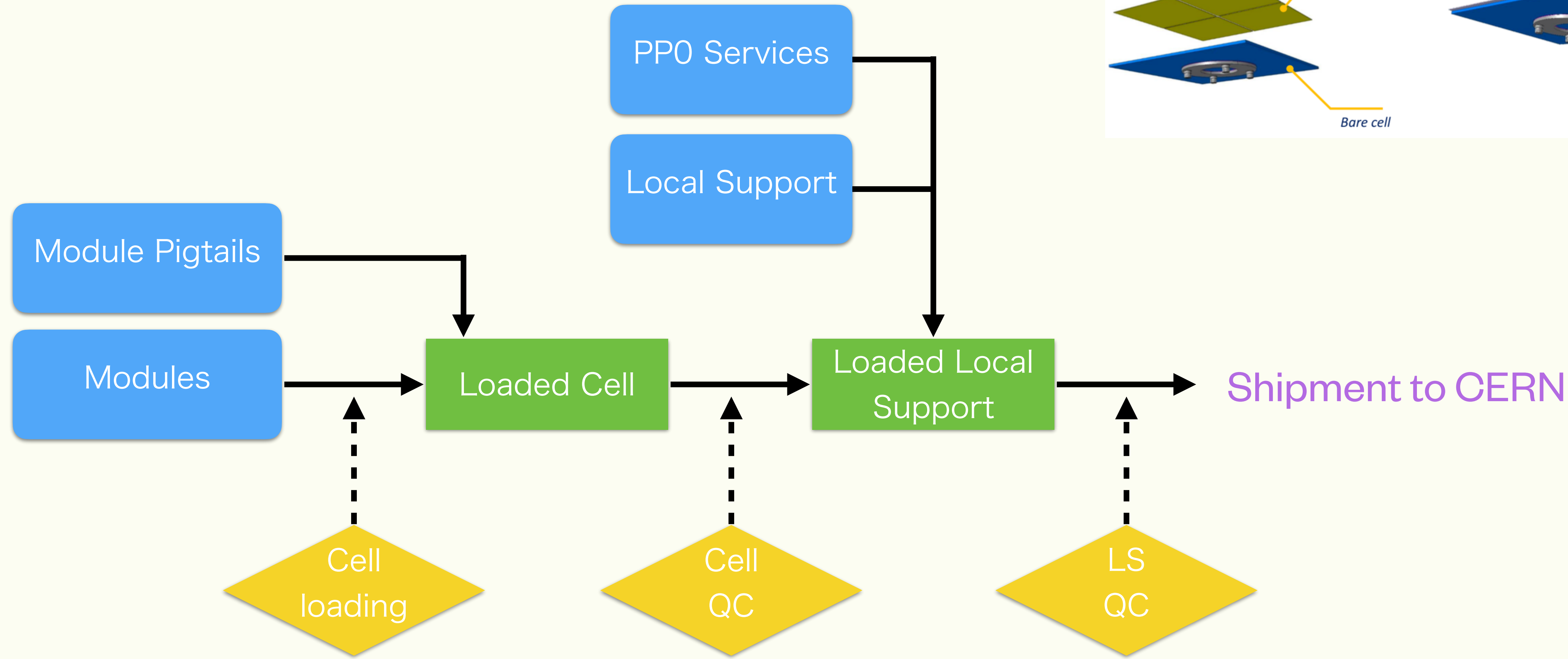


## Monitored by Grafana (recorded in the influxDB)





# Loaded Cell Module

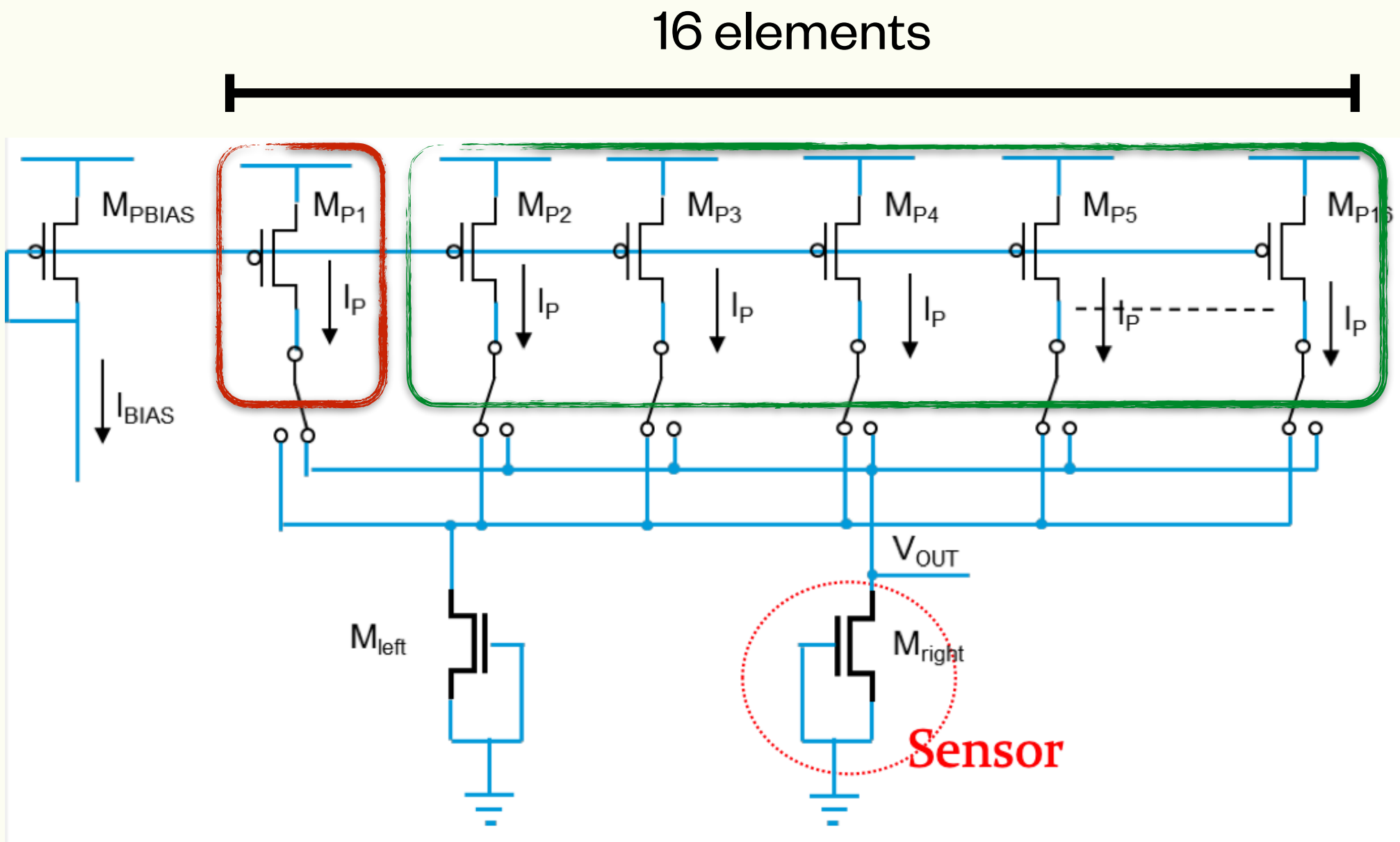
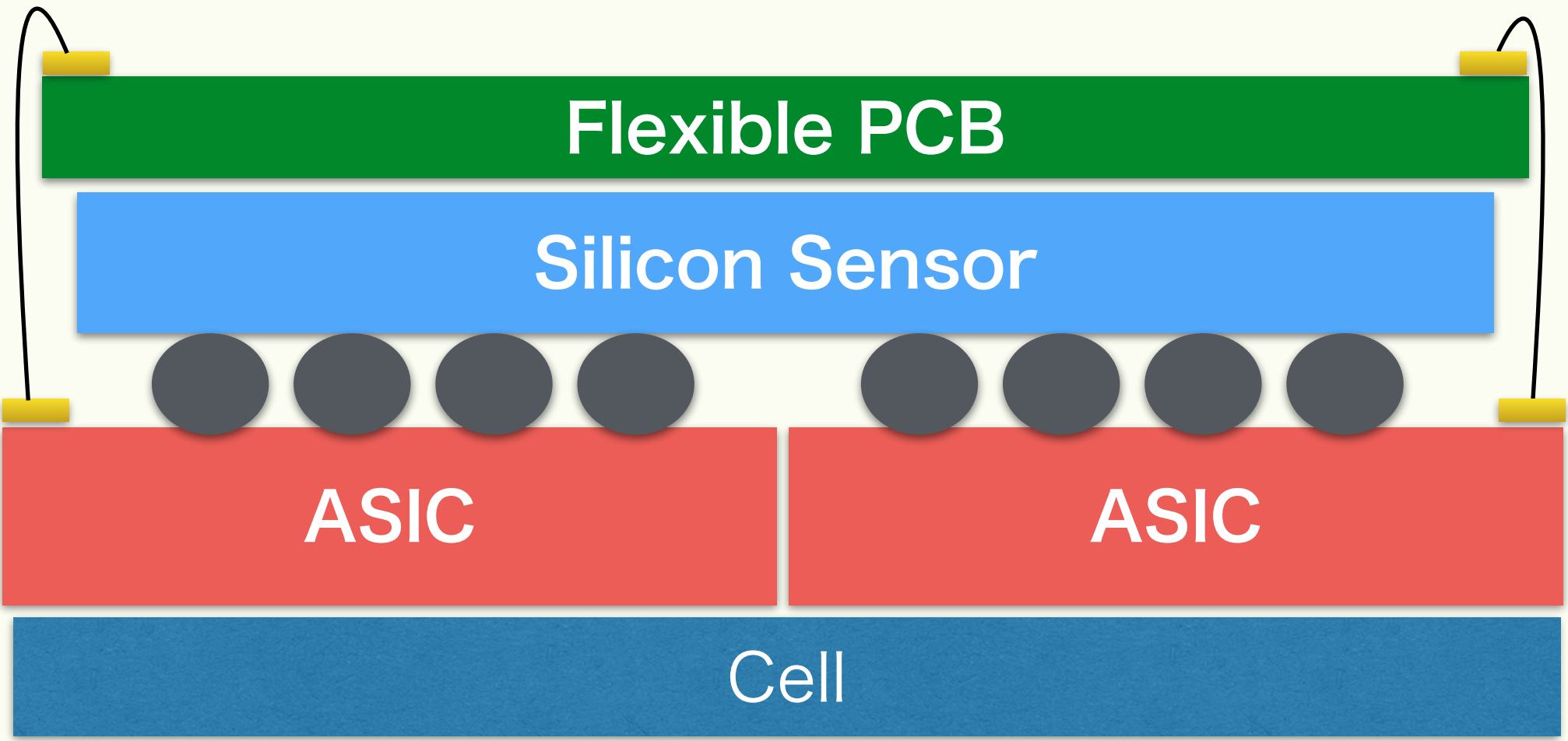




# Module Temperature

## Temperature Sensors of the Module

- 2 NTCs on the PCB
- 4 NMOS temperature sensors in each ASIC
  - ➔ These sensors are available only when chip turns on



$$\Delta V = N_f \times \frac{kT}{q} \times \ln R$$

$$V_1 = M_{right} \text{ Biased at } 1 \times I_p$$

$$V_2 = M_{right} \text{ Biased at } 15 \times I_p$$

$$\Delta V = V_2 - V_1$$

How to calibrate temperature sensors in the ASIC?

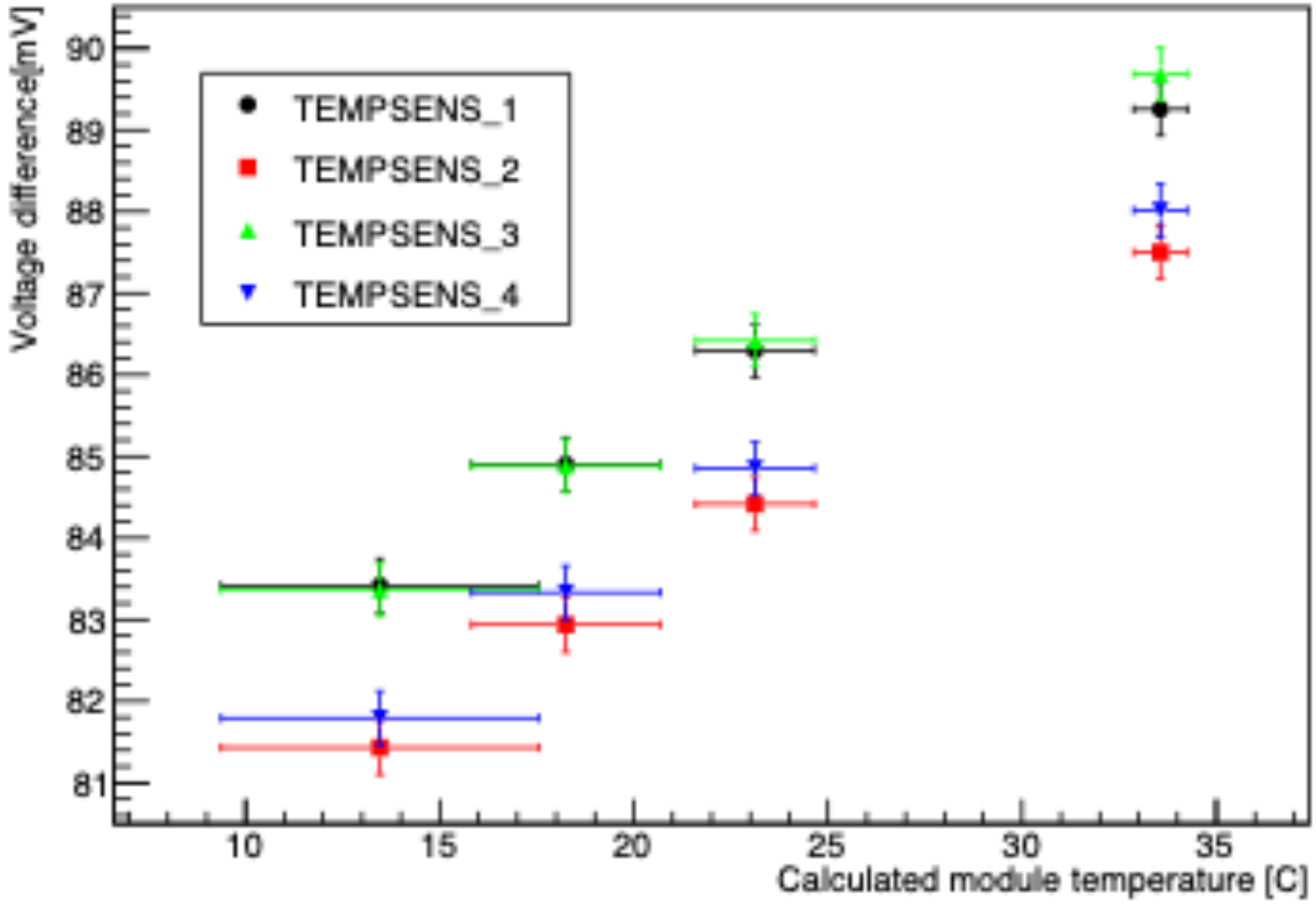
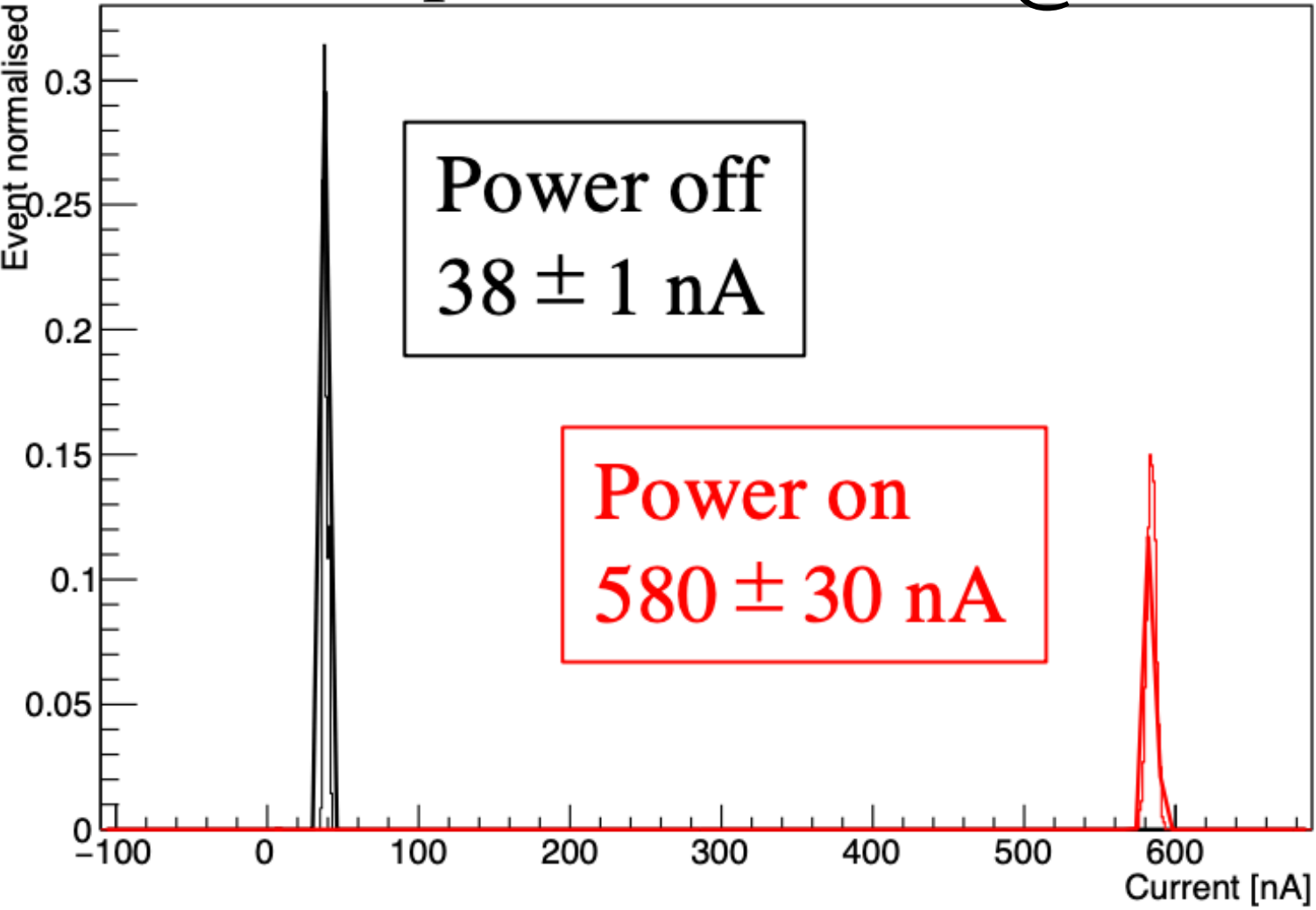


# Temperature Sensor Calibration

Leakage current of a silicon sensor depends on its temperature

$$\frac{I(T_2)}{I(T_1)} = \left(\frac{T_2}{T_1}\right)^2 e^{-\frac{E_g(T_2)}{2kT_2} + \frac{E_g(T_1)}{2kT_1}}, E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}$$

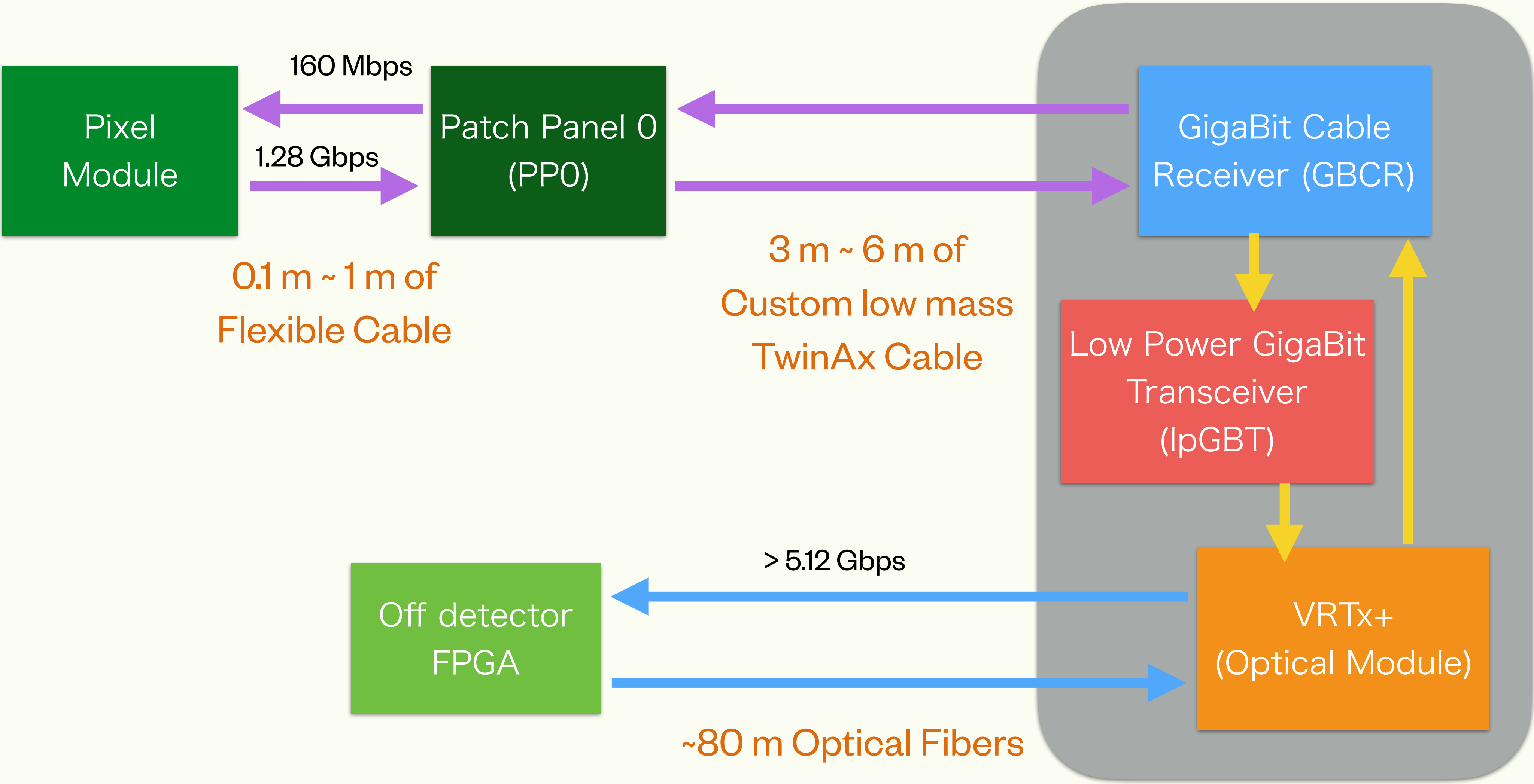
In the climate chamber @ 0 C



Able to calibrate each sensor with the accuracy of ± 1.3 C



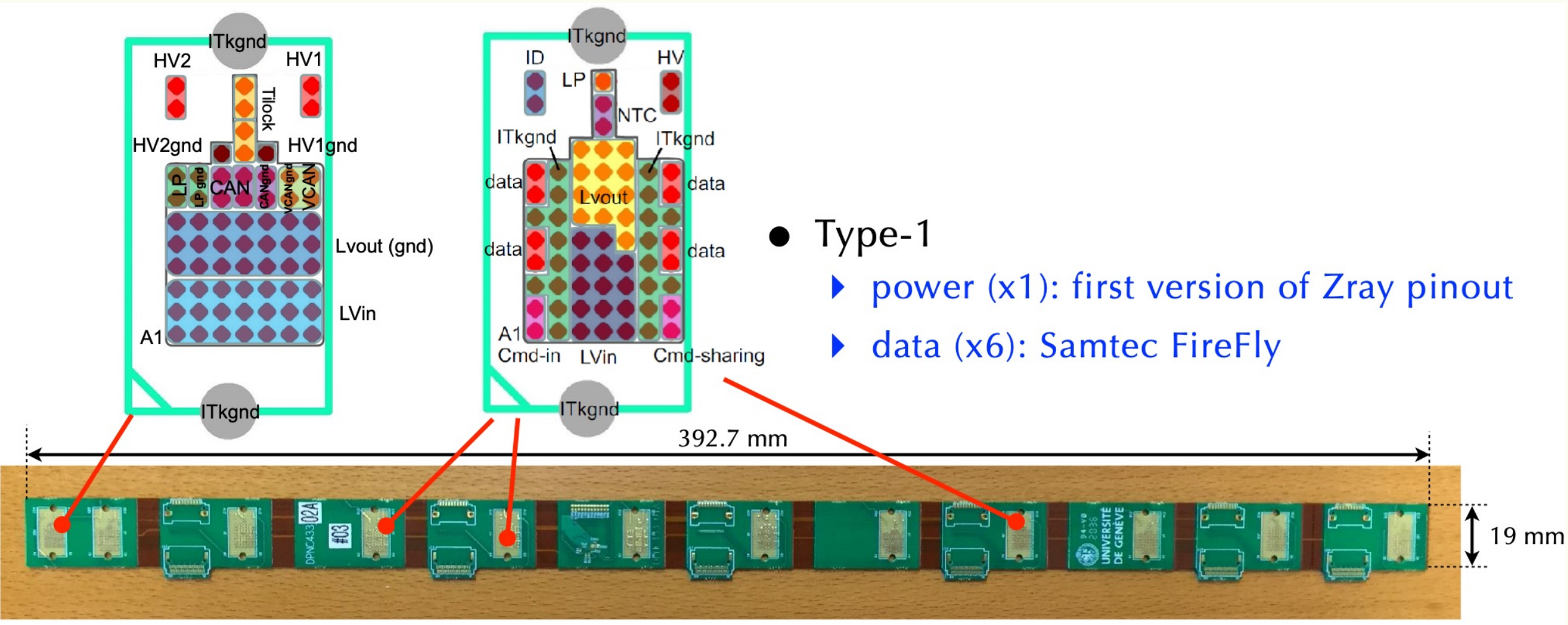
# Upstream Data Transmission



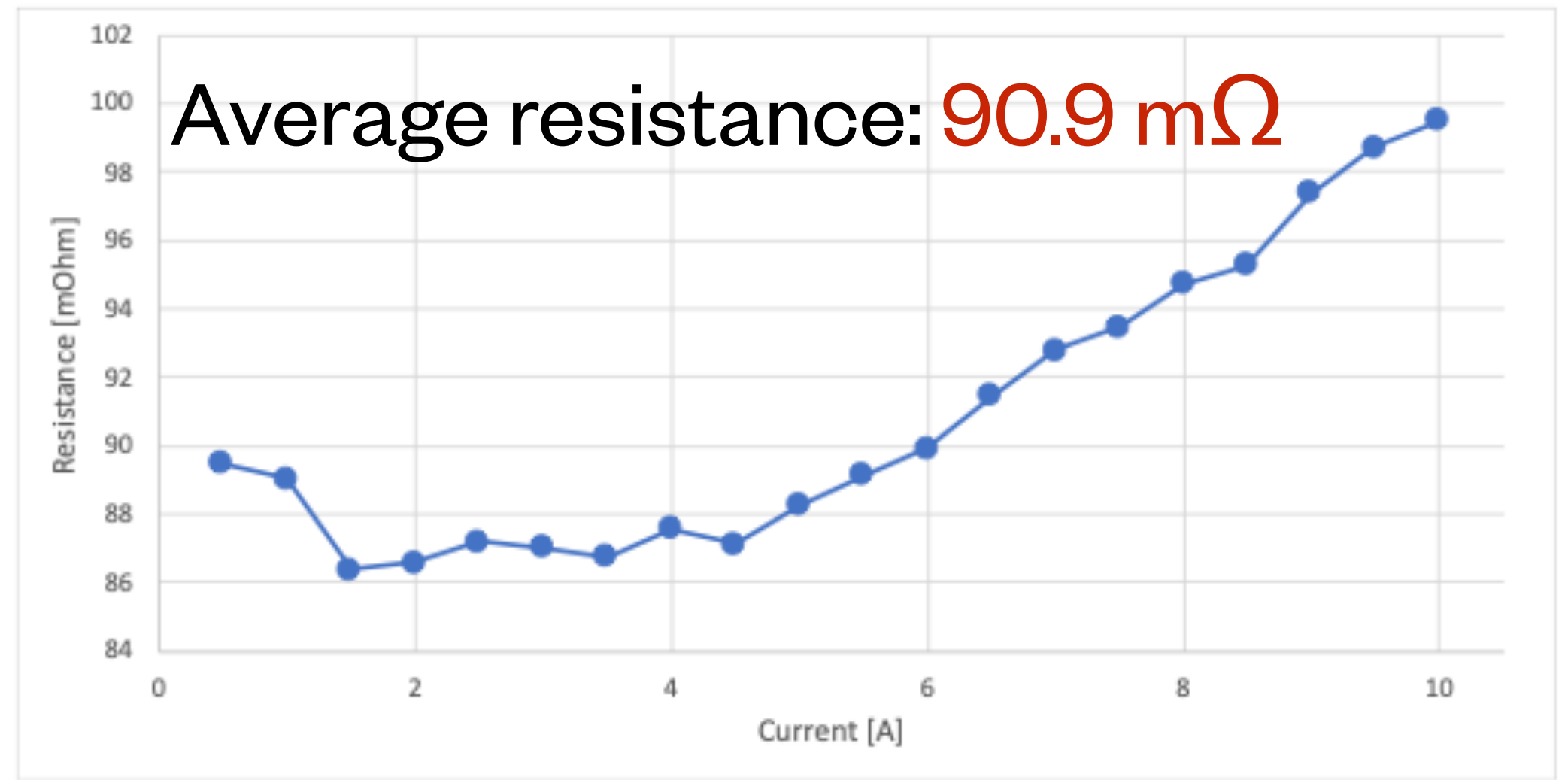
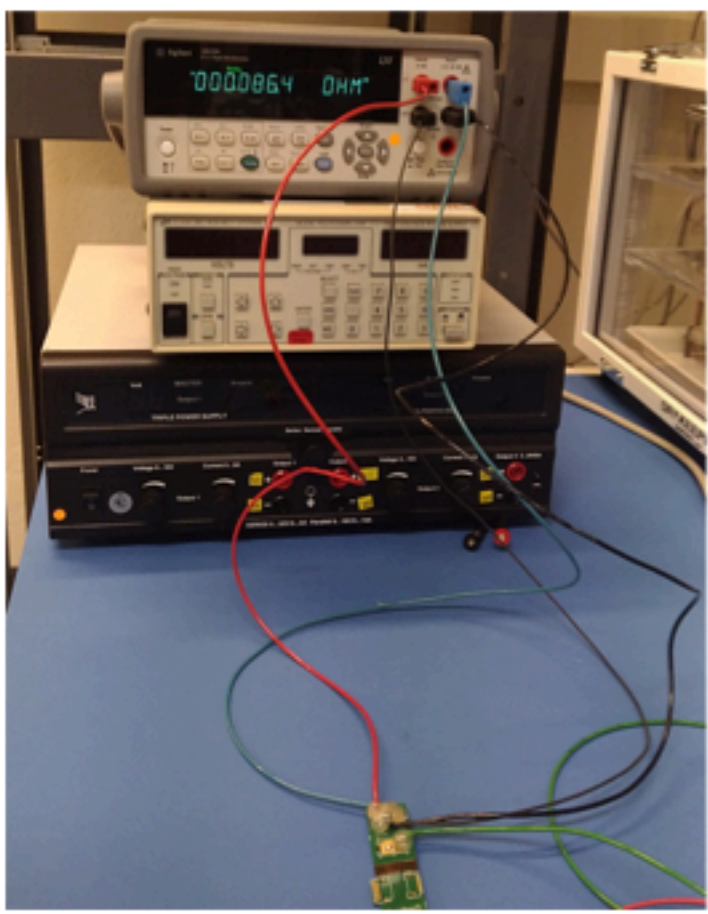
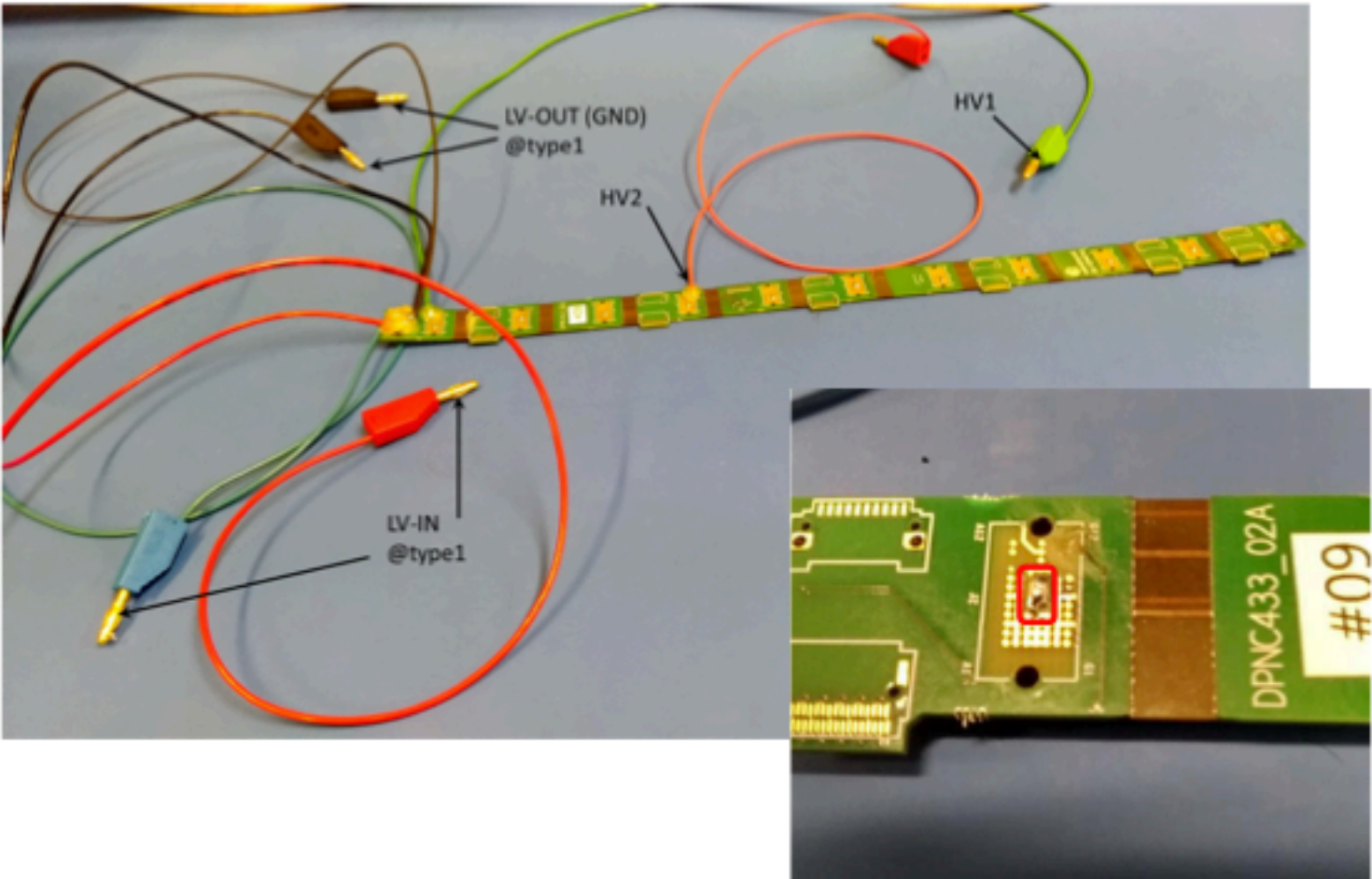


# PP0 Prototype

- First inclined PP0 prototype
  - based on design done for services PDR
  - Adapted from L4 to L3



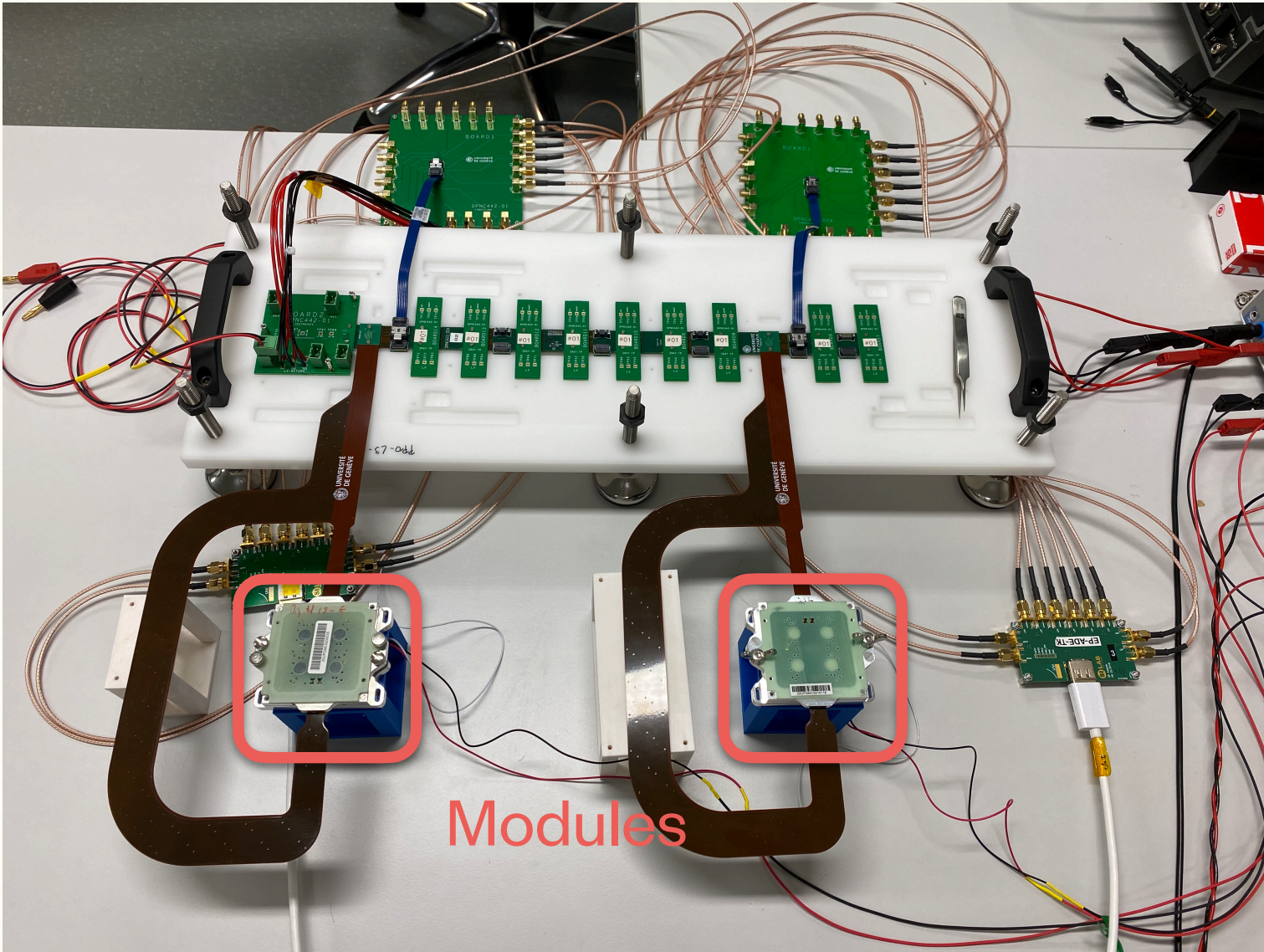
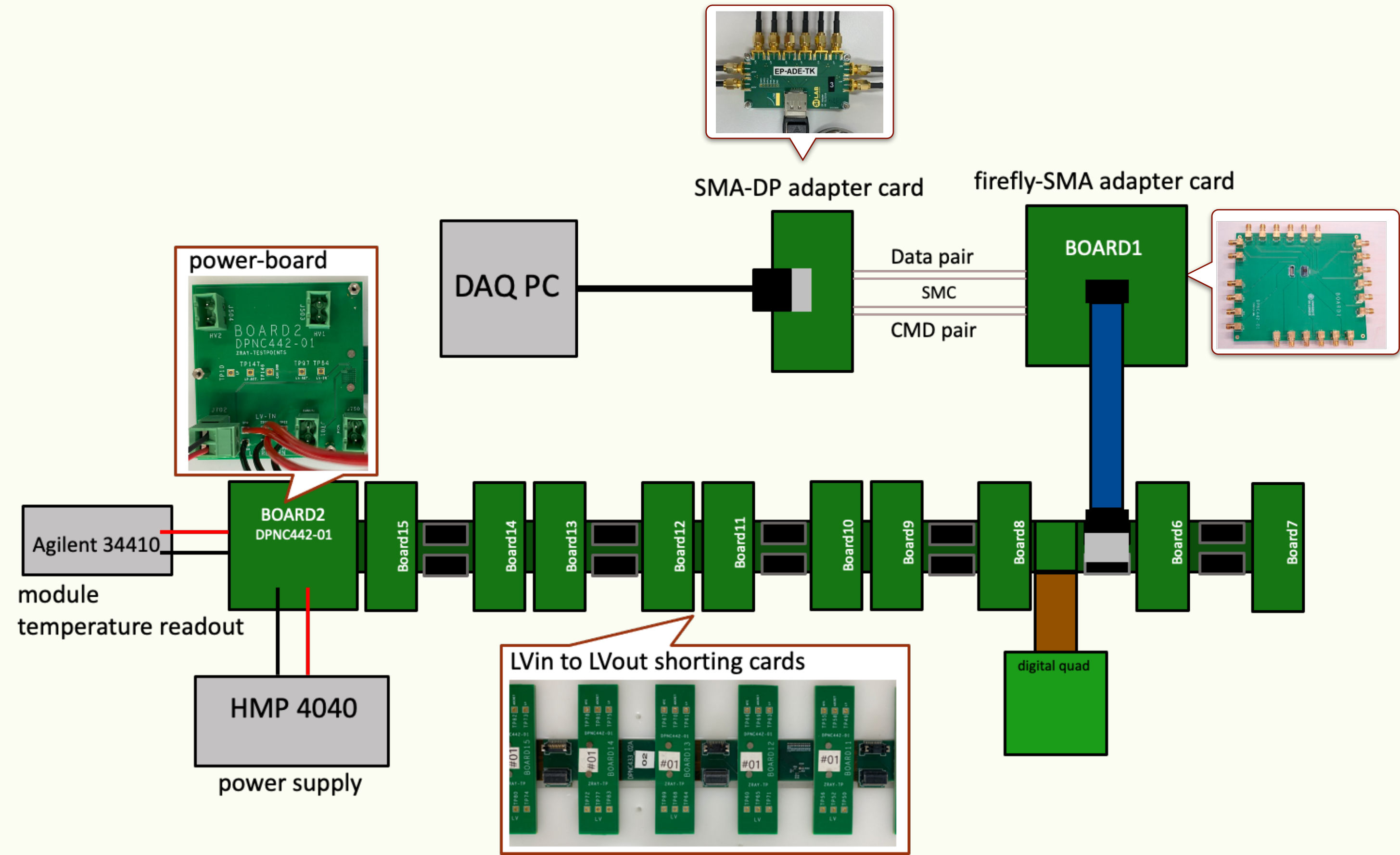
## LV round-trip resistance





# Readout Test for PPO Prototype

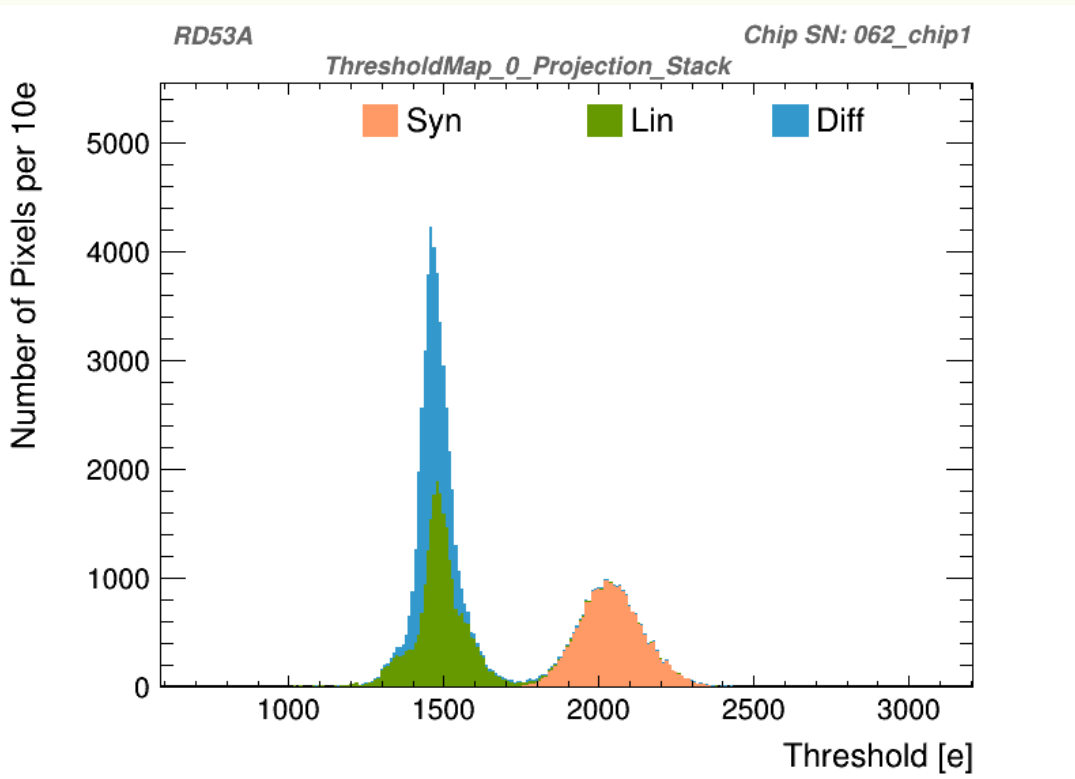
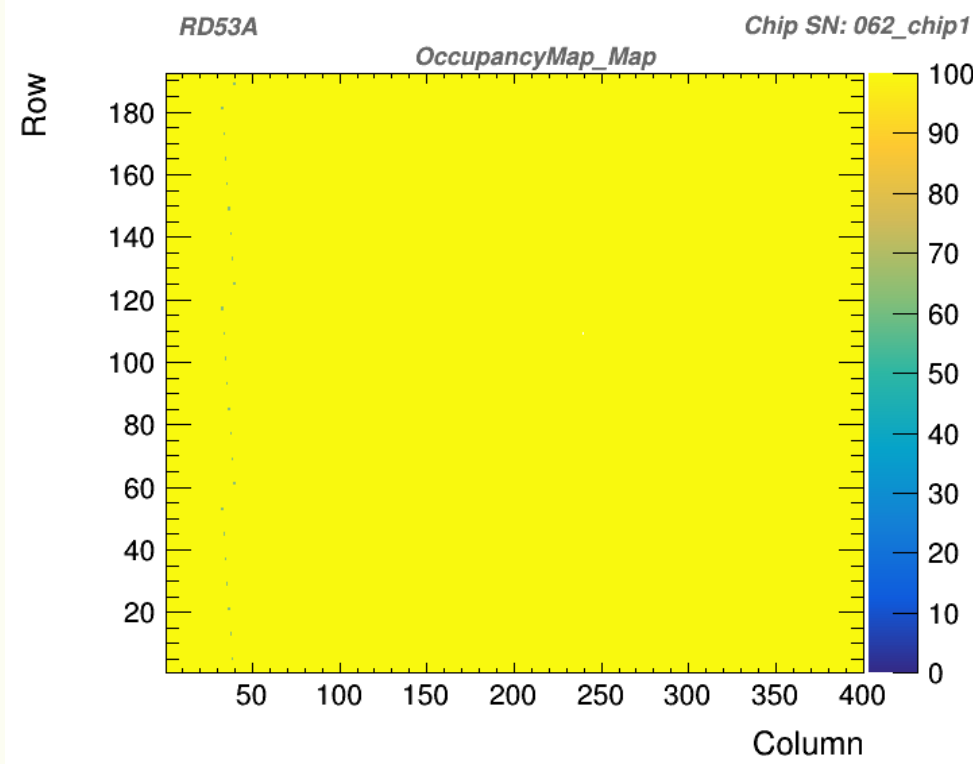
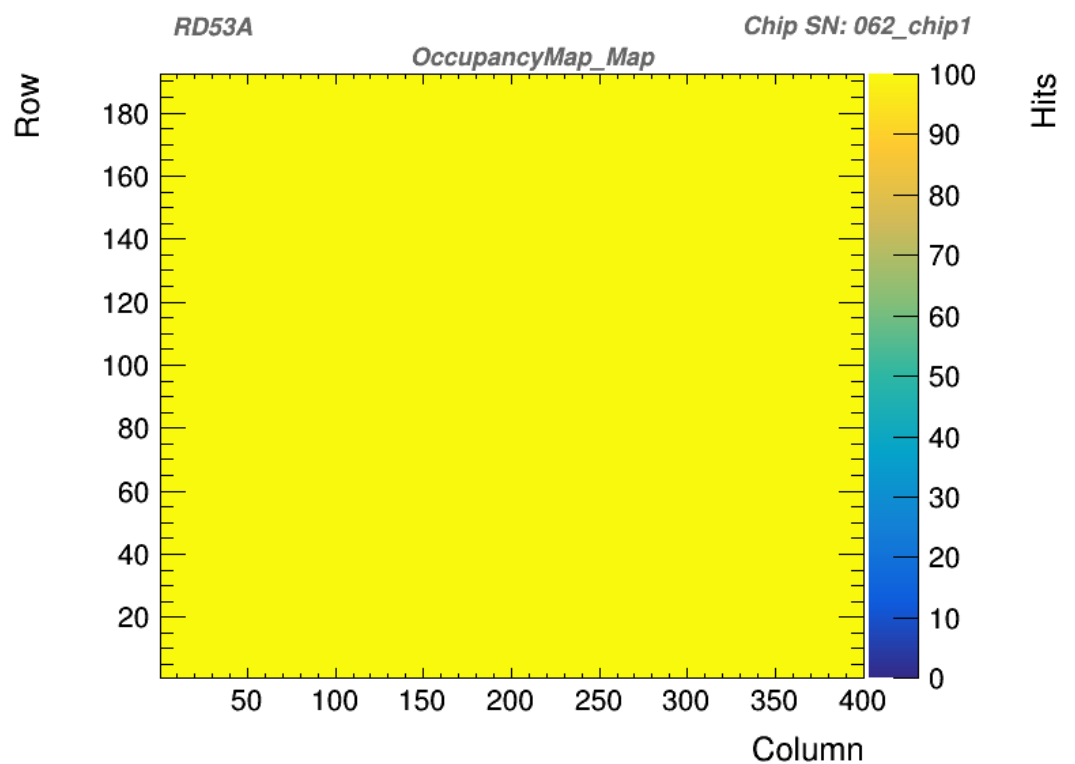
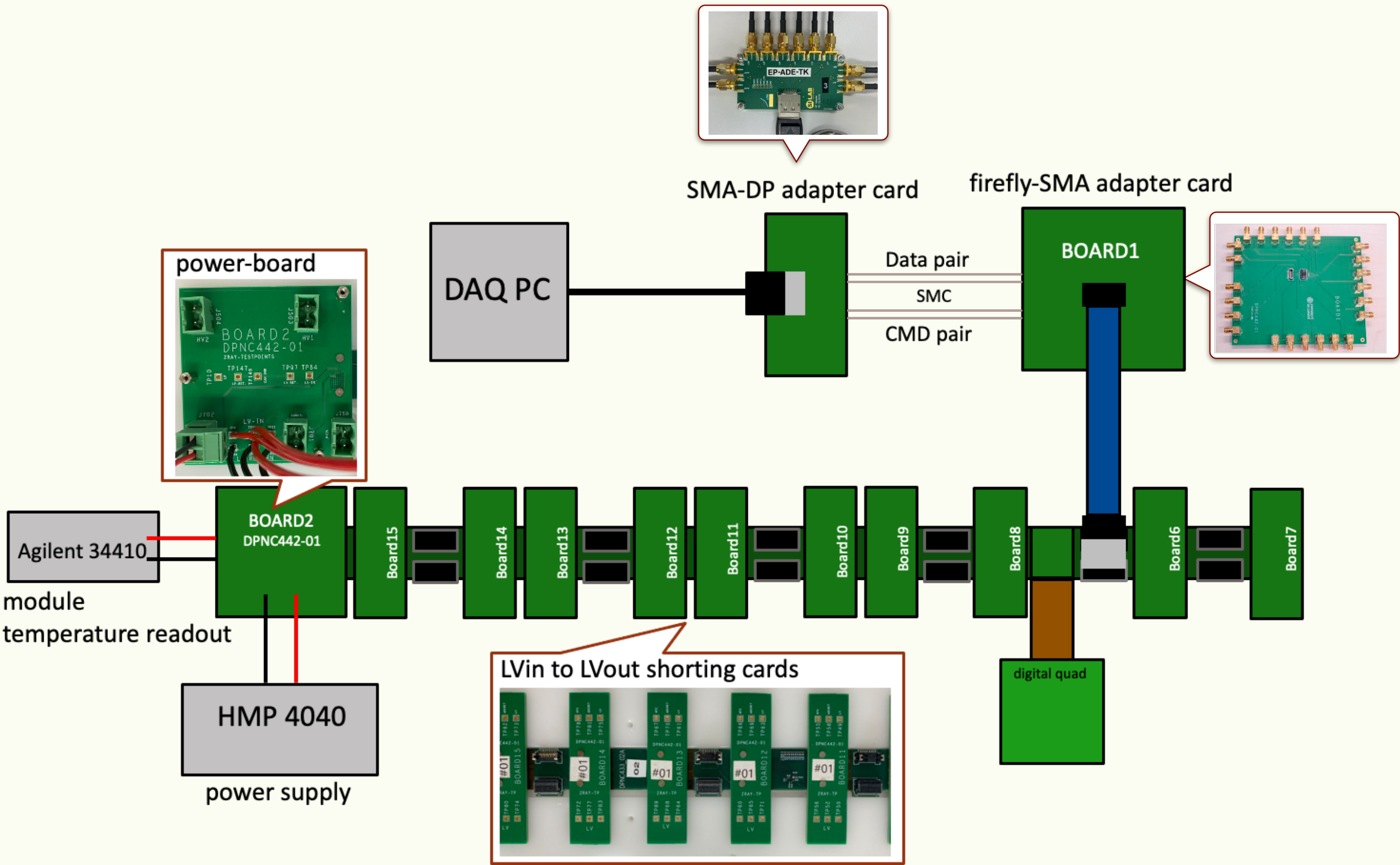
- Testing with 2 quad modules





# Readout Test for PPO Prototype

- Testing with 2 quad modules



Get equivalent results as module stand alone test



# Conclusion

- There are many activities toward Phase-II ATLAS ITk Upgrade
  - Preparing for the mass production of Pixel detector
  - Testing setup, procedure, database, and so on...
- Real production phase is approaching!!

Thank you for your attention!!

ご清聴有り難うございました。