ATLAS ITk-Pixel Detector Overview

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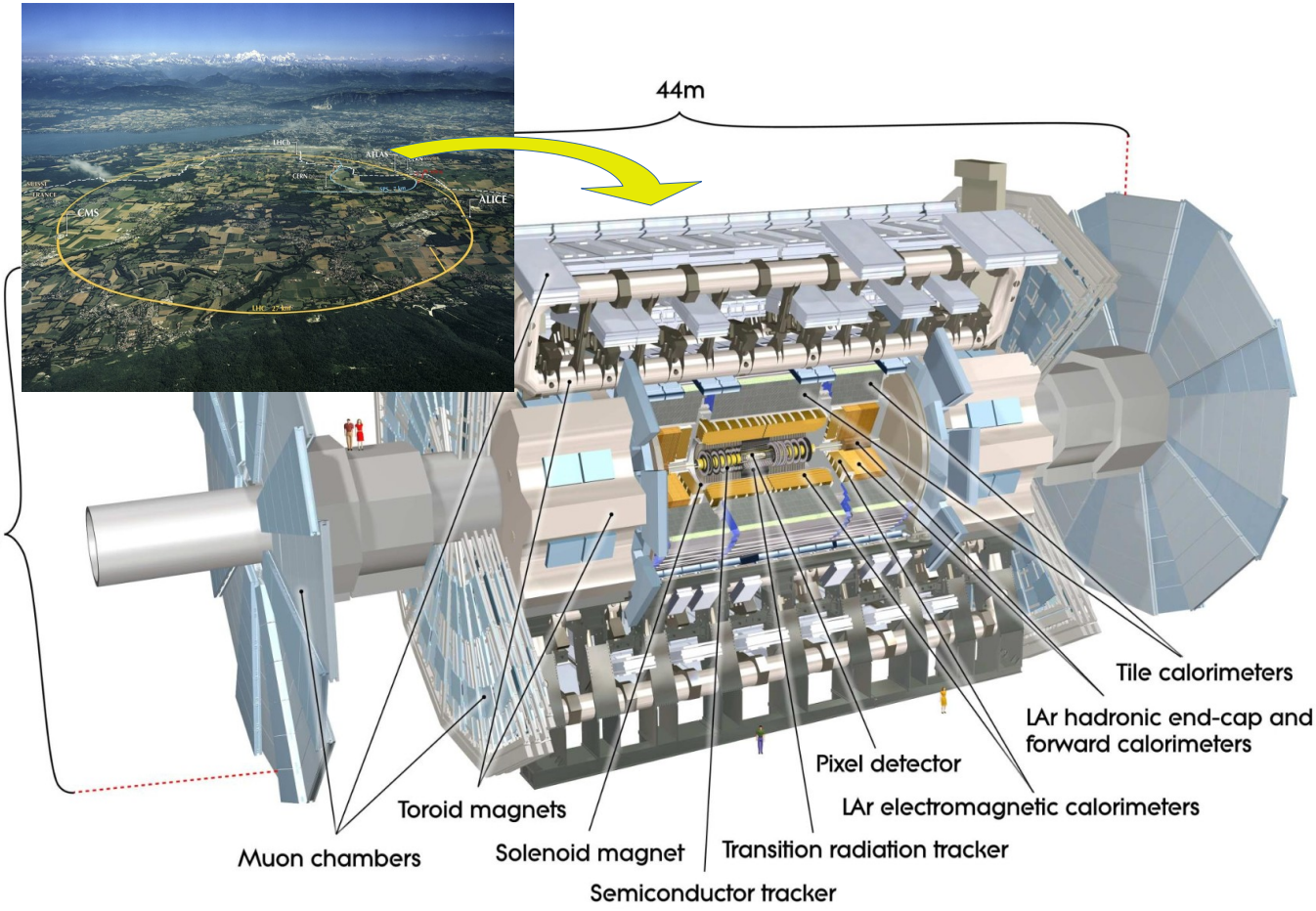
On behalf of the ITk-Pixel Collaboration

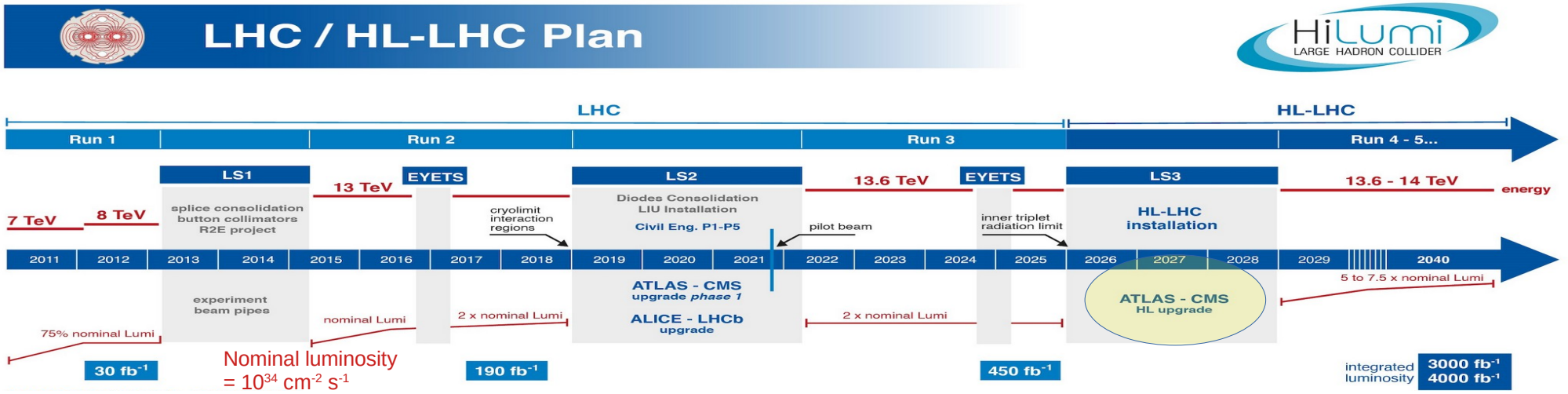
GEORG-AUGUST-UNIVERSITÄT GÖTTINGEN IN PUBLICA COMMODA SEIT 1737

ATLAS LHC

- **LHC** 27km ring at CERN area, with ATLAS, CMS, LHCb, ALICE experiments.
  - Started operation in 2011.
  - **To be upgraded to HL-LHC**.
- **ATLAS-LHC;**
  - Largest particle detector ever constructed.
  - 25m x 44m ; 7000 tonnes.
  - 6 different sub-system detectors/trackers (see Oleg's talk).
  - Investigate wide range of physics, from **Higgs boson** to extra dimensions and particles that could make up **dark matter.**



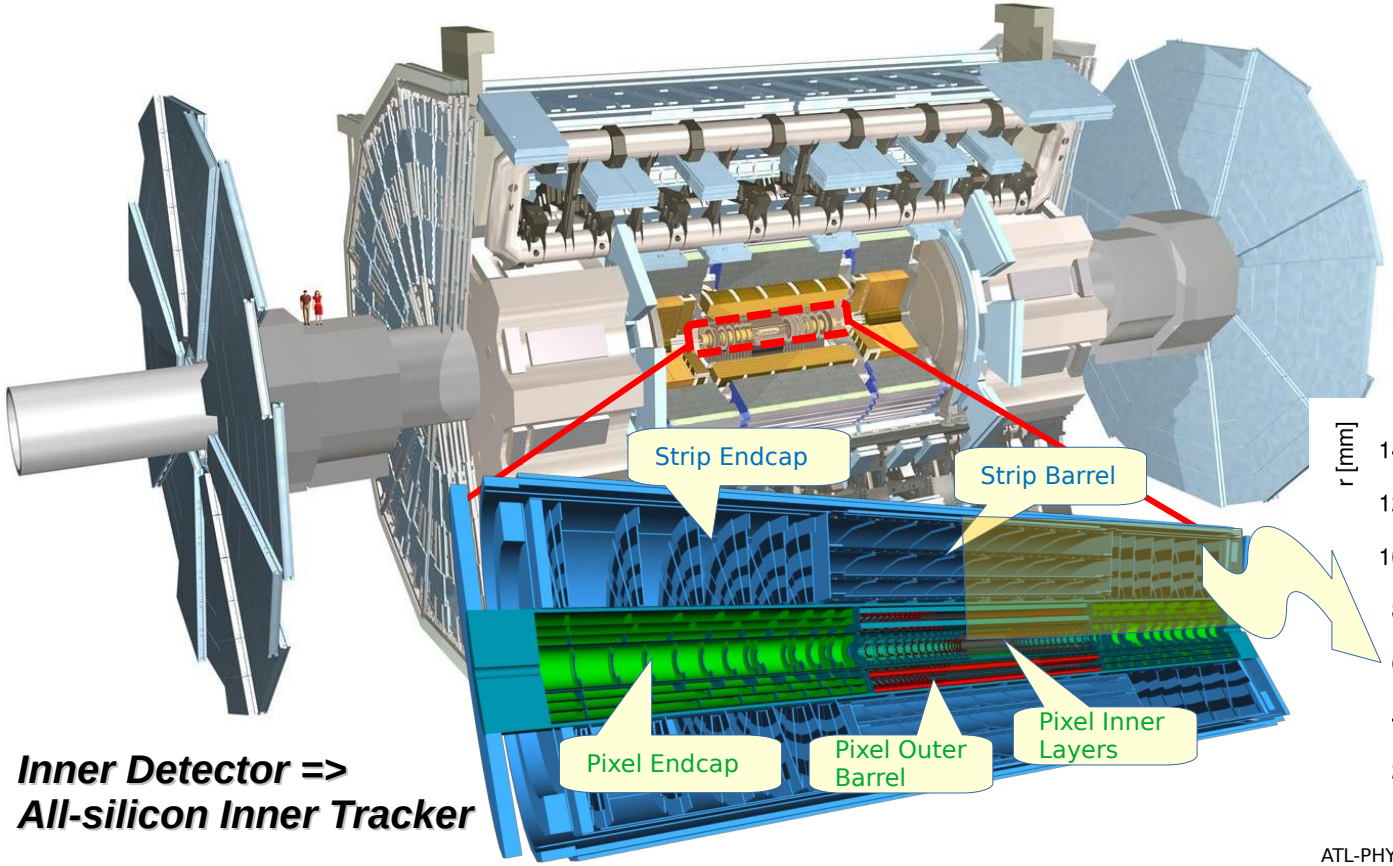
LHC to HL-LHC



- LHC → High-Luminosity LHC upgrade to generate a total of 3000-4000 fb^{-1} of data in 10 years, starting in 2029 (~10 times higher integrated luminosity compared to 450 fb^{-1} by end of Run3).
- In ATLAS: Increase average pile-up from ≈ 60 to up to 200 proton-proton collisions @ 40 MHz (25 ns bunch crossing) ⇒ *Higher particle density and radiation damage*
  - Track density too high for the current Inner Detector (ID),
  - Current ID nearing its end of life:

⇒ *Build new tracking detector, the Inner Tracker (ITk)*

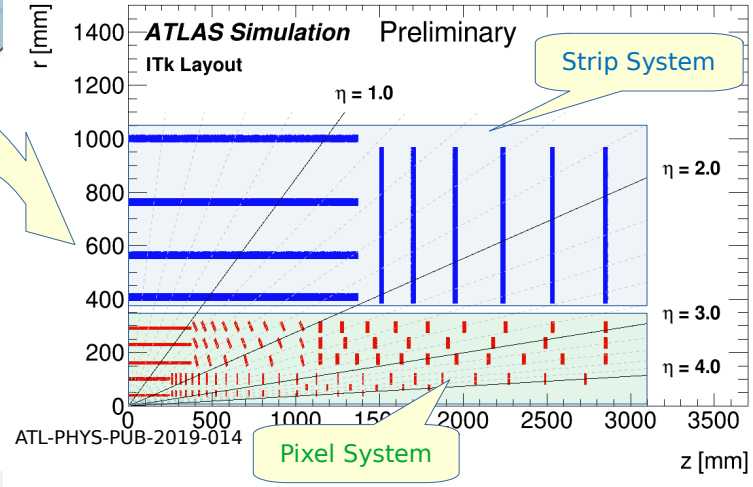
ATLAS ITk



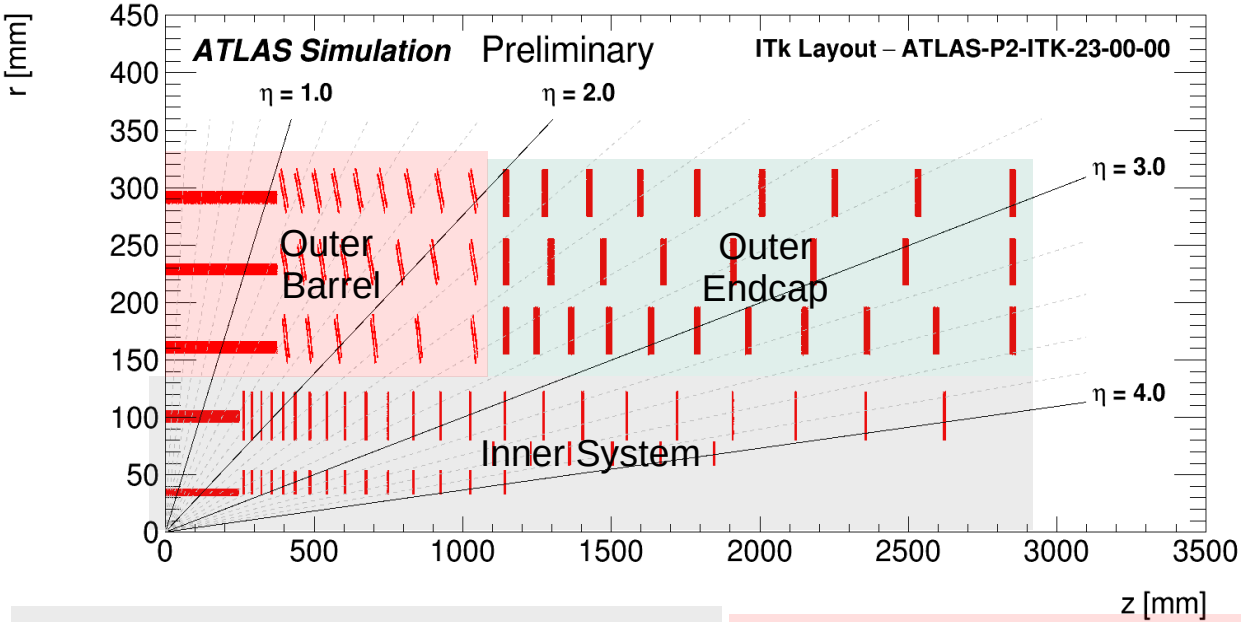
Inner Detector =>
All-silicon Inner Tracker

New ITk:

- Better performance than ID
- **Pixel (this talk)** and Strip (see Elizaveta's talk) systems
- Increased granularity
- Increased radiation hardness
- Increased trigger rate (1MHz)
- **AND** reduced material budget (See Yassine's talk)



ATLAS ITk Pixel



Upgrade summary..

	Current pixel system	New ITk
Granularity (pixels)	~92 M	~5.1 G
N° of modules	~2000	~9700
Active area (m^2)	~1.9	~13
Pseudo-rapidity $\|\eta\|$	< 2.5	< 4

Inner System
- L0-L1 layers of flat staves and rings:
  - 2600 modules
  - 2.4 m^2
- L0: 3D single modules, radius = 39mm
- L1: n-in-p planar quad modules
- Replaceable @2000 fb^{-1}

Outer Barrel
- L2-L3-L4 layers of flat staves (longerons) and inclined rings
- 4772 n-in-p planar quad modules
- 6.94 m^2

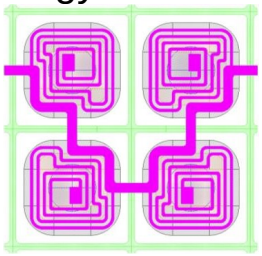
Outer End-cap
- L2-L3-L4 layers of rings
- 2344 n-in-p planar quad modules
- 3.64 m^2

Sensors and Modules

Basic principle

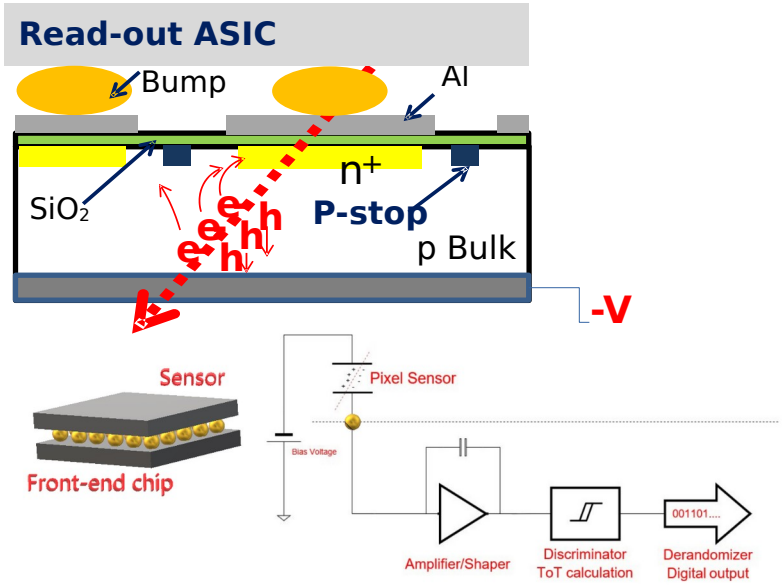
- Backside is negative bias and n+ is ground.
- Detect electron-hole pairs created by ionizing energy loss from minimum ionizing particle.

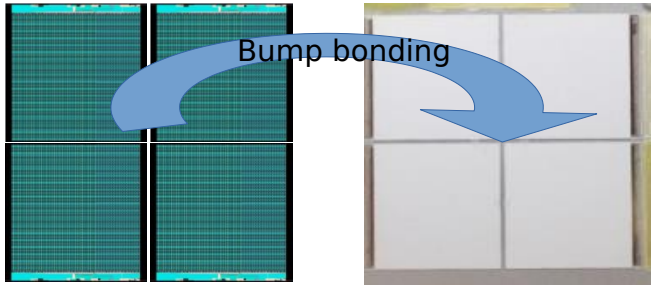
- Pixel detector
  - To ground all pixels, high resistivity biasing grid is necessary (Si-poly resistor)
  - Readout ASIC is connected by “bump bonding”.
  - Sensor thickness: Layer 0,1 : 100um Layer 2,3,4 : 150um



Planar sensor

- n-in-p used in L1 (100 um), and L2,3,4 (150 um)
- Quad modules (1 sensor 40 x 40 mm^2; 4 FE ASICs 20 x 20 mm^2)

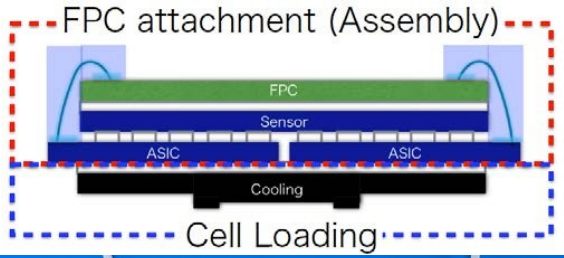


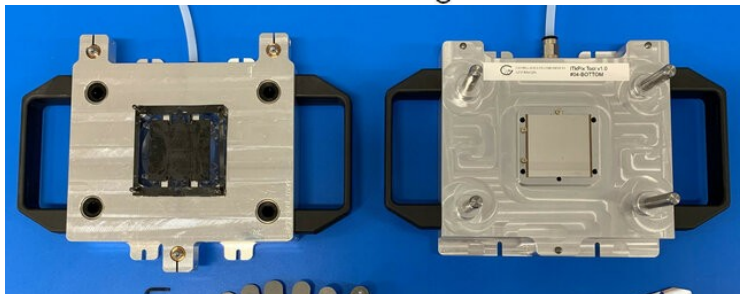


Sensors and Modules

Quad Module (QM) assembly

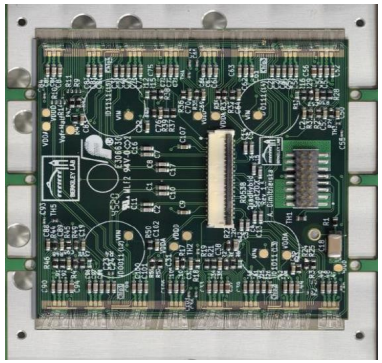
- Once the sensor is bump bonded to the FE ASICs, module is glued to a Flexible Printed Circuit (FPC), using a special assembly tool.
- ASICs are then wire bonded to the FCP.





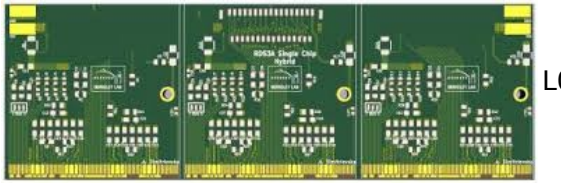
QM Testing

- Design validation (DV) Testing during prototyping and pre-production:
  - Thermal cycling done to stress the bumps.
  - Different electrical tests also performed to verify the QM correct functioning.
  - Testbeam campaigns for um-irradiated and irradiated modules to test module efficiency and track reconstruction.
- Later: Quality control (QC) on each module built during production → make sure to install only good modules.



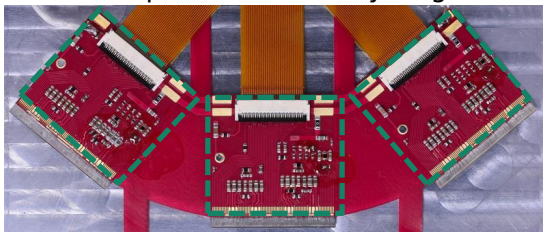
3D sensors – Single module

- Used in L0.
- Single-side technology: conductive support wafer (Si-Si), both electrodes etched from the same side.
- 150 µm thin active substrate to reduce cluster size and data rates.
- Small pixels (high occupancy + resolution):
  - Rings: 50x50 µm2
  - Flat barrel: 25x100 µm2
- Single module (1 sensor 20 x 20 mm^2; 1 FE ASIC 20 x 20 mm^2) bump bonded.
- Arranged in triplets for L0 ring and barrel regions.
- Same as QM, wire bonding and testing.
- Testbeam campaigns for um-irradiated and irradiated modules to test module efficiency and track reconstruction.

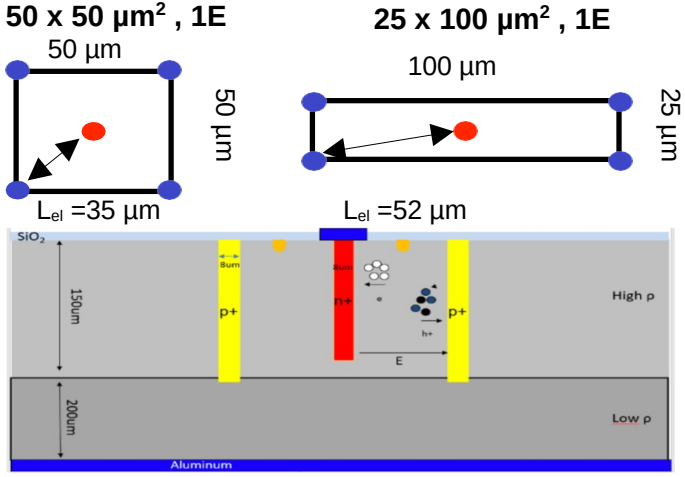


L0 barrel

3D sensor : Triplet structured by single modules



L0 ring



Testbeam Example

- **Testbeam** campaign w/ ITkPixV1 un-irradiated / irradiated modules (2023).
- Done at CERN – SPS north area.
- Pion beam at 120 GeV passes through Mimosa26 telescope.
- Required in-pixel efficiency is 98,5% for un-irradiated and 97% for irradiated planar QMs are met.
- For 3D modules, required in-pixel efficiency is 96%.
  - Near p+ electrode region, it drops to 85% and 70%.
  - Outside it reaches 100%.
  - Average efficiency requirement is met.
  - ITkPixV2 tests planned during 2024

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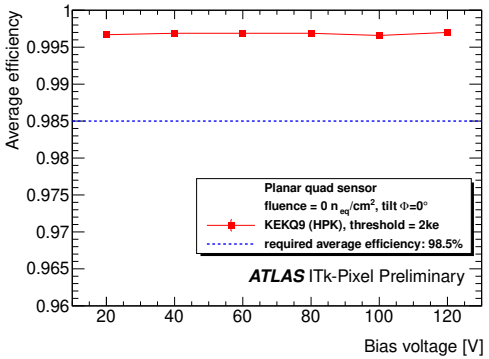
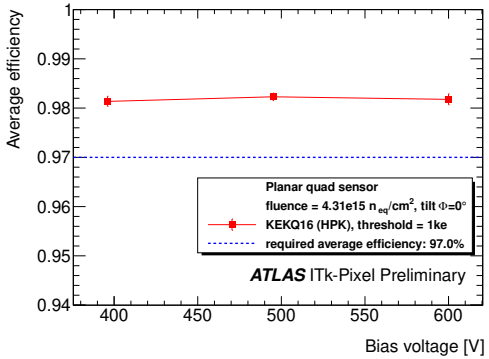
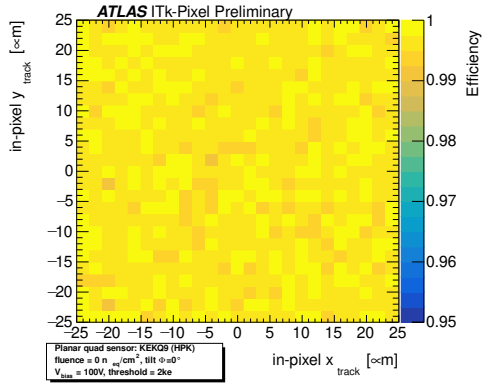


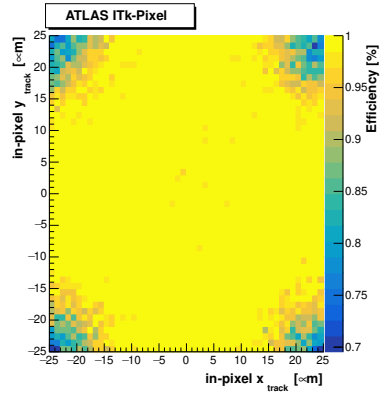
Un-irradiated planar QM



irradiated planar QM

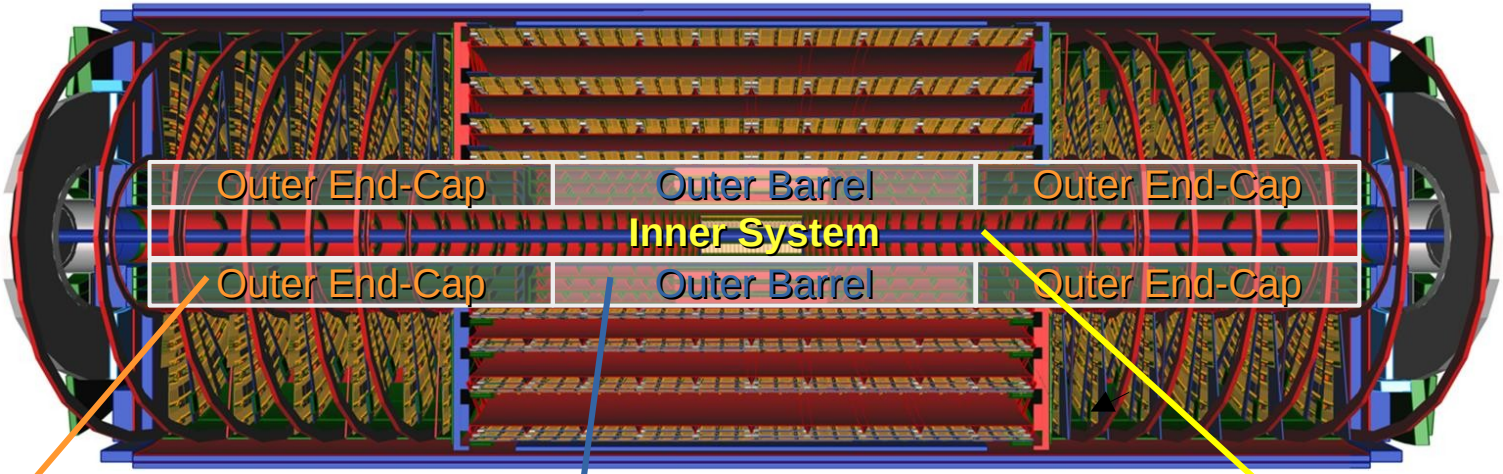


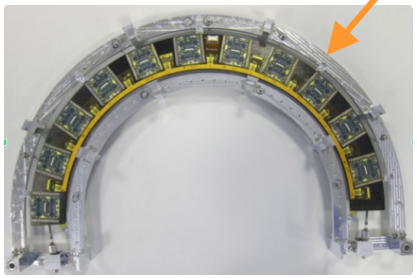
Un-irradiated planar QM



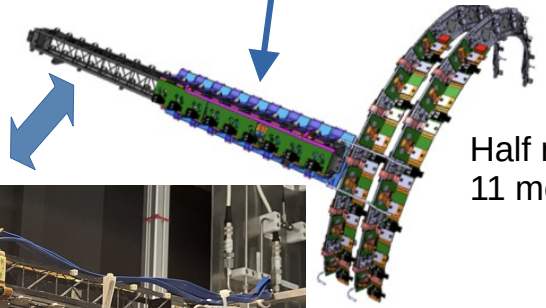
Un-irradiated 3D sensor

ITk-Pixel Building Blocks

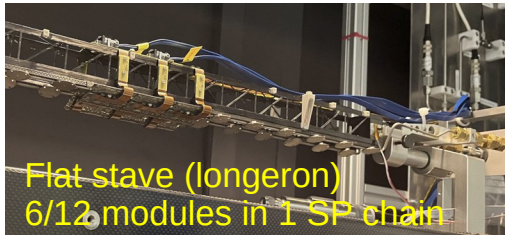




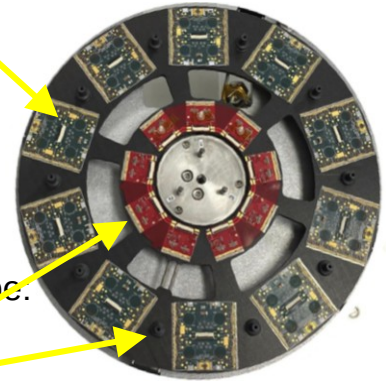
Half ring prototype
- 11 modules in 1 Serial Powering (SP) chain



Half ring schematic
11 modules in 1 SP chain



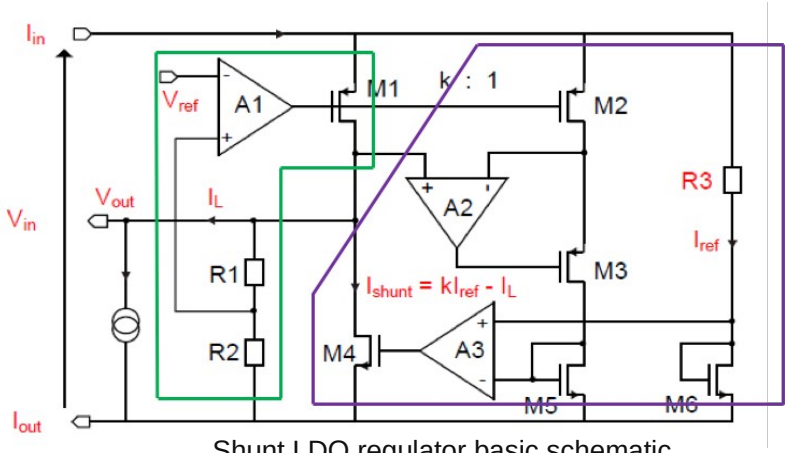
Outer Barrel Demonstrator @SR1- CERN



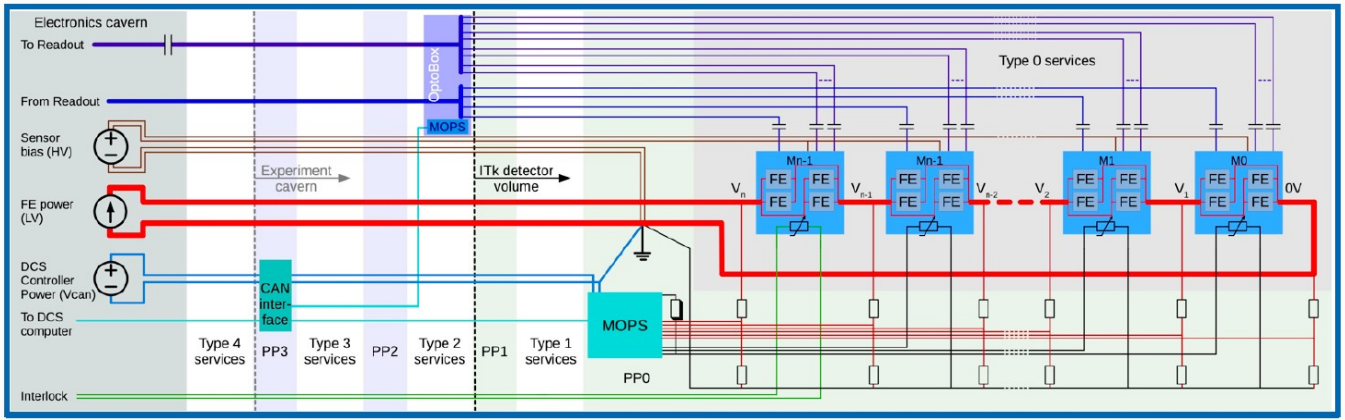
Loaded ring prototype:
L0: 3D modules
L1: planar QMs

Pixel Serial Powering

- To provide required power to operate all FE over long wires, several modules (3 to 16) are connected in series and powered by a constant current source.
- **Shunt LDO regulators** are integrated in FE to generate constant operating voltage
- Module FEs are powered in parallel
- Dedicated DCS chip (MOPS) used for monitoring.



Shunt LDO regulator basic schematic



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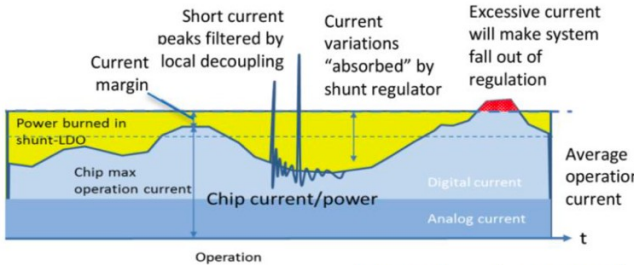
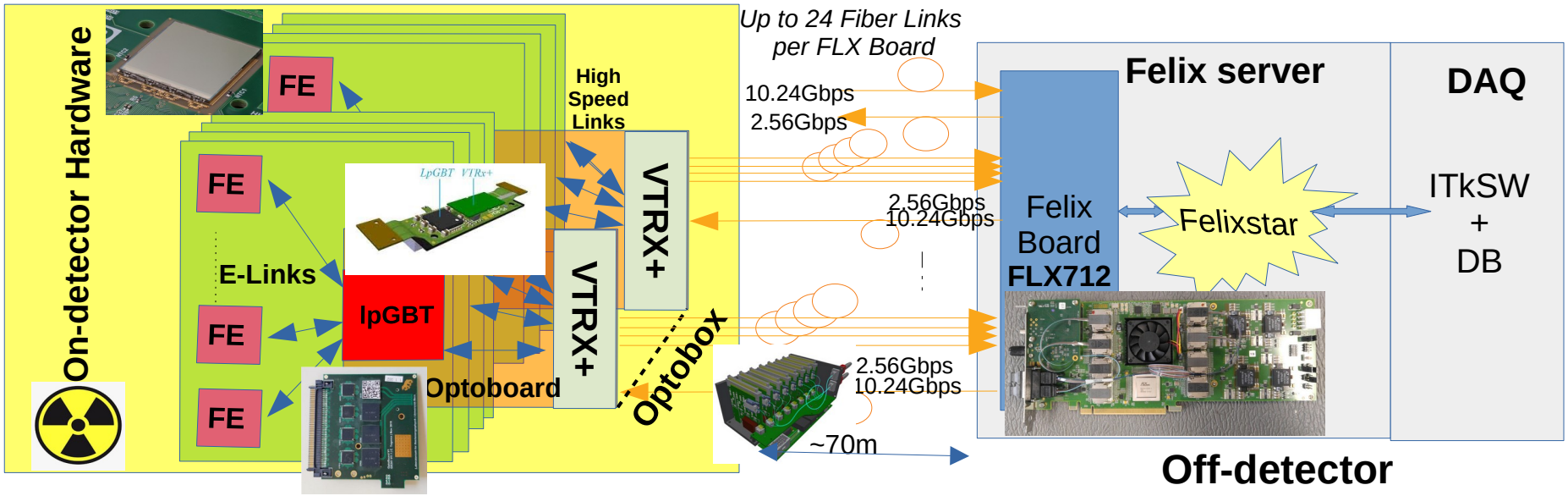


FE overall current stabilized by shunt LDO (within some limit!)

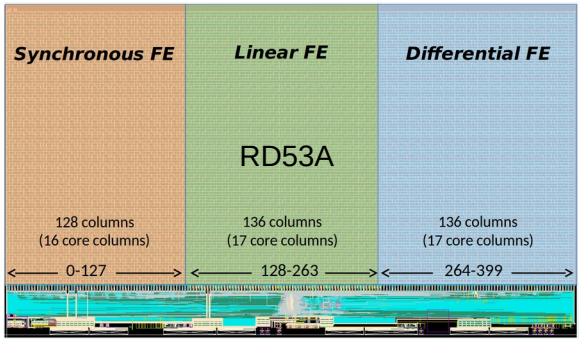
ITk-Pixel DAQ

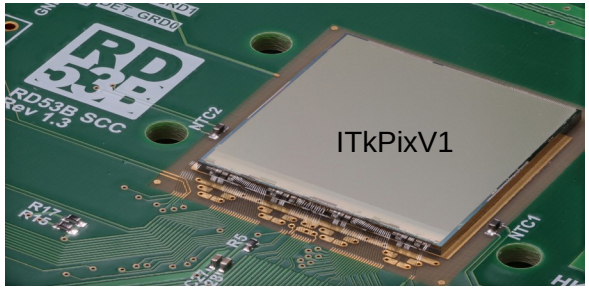


- **ITkSW**: DAQ software based on YARR (+ DB and storage).
- Networking services (**NetioNext/Felixstar**).
- **FELIX:** PC-based gateway w/ PCIe FPGA board (**FLX-712**) and software tools, used in ATLAS and provided/maintained centrally from the TDAQ group
- **VLDB+/Optoboard (Optobox):** lpGBT(s), VTRX+, GBCR (ASICs developed at CERN)
- Connection cabling (electrical (firefly/Twinax)/optical).
- **FEs**: RD53A/RD53B(ITkPix-V1)/RD53C(**ITkPixV2**).

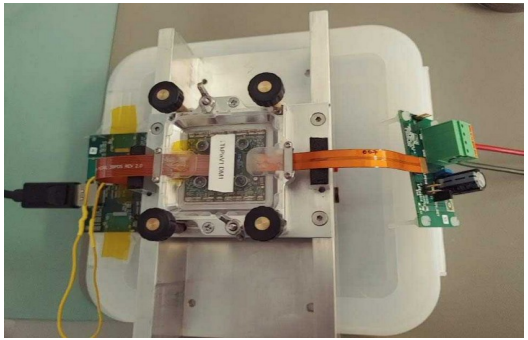
Readout FE Chips/QMs

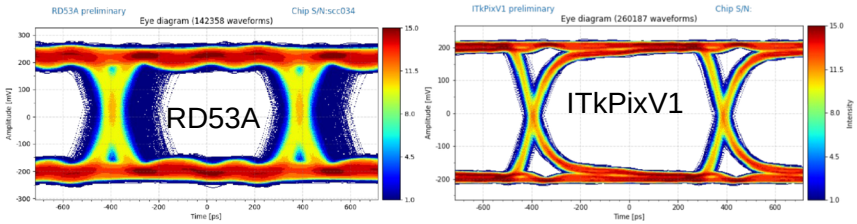
- **RD53 collaboration** to develop the FE readout chip common for ATLAS and CMS pixel detectors:
  - RD53A: prototype chip with 3 FE analog part flavors: synchronous, linear and differential.
  - RD53B: improved design ITkPix for ATLAS (differential FE, 400×384 pixels), CROC for CMS (linear FE, 432×336 pixels). ITkPixV1 tested and few bugs identified. Link sharing feature implemented.
  - RD53C: ITkPixV2 is the production FE, delivery started and first modules currently under test.





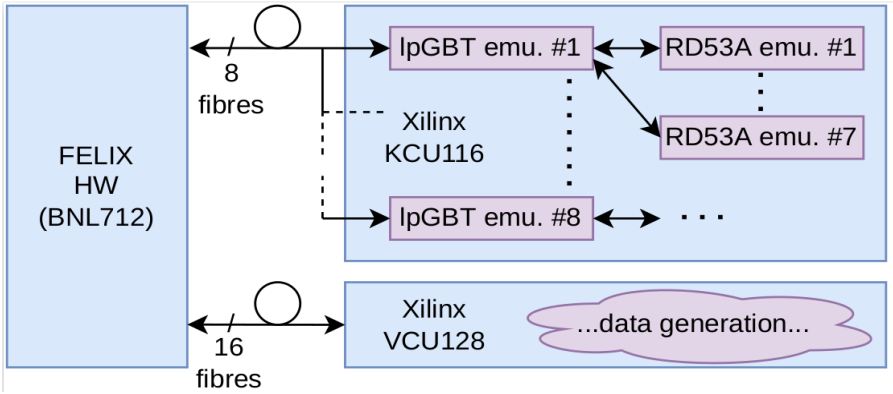
ITkPixV1
digital QM

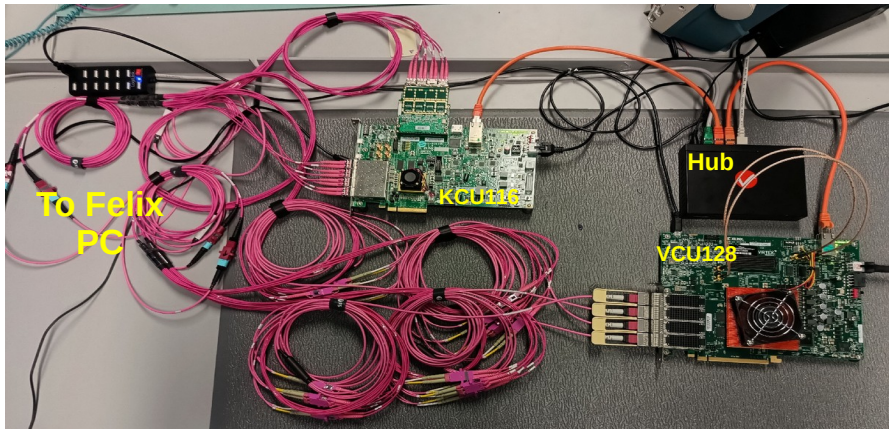




Readout Chain Testing

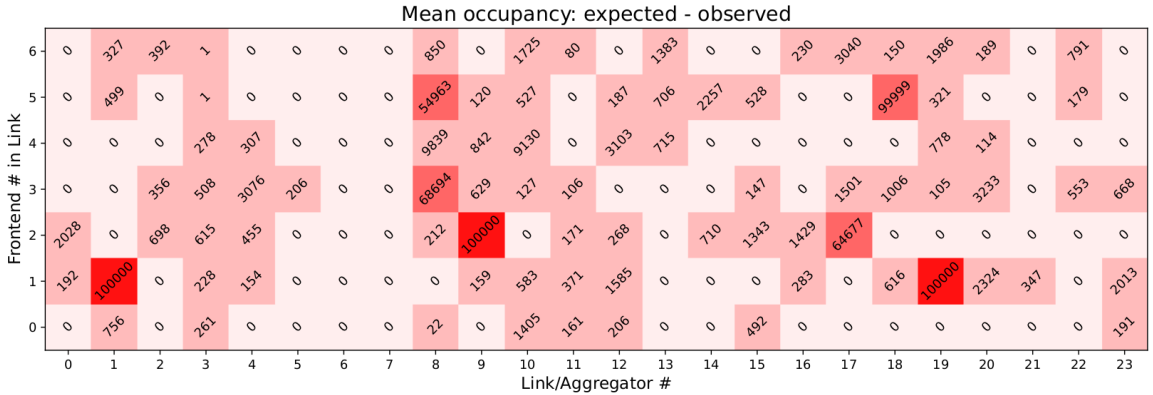
- FLX712 setup:
  - Has 24 fiber links
  - Each fiber linked to 1 lpGBT
  - Connected to 6/7 RD53A/B E-links @1.28Gbps
- (Sub-)system test with only ONE FLX712 requires:
  - **HW: 24 lpGBTs +168 FEs + connections**
  - **OR emulators on FPGAs with realistic/verified functionalities**





Readout Chain Testing

- Start by using FPGA lpGBT and RD53A emulators (move to RD53B later)
  - KCU116: 4 SFPs + FMC/4 SFPs => 8 links (8 lpGBT + 56 RD53A emulator instances)
  - VCU128: 4 QSFP28 => 16 links (16 lpGBT and 112 RD53A emulator instances)
- System configuration/control require more functional blocs => **SoC design** (Processing system (PS) + peripherals..)
- PS built around Xilinx MicroBlaze soft IP, with bare metal FW (no need to any RTOS)
- Individual/multiple/all FEs (10 hits/event, with 512000 triggers sent)
  - Lost triggers witnessed (with variable loss pattern)
  - Work in progress...




```
(venv) lab34:~/stress_test_sw/apps$ ./init-board.py vcu128 ../configs/config.lpgbt
Initializing board with IP 192.169.1.11 on port 7
Board("vcu128", 192.169.1.11:7, device="")
Available frontends:
00: xxxxxxx
01: xxxxxxx
02: xxxxxxx
```

```
lab34:~/Scripts$ flx-info link
Card type : FLX-712
Firmw type: PIXEL

Link alignment status
-------------------------
Channel |  0   1   2   3   4   5   6   7   8   9  10  11
-------------------------------------------------------
Aligned | YES YES YES YES YES YES YES YES YES YES YES YES

Channel | 12  13  14  15  16  17  18  19  20  21  22  23
-------------------------------------------------------
Aligned | YES YES YES YES YES YES YES YES YES YES YES YES
```

```
-------------------------
Endpoint 0 ('*'=aligned, '-'=not aligned)
LNK 0        8       16       24       32
 0: *---*--- *---*--- *---*--- *---**-- -----
 1: *---*--- *---*--- *---*--- *---**-- -----
 2: *---*--- *---*--- *---*--- *---**-- -----
 3: *---*--- *---*--- *---*--- *---**-- -----
 4: *---*--- *---*--- *---*--- *---**-- -----
 5: *---*--- *---*--- *---*--- *---**-- -----
 6: *---*--- *---*--- *---*--- *---**-- -----
 7: *---*--- *---*--- *---*--- *---**-- -----
 8: *---*--- *---*--- *---*--- *---**-- -----
 9: *---*--- *---*--- *---*--- *---**-- -----
10: *---*--- *---*--- *---*--- *---**-- -----
11: *---*--- *---*--- *---*--- *---**-- -----
Endpoint 1 ('*'=aligned, '-'=not aligned)
LNK 0        8       16       24       32
 0: *---*--- *---*--- *---*--- *---**-- -----
 1: *---*--- *---*--- *---*--- *---**-- -----
 2: *---*--- *---*--- *---*--- *---**-- -----
 3: *---*--- *---*--- *---*--- *---**-- -----
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10: *---*--- *---*--- *---*--- *---**-- -----
11: *---*--- *---*--- *---*--- *---**-- -----
```

Conclusions

New ATLAS all-silicon ITk detector is in preparation for the HL-LHC phase-II upgrade:

- Increase granularity, average pile-up, radiation hardness, trigger rate..
- Divided in ITk Pixel and Strip subsystems.
- Use new sensor technology, readout FE chips, other ASICs.
- DAQ readout chain development is undergoing.
- Test setups are being qualified for production.
- ATLAS ITk Pixel collaboration member institutes are about to pass from pre-production into production to have upgraded ITk installed and operational by 2029.

Thank you!