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Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Elena Mazzeo

On behalf of the ATLAS Liquid Argon Calorimeter Group

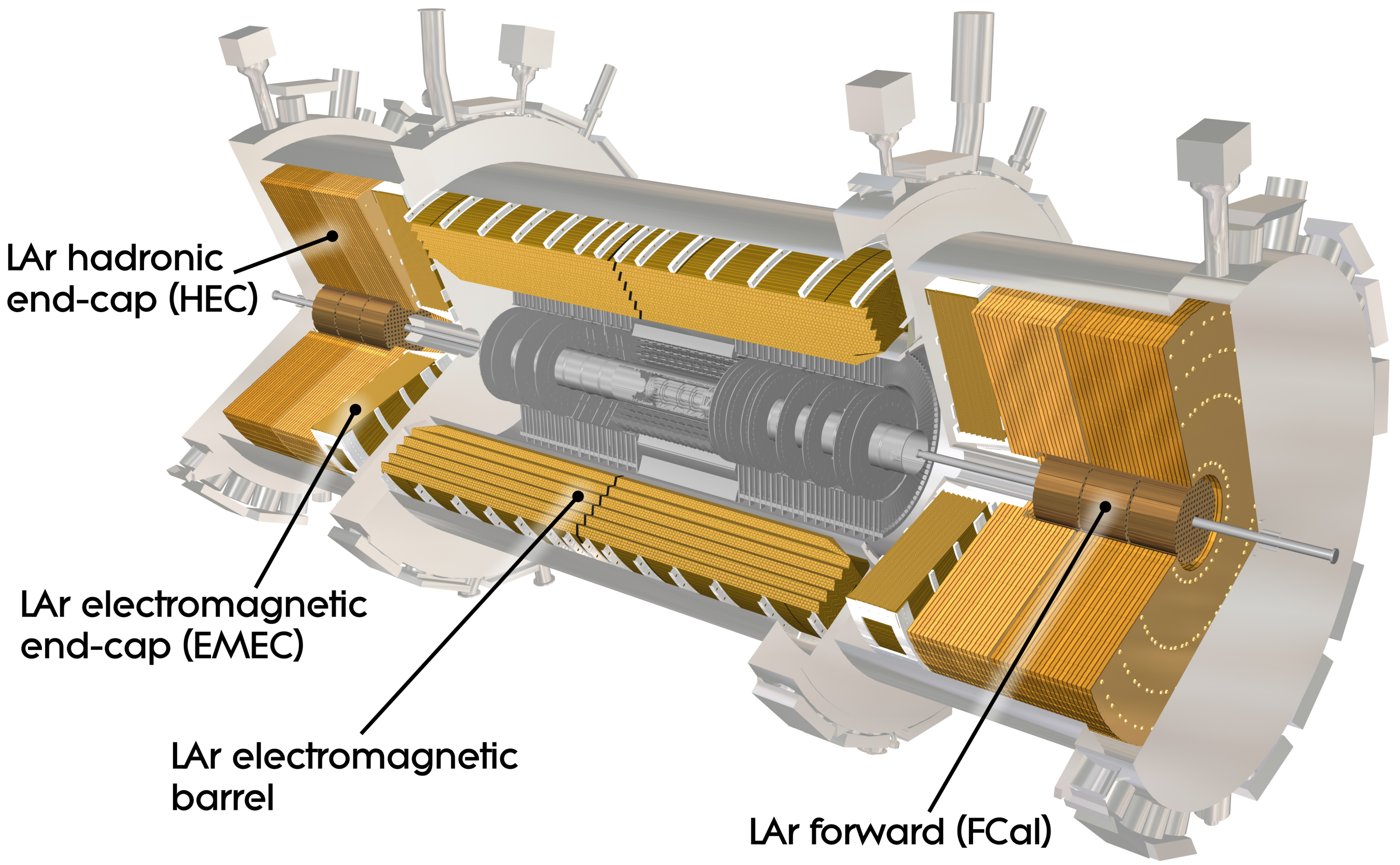
UNIVERSITÀ DEGLI STUDI DI MILANO

INFN

ATLAS EXPERIMENT

The ATLAS Liquid Argon (LAr) Calorimeter

- Sampling calorimeter based on **liquid argon** as **active medium**.
- Measures energy, position and timing of **electromagnetic showers** (electrons and photons) + jets.



EM calorimeter (barrel + endcap)

- Lead + LAr
- 173,312 read-out channels
- Coverage: |η| < 3.2

Hadronic Endcap (HEC)

- Copper + LAr
- 5632 read-out channels
- Coverage: 1.5 < |η| < 3.2

Forward Calorimeter (FCal)

- Copper/Tungsten + LAr
- 3524 read-out channels
- Coverage: 3.1 < |η| < 4.9

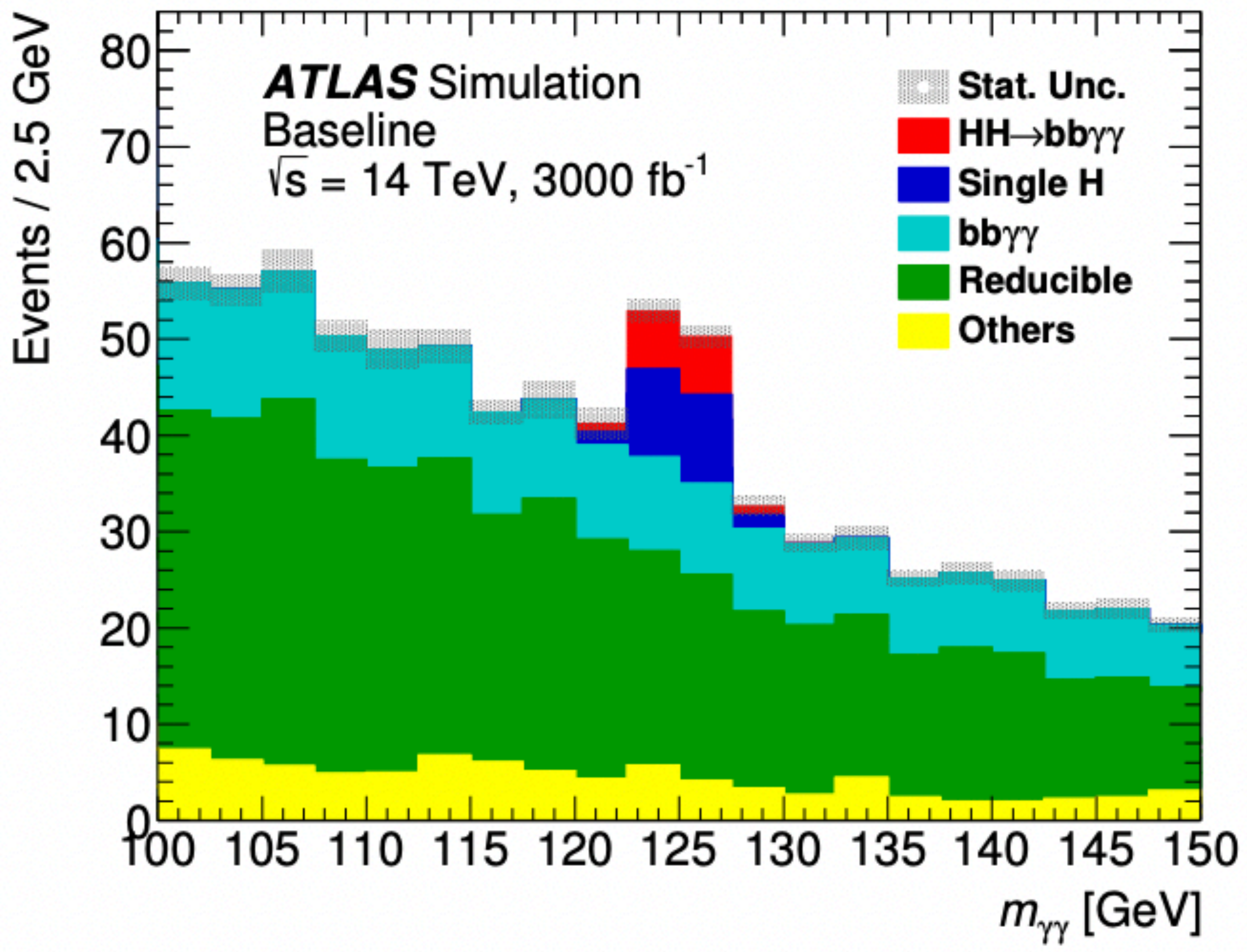
= **182,468 cells**!

→ **Read-out electronics** samples data at **40 MHz** and sends off the detector for analysis and triggering!

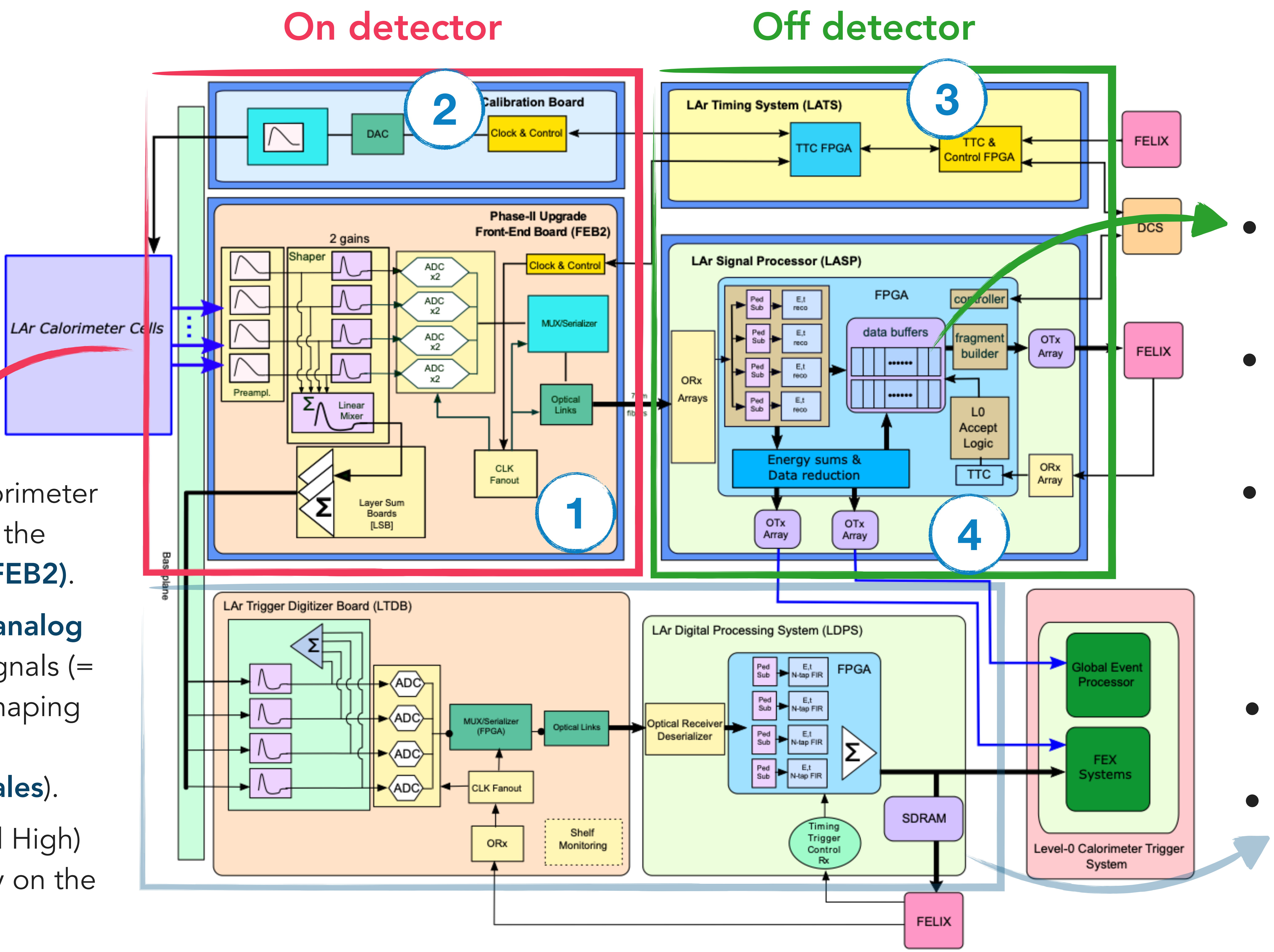
The High Luminosity LHC (HL-LHC) phase

- During Run 4, ATLAS is expected to collect **3000 fb^{-1}** of data (**× 20 w.r.t. Run 2 data**) during **10 years of operation**.
- **Achieved** thanks to instantaneous luminosity up to 7 × 10^{34} cm^{-2}s^{-1} = **7 × design luminosity**.
- **Challenging operation** environment!
  - ATLAS trigger & data acquisition (**TDAQ**) system needs to handle **simultaneous *pp* interactions** (= **pileup** ⟨μ⟩) up to ~**200**.
  - Stronger **radiation tolerance** for on-detector electronics.

- To **survive** the **extreme conditions** of the **HL-LHC data-taking**, the ATLAS detectors will undergo major upgrades (= **Phase 2 upgrade**!).
  - Includes redesigning and replacing the **readout electronics** for the **LAr calorimeters**
    - Will have to cope with the **increased data-volume** at HL-LHC and tolerate stronger radiation doses, while retaining **excellent performance** for the **measurements** of **incoming electrons, photons, and jets**.



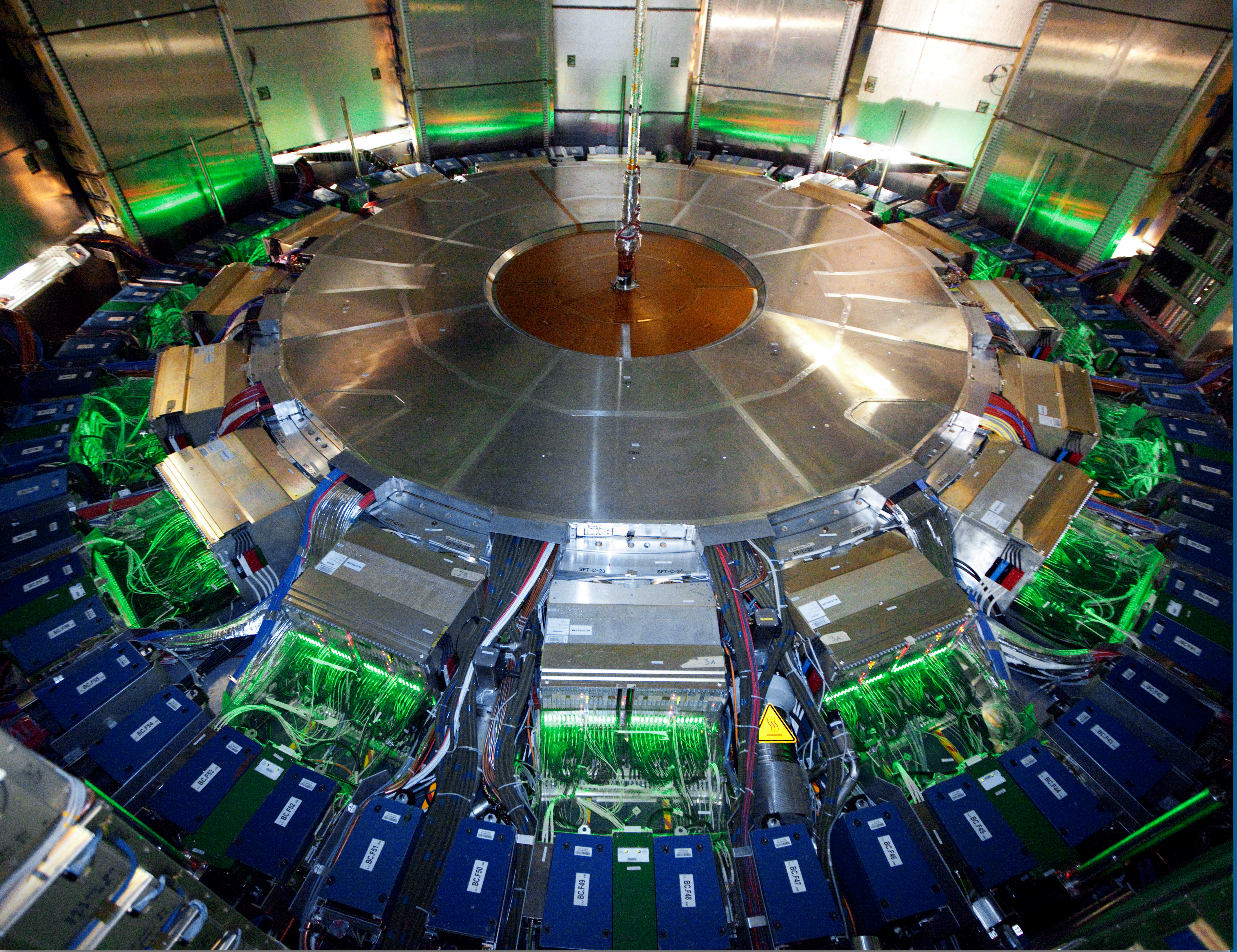
Outline of the LAr HL-LHC readout



- Signals from the calorimeter cells are read out by the **Front End Boards (FEB2)**.
- The FEB2s perform **analog processing** of the signals (= preamplification + shaping and splitting in **two** overlapping **gain scales**).
- **Both gains** (Low and High) are **digitized** directly on the FEB2s.

- **Digitized signals** are sent via optical links from the FEB2s to the LAr Signal Processing boards (**LASPs**).
- LASPs performs **digital filtering** and **accurate** and **fast energy & timing calculations**.
- LASPs also send **inputs** to the **trigger system** (= will **receive full granularity calorimeter data @ 40 MHz**)!

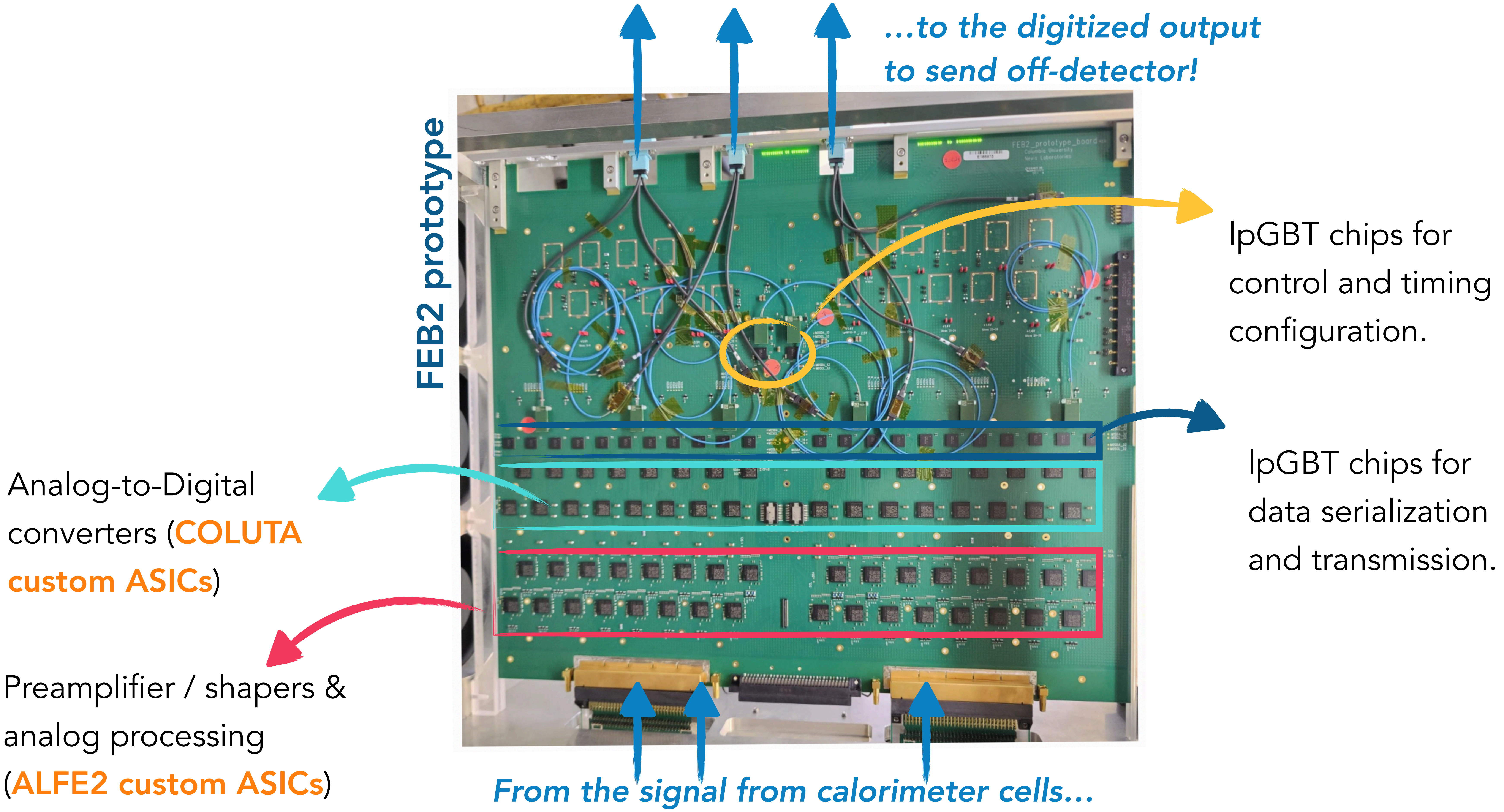
- Second complementary **TDAQ chain** relies on the **Phase 1 trigger**.
- Described in **Émilien's presentation**!



On-detector electronics

Outline of the Front End Boards (FEB2)

- The Front End Boards (FEB2s) receives signals from calorimeter cells and perform **analog processing**.
- Signals are **digitized**, **serialized** and **transmitted** off-detector via lpGBT protocol.
- **1524 FEB2s** with **128 channels** each.



Key results

- First **full-size prototype** (with **all 128 channels** populated) is **ready**, and is **currently being tested**.
- In particular, tests for **radiation-hard powering solutions** are in progress (see Slide 8 for details).
- Next prototype expected in Summer 2024.

Outlook

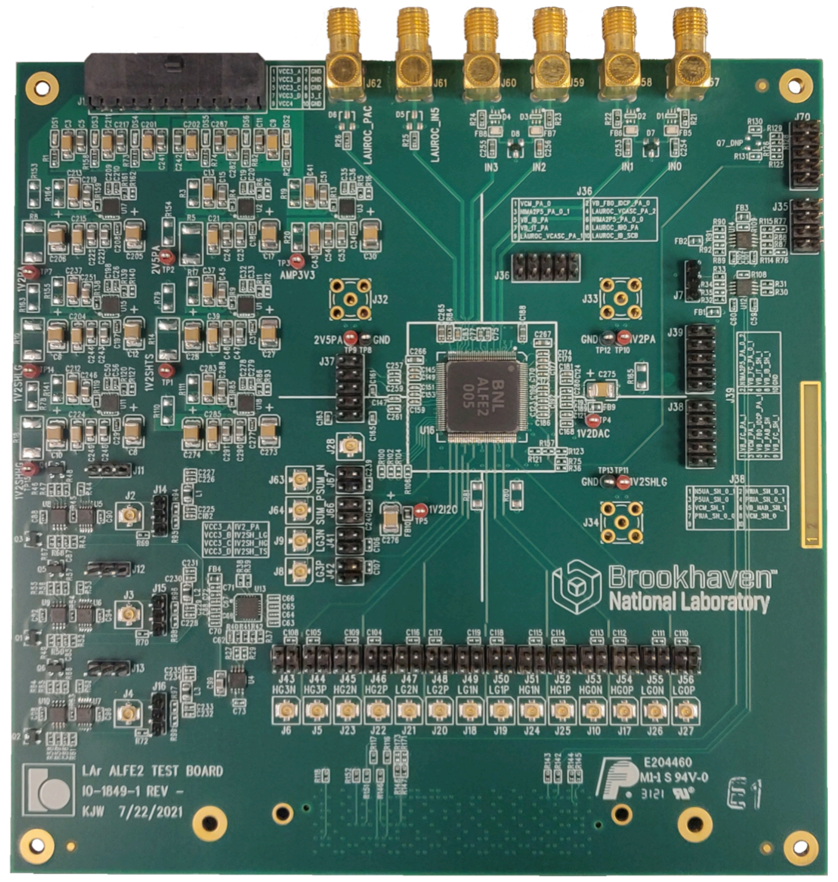
First large-scale integration test of the **full readout chain** is expected for Summer 2024.

ALFE2 and COLUTA custom ASICs

1

ALFE2 custom ASIC: Pre-Amplifier/Shaper (PA/S)

ALFE2 test board



- Based on 130 nm CMOS technology, provides **amplification** and **bipolar CR-(RC)²** **shaping** over **two overlapping gain scales** (High and Low).
- Each ASIC will handle signals from 4 calorimeter cells, and provide 9 differential inputs to the ADCs (= 4 analog signals × 2 gains + 1 sum signal for hardware trigger).

Key results

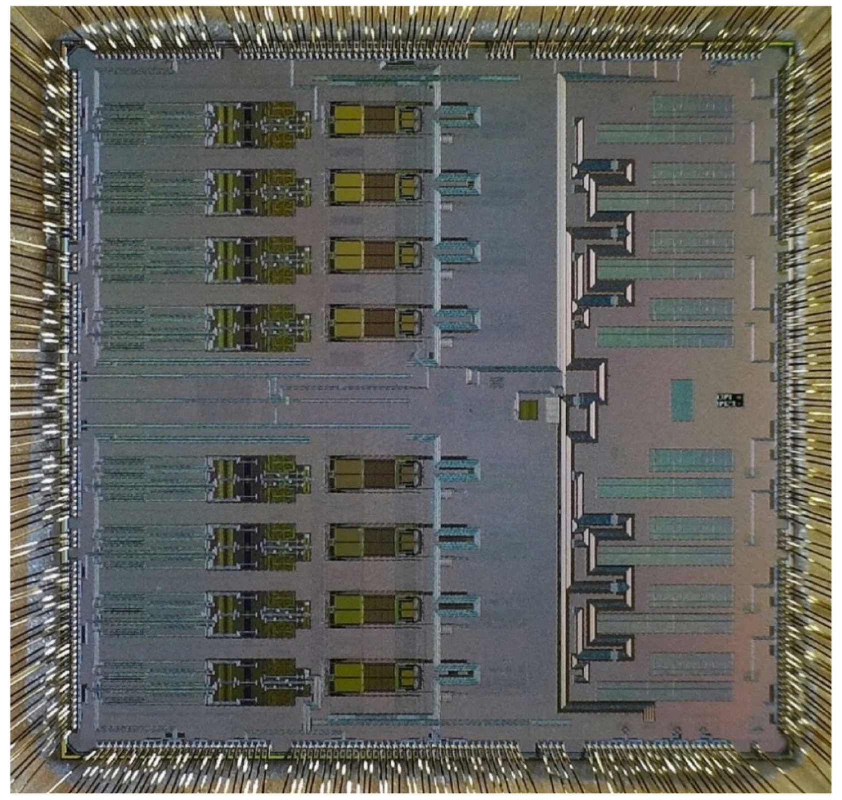
- Non-linearity < 0.1% and noise ~ 150 nA (greatly exceeding the 350 nA requirement!) for 10 mA channels.
- Radiation tolerance: performant after 12 kGy doses (× 8 w.r.t the expected dose!).

= **Exceeding specifications**!

- Both ASICs are **concluding** the **pre-production stage**, and **entering mass production**.
- Preparation of setup for **automatic testing of the full production** in advanced stage!

COLUTAv4 custom ASIC: Analog to Digital Converter (ADC)

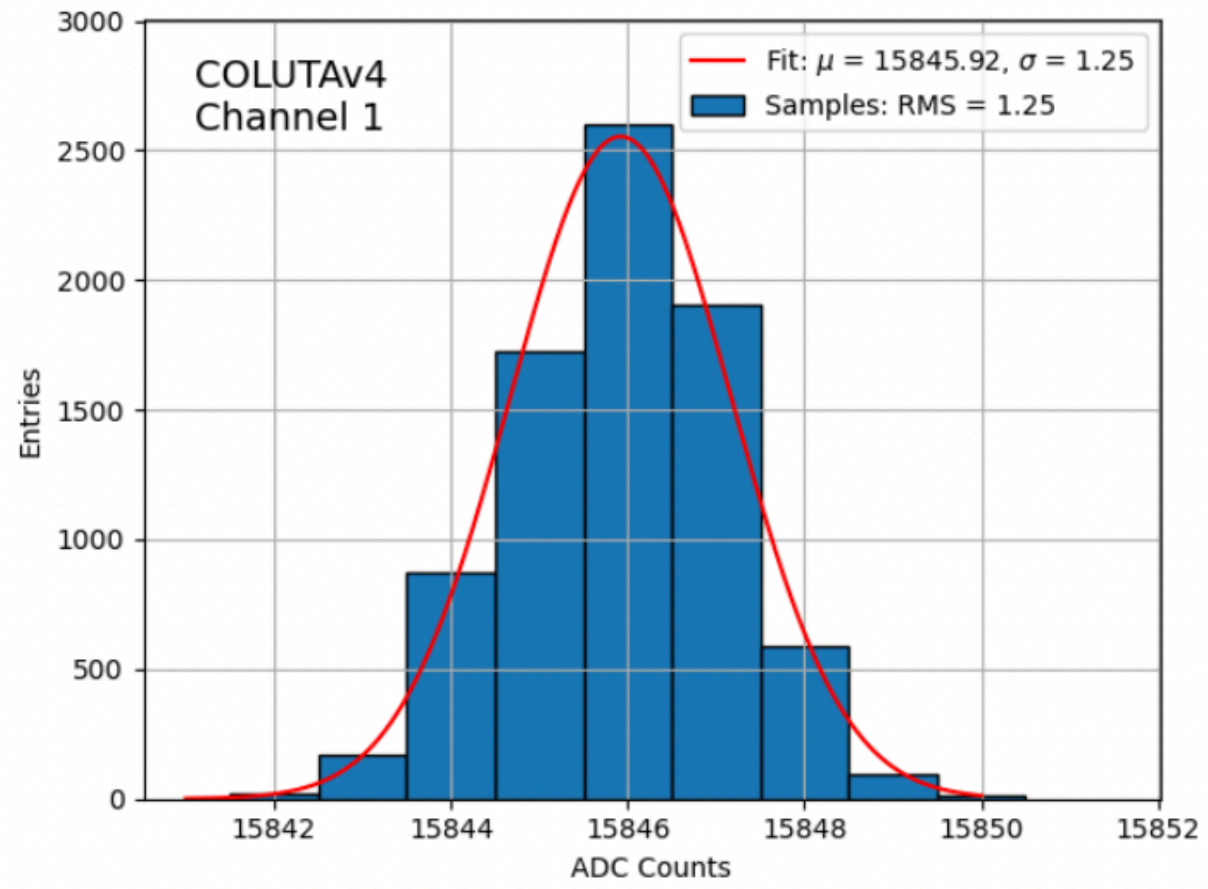
COLUTA chip die



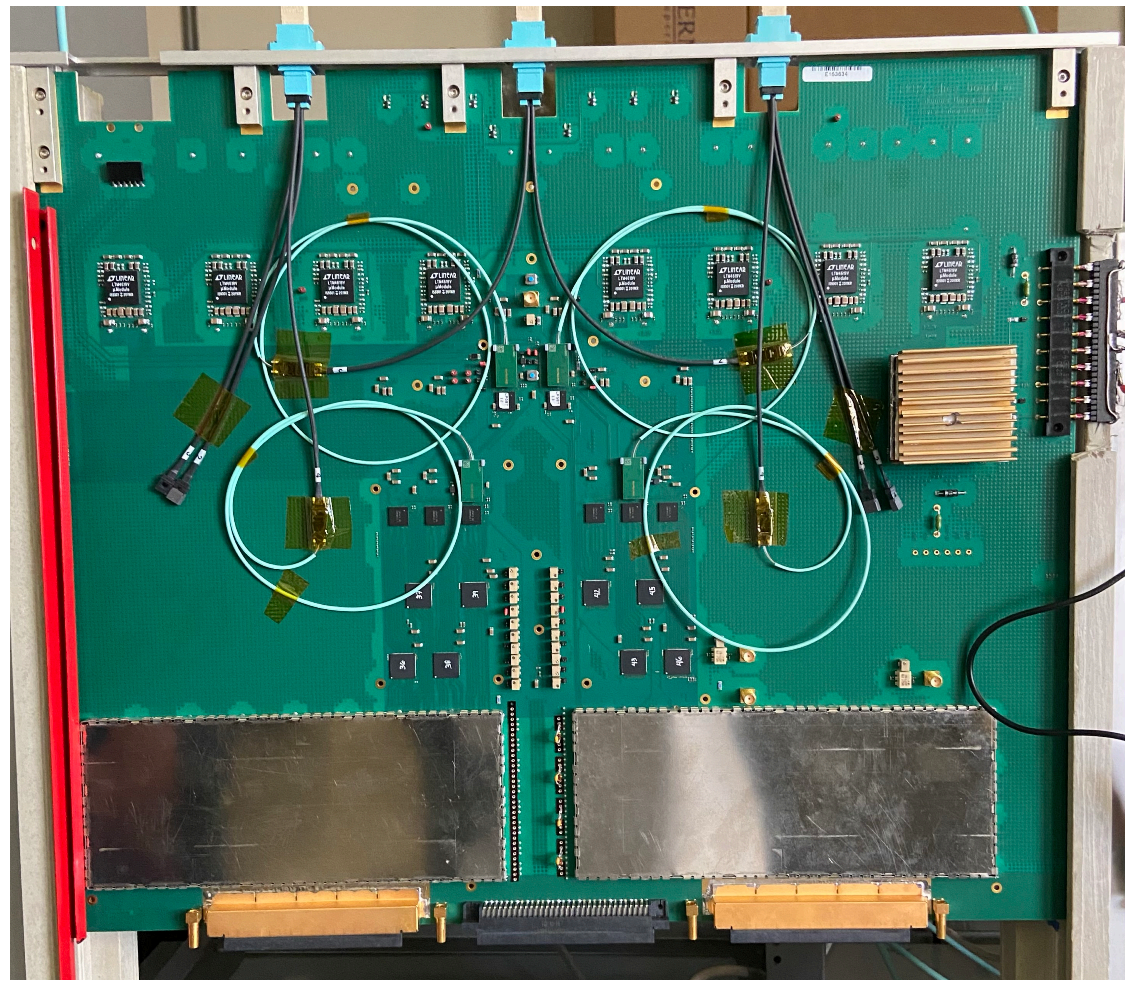
- Based on 65 nm CMOS technology, **digitizes** PA/S outputs at **40 MHz** on a **14-bit dynamic range** with two gains (required to cover the full required 16-bit dynamic range) and > 11-bit resolution.
- It covers **8 channels** = 4 analog LAr signals × 2 gains.

Key results

- Excellent uniformity performance with injection of 2MHz sine wave.
- Low pedestal noise: RMS of 12 ADC counts.



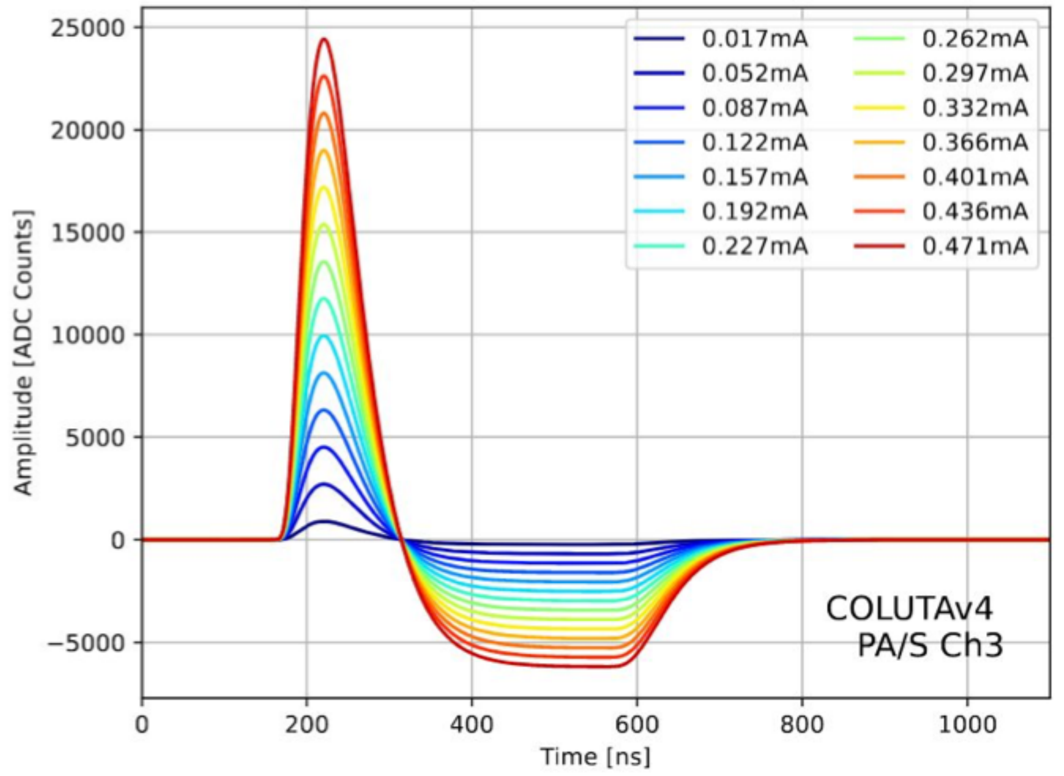
Integration & powering with FEB2 (pre-)prototype

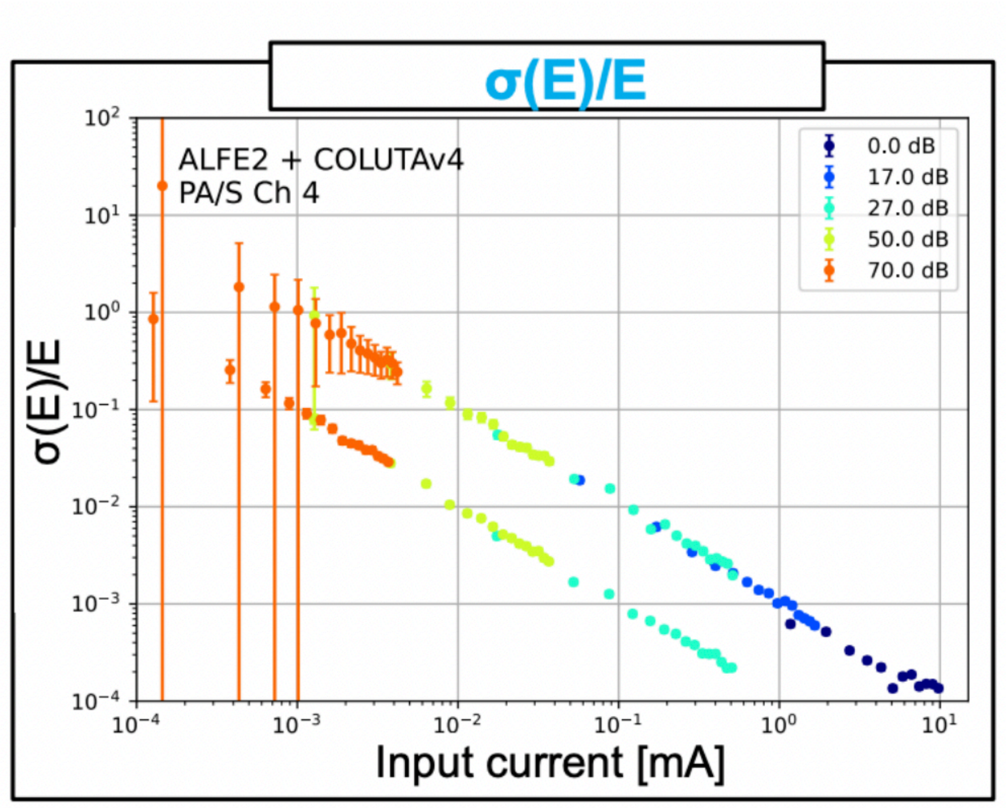


- Slice board with **32 channels** (1 / 4 of FEB2) with same **density** as **final** FEB2.
  - Includes 8 preamplifiers / shapers, 8 ADCs, and 8 lpGBT + VTRX+ chips for configuring the board and for data serialization and transmission.
- Demonstrated the functionality of the read-out and control for 32 channels.
- Used for **characterizing energy** and **timing**, **linearity**, and **multi-channel performance,** and for testing the power distribution system.

PA/S + ADC performance

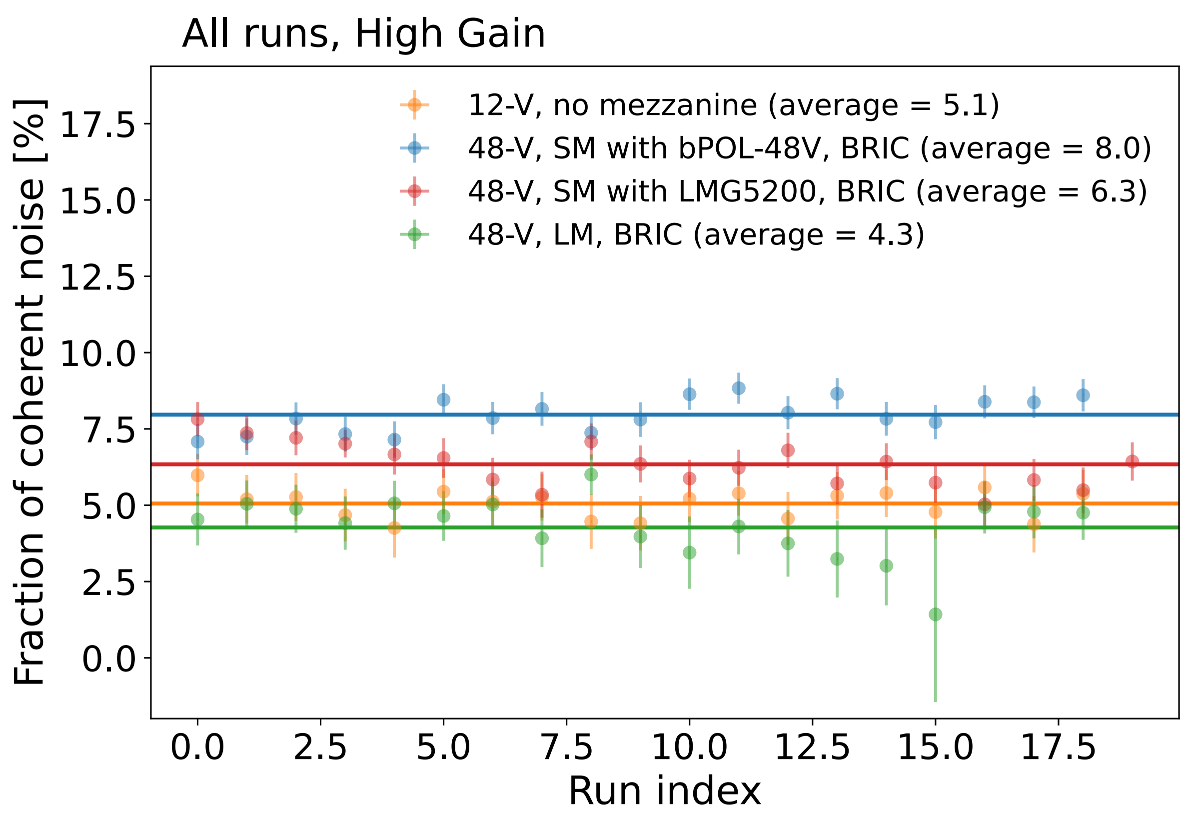
Tests with injected pulses show an **excellent uniformity in pulse shapes**, as well as **extremely low electronic noise**.





Power distribution

- Tested various solutions for **on-board stepping down 48-V** power supply to the **voltages** needed by the **ASICs** with the help of **mezzanines**.
- **Noise** level **under control** using **radiation-soft** solutions.



- Tests with **CERN-developed radiation-hard** solutions using bPOL48V + bPOL12V are ongoing.

Calibration boards

2

- The calibration boards inject **known** calorimeter **signals** at the LAr copper electrodes with **16-bit dynamic range** to **calibrate** read-out electronics.
- **128 boards** (with **128 channels** each) are needed to calibrate 182,468 cells!

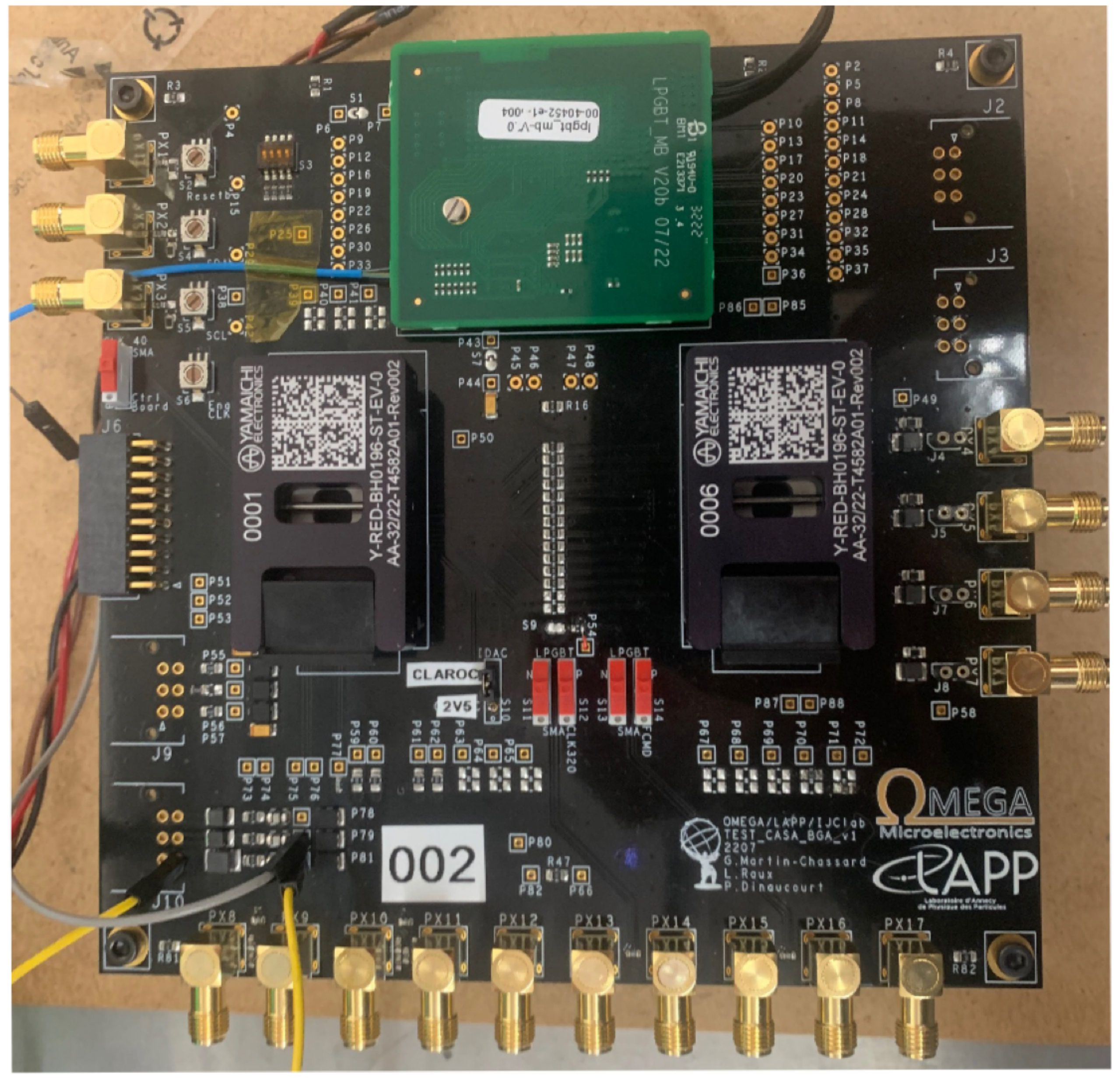
CLAROC custom ASIC

- **Creates pulse** by opening high frequency (HF) switch.
- Based on 180 nm HV-CMOS (XFAB) technology. → Needed to **cover full dynamic range**.

LADOC custom ASIC

16-bit **Digital to Analog Converter**, commands HF switch (based on 130 nm TSMC technology).

LADOC / CLAROC test board



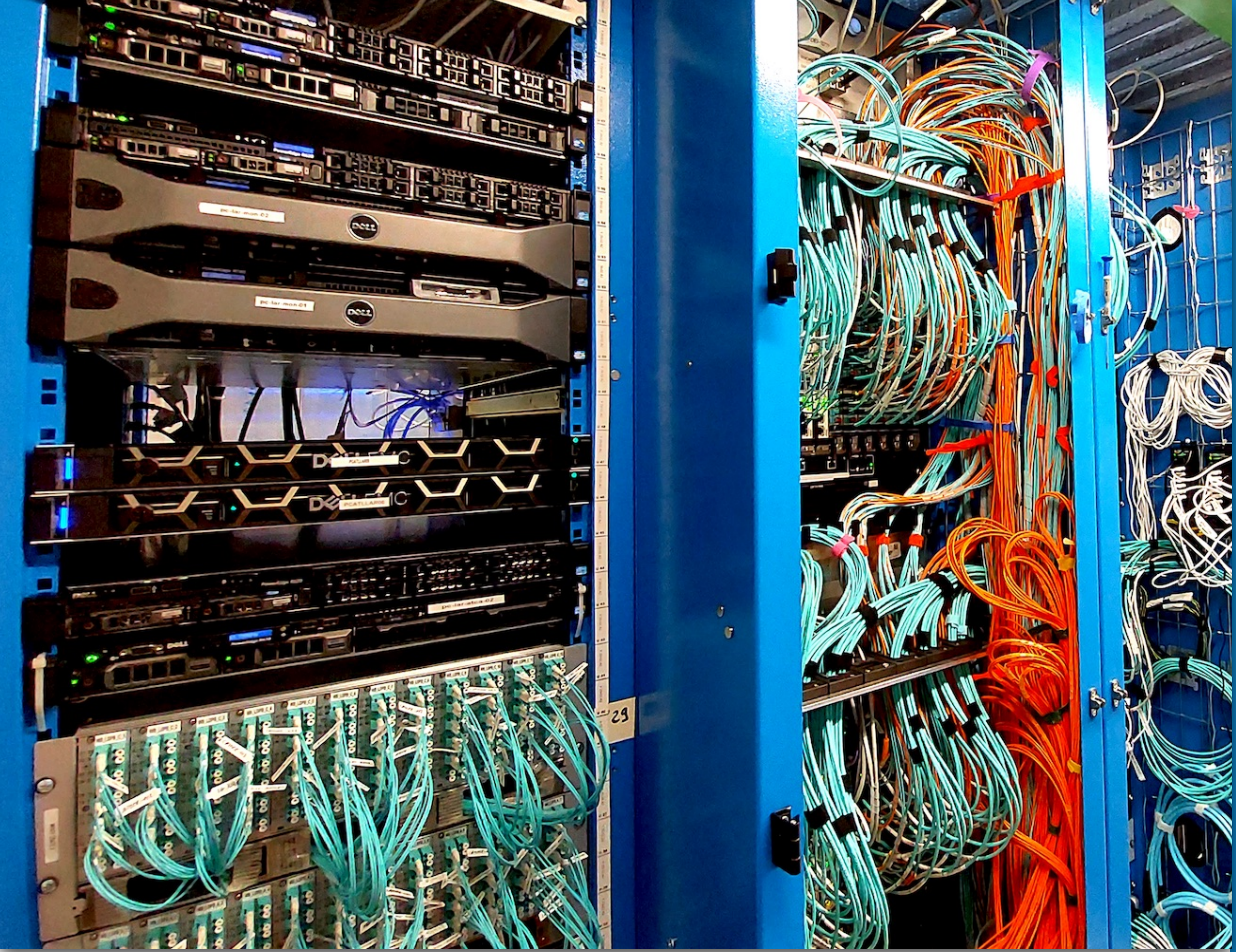
Key results

- Both ASICs in their current version (CLAROCv4 and LADOCv2) exceed **linearity requirements of a factor between 2 and 10!**
- Further radiation testing of ASICs is ongoing.

	Integral non-linearity requirements
High gain (low current = 0-5 mA)	0.1%
Intermediate current range (0-200 mA)	0.2%
High and very high current range (0-300/320 mA)	1-2%

Outlook

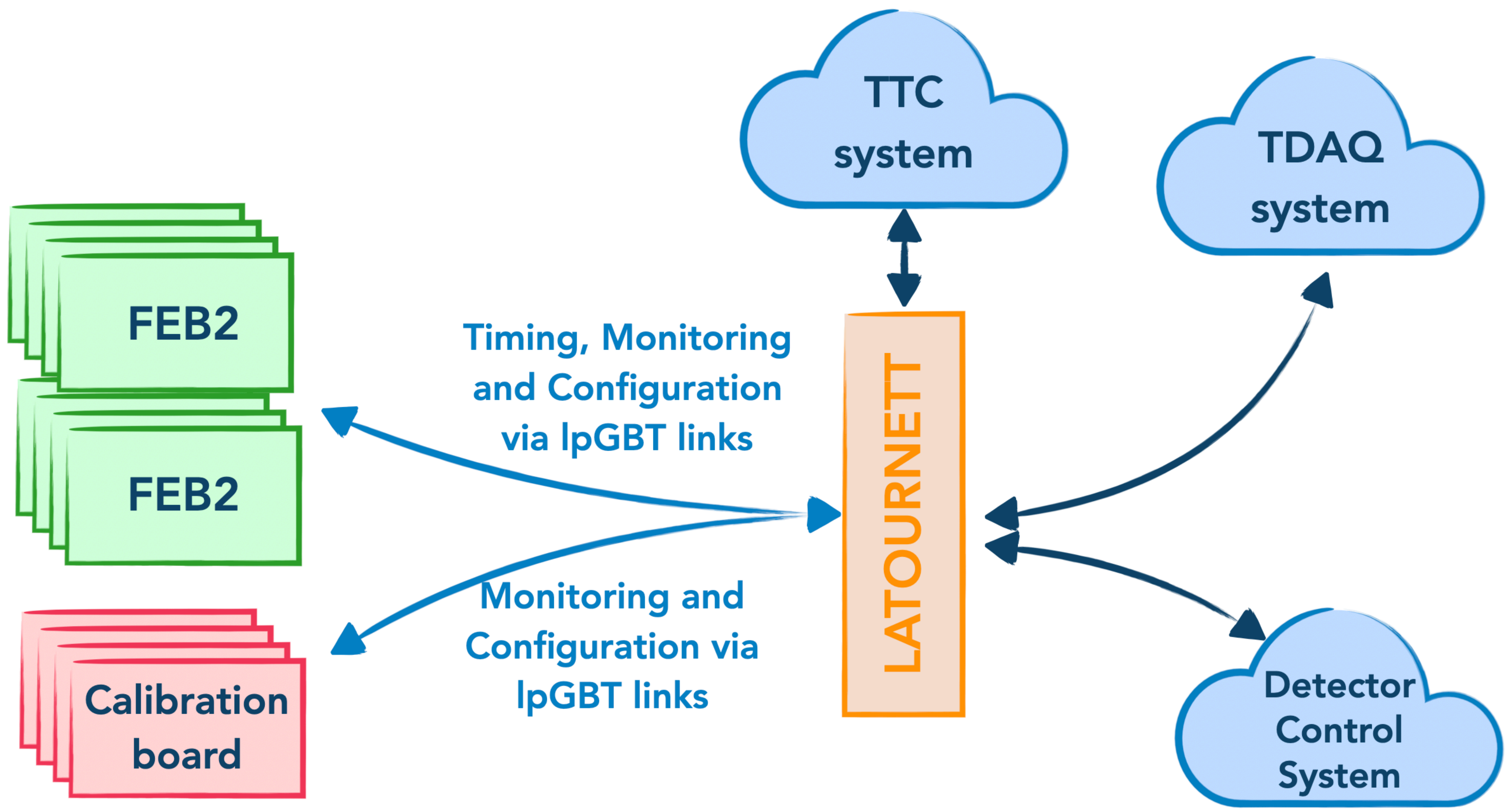
- Construction of second version of **full-scale board** (CABANEv2) **in progress**.
- Both ASICs **entering mass production**: LADOCv2b is the **final version**, now in mass production, while CLAROCv4b is submitted.



Off-detector electronics

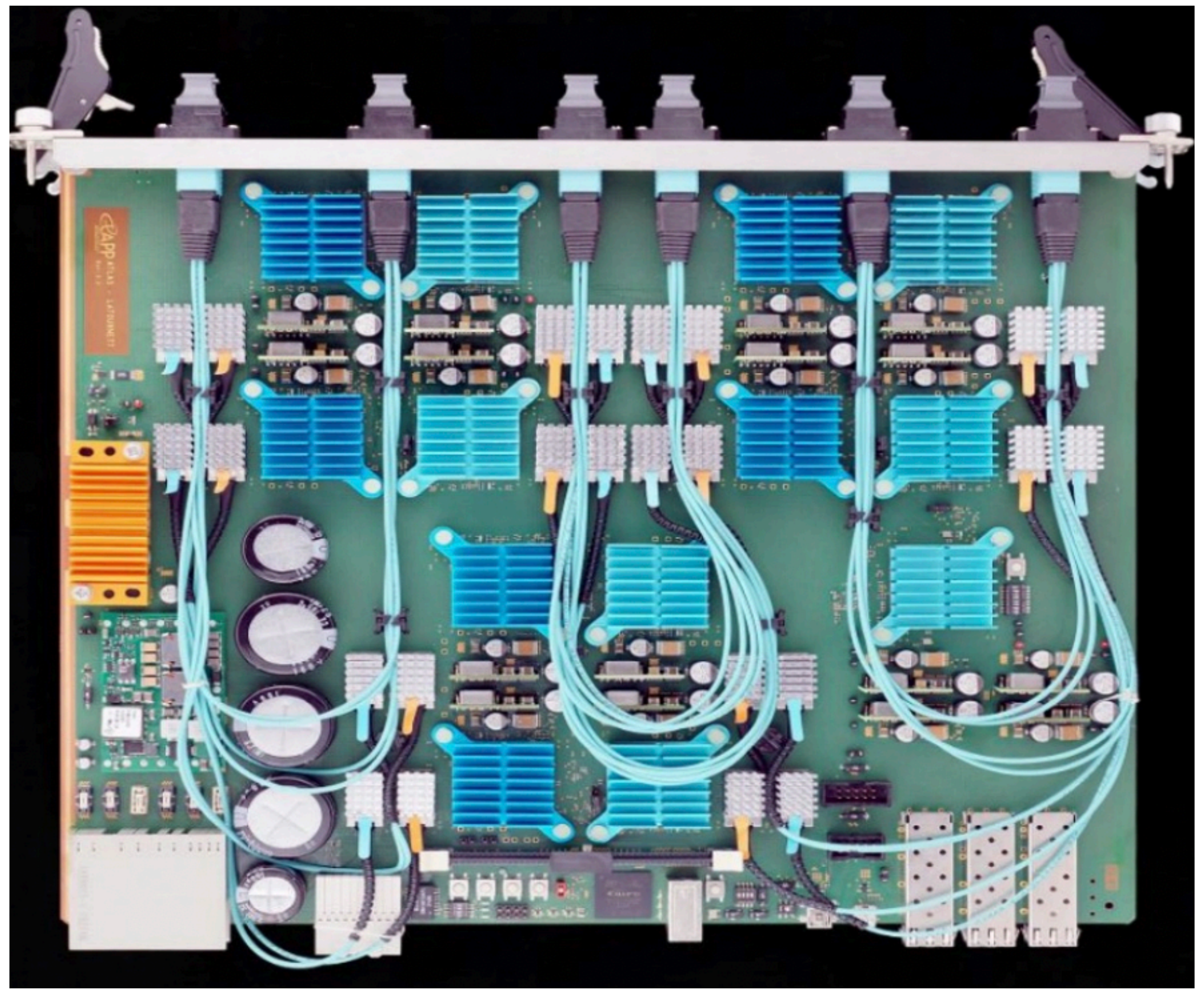
LAr timing system (LATS)

3



- The **LAr timing system** (**LATS**) handles Trigger, Timing and Control (**TTC) distribution, configuration, and monitoring** of the **FEB2** and **Calibration** boards, relying on **lpGBT protocol**.
- **30 LATOURNETT ATCA blades**.
  - Each equipped with **1 central + 12 array** Cyclone 10 GX **FPGAs**.
  - **Each controls 72 on-detector boards** with two dual links for redundancy.

LATOURNETT v1



Key results

- Completed **test board design** and prepared **test bench**.
- First full prototype cabled, and passed basic electrical tests.
- Proposed architecture for **integration** with **ATLAS TTC and TDAQ systems**.
- First integration tests with FEB2 and Calibration board ongoing.

Outlook

- Fabrication of second prototype (**LATOURNETT v2**) **to start in early 2025.**
- **New integration tests** foreseen after the hardware becomes available.
- **Software and firmware development ongoing** with **LATOURNETT v1** and FPGA devkits.

LAr signal processor (LASP)

4

The LAr signal processor (LASP) applies **digital filtering** to waveform from the FEB2, calculates **energy** and **time**, and **transmits to TDAQ** systems.

➡ Considering **ML architectures** to implement in FPGA for **energy reconstruction**.

LASP ATCA board (main blade)

- Receives data from up to 6 FEB2s (= **768 channels**) using lpGBT protocol at 10.24 Gbps.
- Computes energy and time in real time (= for each LHC bunch crossing @ 40 MHz).
- **Sends output** to the trigger system **at 25 Gbps**.
- Data is buffered for $\sim 10\ \mu s$ until a trigger decision is reached.
- Upon a trigger accept, data is sent to the DAQ system.
- Implemented using two **Intel Agilex** FPGAs per blade.

Smart Rear Transition Module (sRTM)

- Complements LASP main blade.
- Used for data transmission and TTC integration.

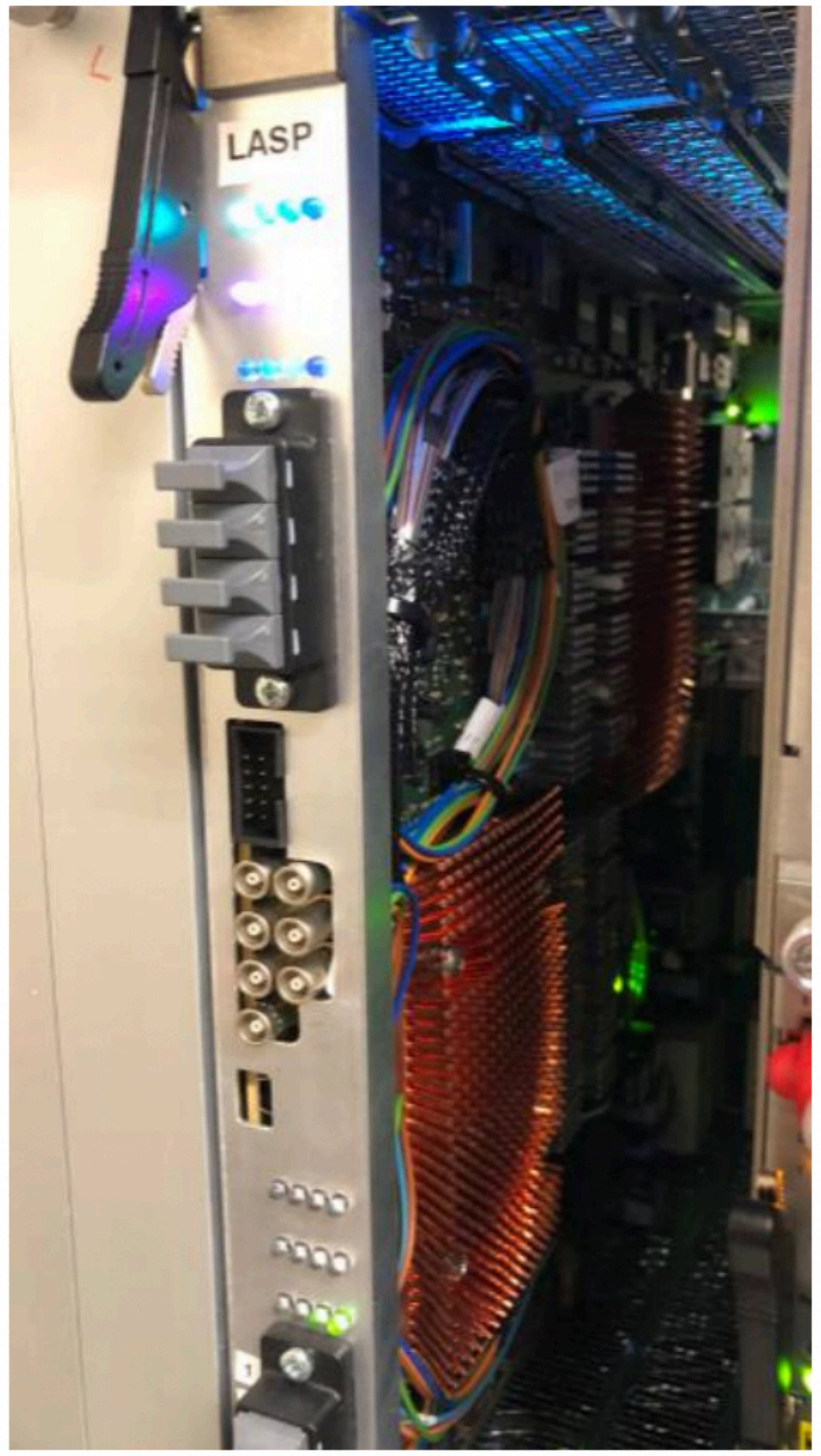
Key results

- A first set of test boards are produced, and are continuously running in test bench.
- **Regular monitoring** of **temperature**, **voltage** and **current** in place.
- Validated power, I^2C sensors, and FPGA configuration.

Outlook

- Work ongoing on the firmware, aiming to **optimize** FPGA **resource usage** and **power** consumption.
- Prototype for LASP blades and sRTM being finalized (foreseen for June 2024).
- **Long series of tests** in stand-alone and within the full system are foreseen for this year, to **verify TDR specs**!

LASP test board



Summary

- **On-detector** and **off-detector electronics for the LAr Calorimeters** are being re-designed, to cope with the **challenges** of **data taking** conditions at **HL-LHC**.
- All electronics will be **replaced** by **2029**, and are designed to **run** throughout the **full HL-LHC operation** (~ **2041**).
- Major **progress** on **LAr Phase 2 upgrade**:

FEB2

- **Promising test results** on **FEB2 pre-prototype**, and **new full-size FEB2 prototype ready** and now being tested.
- **First large-scale integration test** of the full readout chain is expected for **Summer 2024**.

Custom ASICs

- Custom ASICs **meet / exceed specifications**!
- ALFE2, COLUTA, CLAROC and LADOC ASICs **now entering mass production**.

Calibration board

Fabrication of second version of **full-scale board** in progress.

LATS

Fabrication of new **LATS prototype** to start in **early 2025**, then **additional stand-alone and system integration tests** are foreseen.

LASP

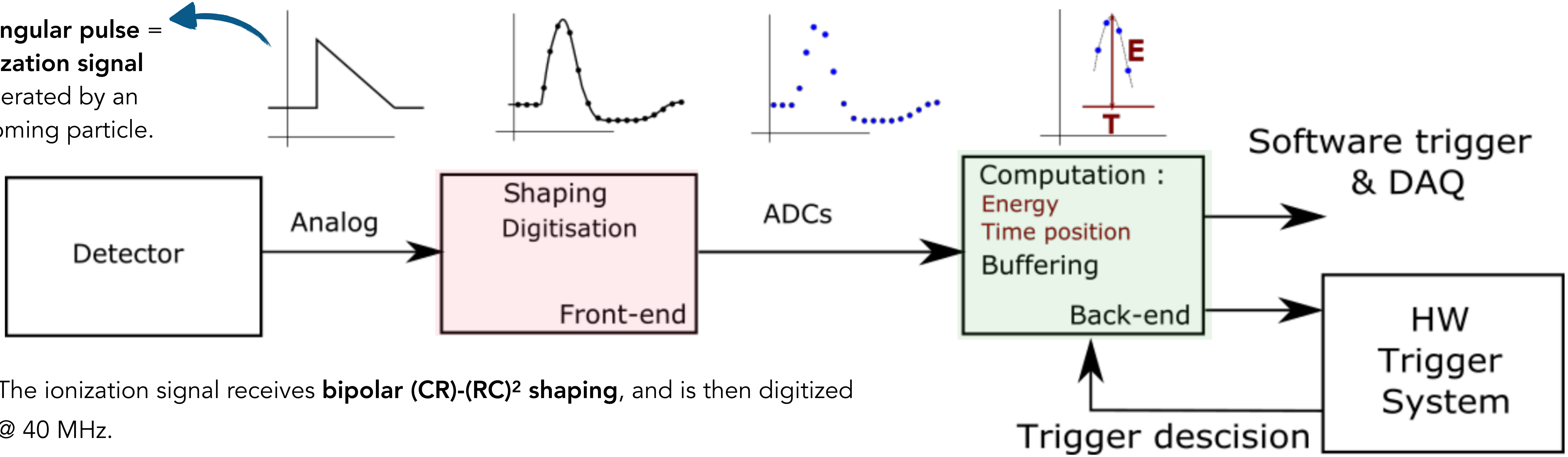
- **Prototype** for LASP blades and sRTM **being finalized** (foreseen for June 2024), and **work on firmware ongoing**.
- **Long series of tests** in stand-alone and within the full system to **verify TDR specs**.

On schedule for installation into ATLAS cavern after the end of Run 3!

Thank you for your attention!

Principles of the LAr HL-LHC readout

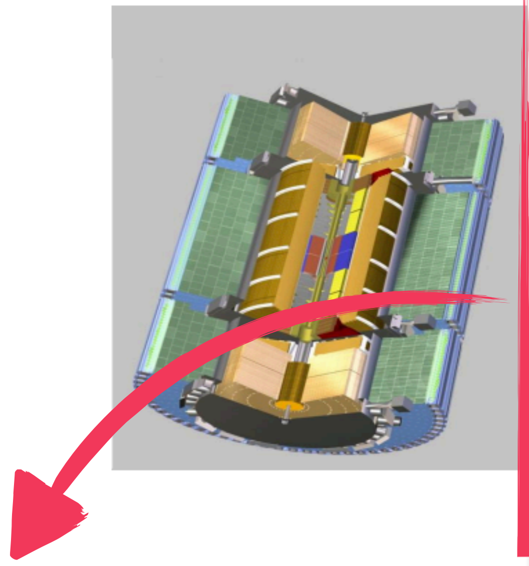
Triangular pulse = **ionization signal** generated by an incoming particle.

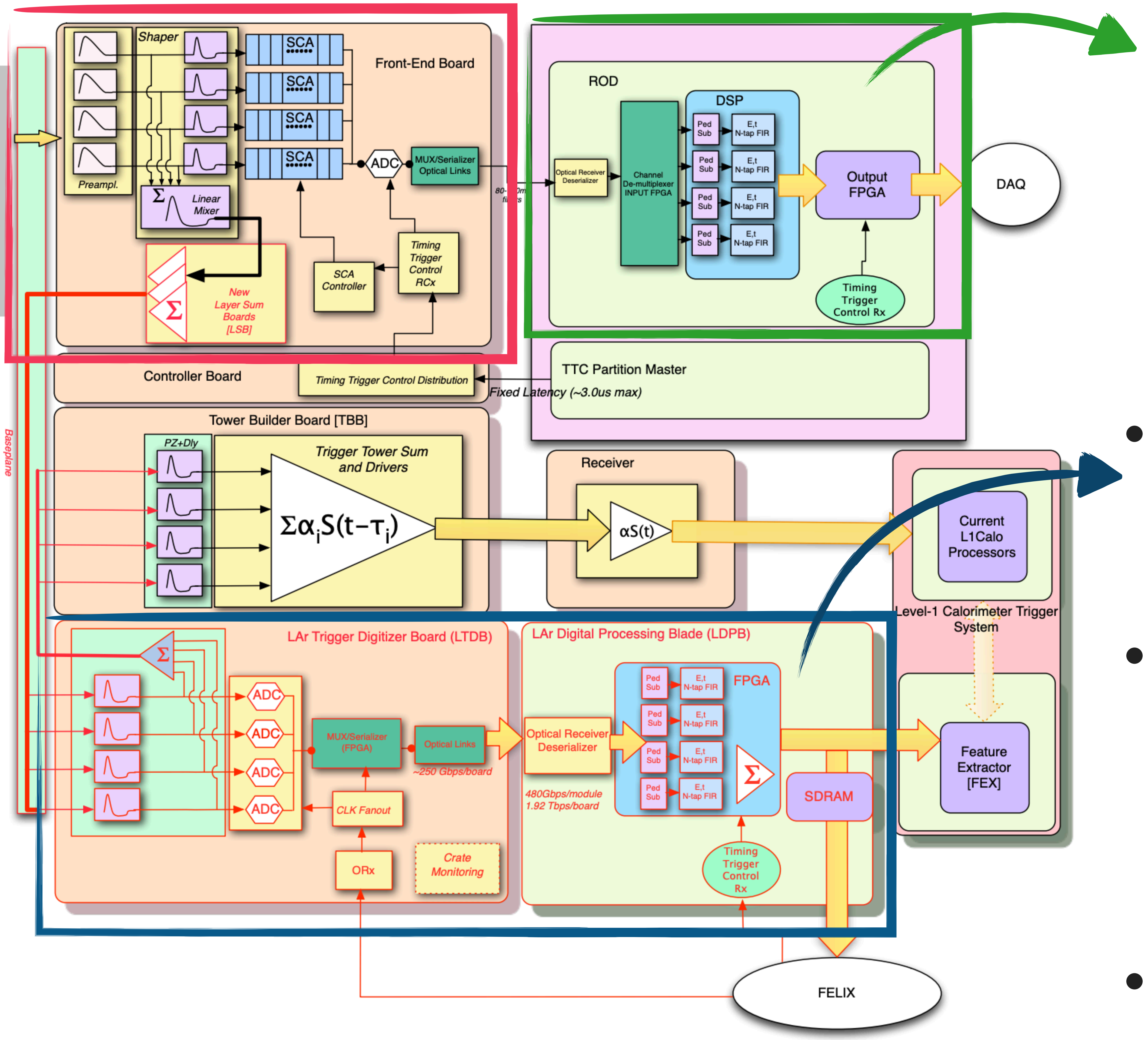


ATLAS Level-0 trigger @ 1 MHz!

- The ionization signal receives **bipolar (CR)-(RC)² shaping**, and is then digitized @ 40 MHz.
- The **digitized data** are **sent off-detector** to the TDAQ system.
- The **off-detector electronics** process the digitized signals to extract **energies for each cell** and compute **time position of the pulse** (= real time computation for the **trigger system**, which **receives full granularity calorimeter information**!). → **Crucial** for **discriminating physics signals from pileup** in **highly dense environments**!
- **Data is buffered** with a latency of 10 μs **off-detector**.
- Upon a trigger accept, the **full precision data stream** is **sent to the DAQ system**.

Principles of the current LAr readout





Each **ROD** receive digitized data from up to 8 FEBs, and **calculates energy, timing, and quality of the pulses** to send to the DAQ system.

- Signals from the calorimeter cells are read out by the **Front End Boards (FEB)**.
- The FEB2s perform **analog processing** of the signals (= preamplification + shaping and splitting in **three gain scales**).
- **Analog signals** are **summed** on the new Layer Sum Boards (LSBs), forming coarser "Super Cells", and **sent to the LTDBs**.
- **Full granularity calorimeter data** is **buffered on-detector**, waiting for a trigger decision.
- Upon an Level 1 trigger accept (rate = ≈ 110 kHz), **signals from the optimal gain scale** are **digitized** by a 12-bit ADC, **serialized and transmitted off-detector** to the DAQ system.

- The **LTDBs digitize** the **Super Cell signals @ 40 MHz**, and send the digitized data off-detector to the LDPBs.
- The analog Super Cell signals are also sent to the **Tower Builder Board (TBB)** which performs **analog sums** for the **legacy analog trigger** (now **being decommissioned**).
- The **LDPBs** convert the **digital Super Cell data** to **energies** in real-time and **send inputs** to the **Level 1 digital trigger**.