Dedicated front-end and readout electronics developments for real time 3D directional detection with MIMAC

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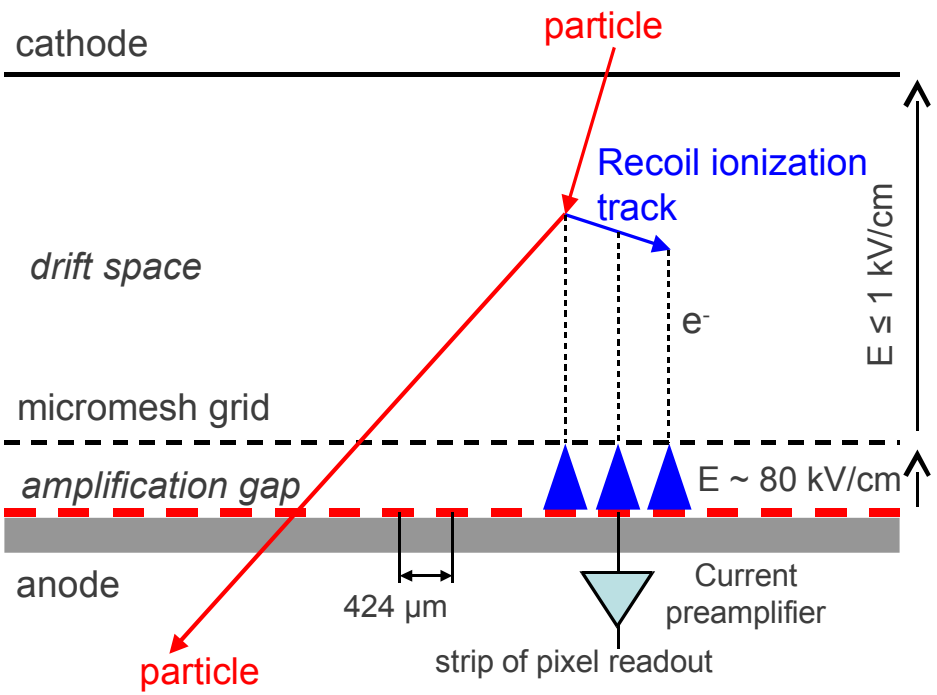
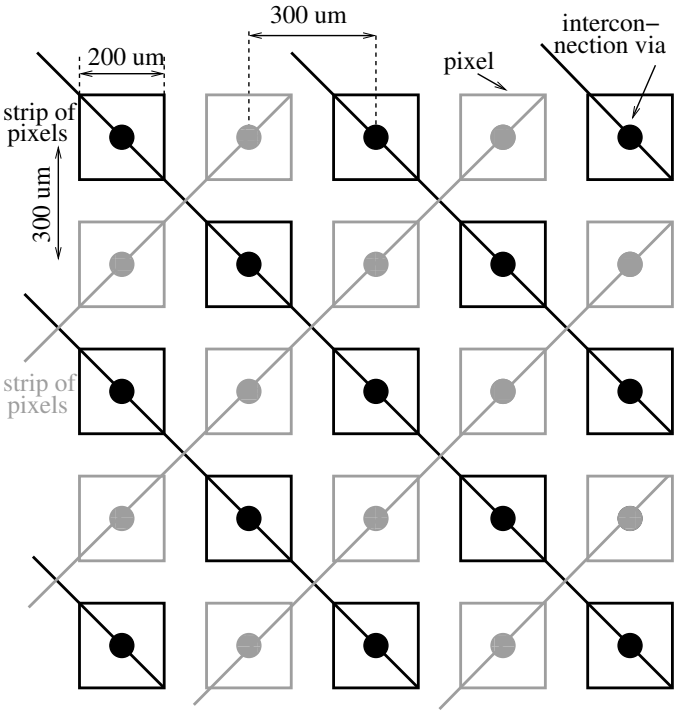
MIMAC detector

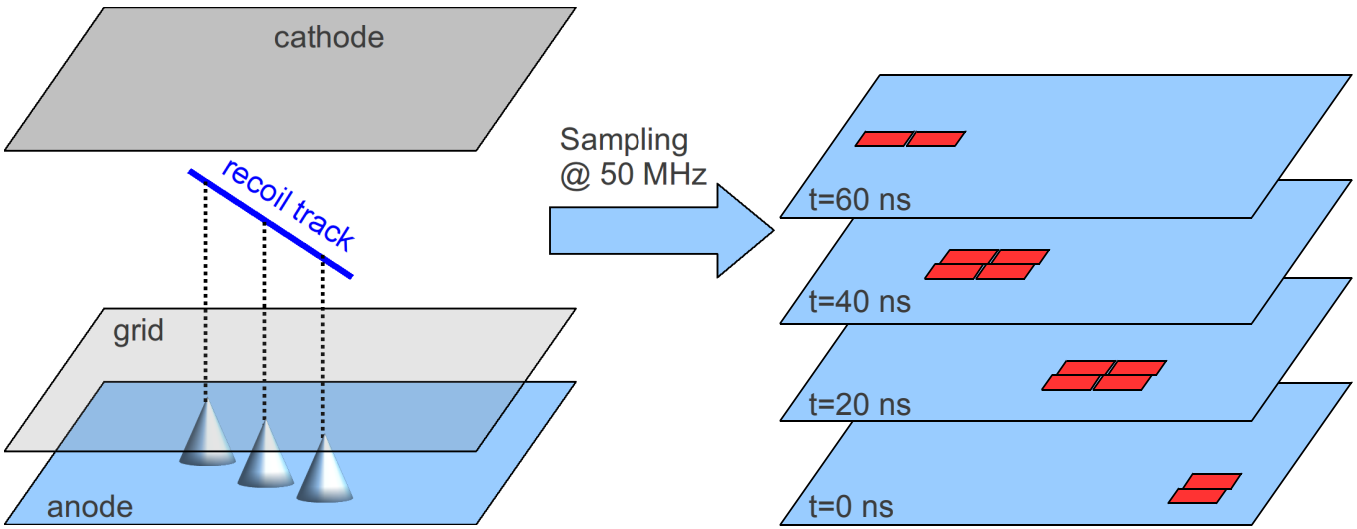




- Pixels are connected in line → "strips of pixels"
- Fired pixel coordinate → coincidence between X and Y strips
- Strips readout by current preamplifier
- Instrumented prototype: 2 orthogonal series of 256 strips of pixels
- Recoil energy obtained by instrumenting readout the grid (CSP)

Access to the third coordinate

- Anode signals are sampled at 50 MHz (20 ns)
- Primary e^- known drift velocity $\rightarrow$ 3rd coordinate (Z)



- Multiplexed strip readout $\rightarrow$ each time slice picture is rectangular

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ASIC design

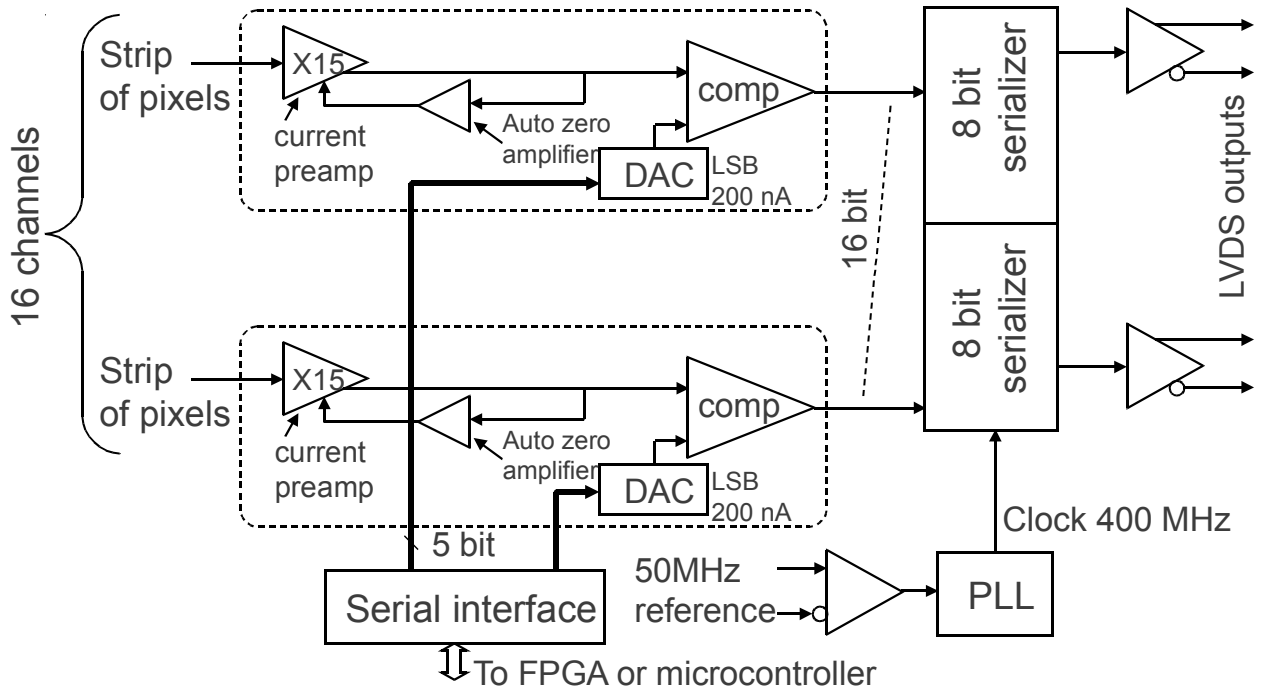
Motivations

- Final objective equip >2500 chambers of 1024 (512+512) strips of pixels
- Minimize: cost, space and power requirement

Specifications

- 64 channels per ASIC
  - balance between integration scale and complexity / yield / package
- Time over threshold → current preamplifier to keep signal shape
- Low current comparator threshold 200 nA, fixed by the worst case:
  - chamber gain 3000
  - recoil energy of 500 eV
  - recoil track parallel to the anode
  - maximum diffusion: 16 pixels fired (4 X strips and 4 Y strips)
- System integration ⇒ minimize board level interconnection

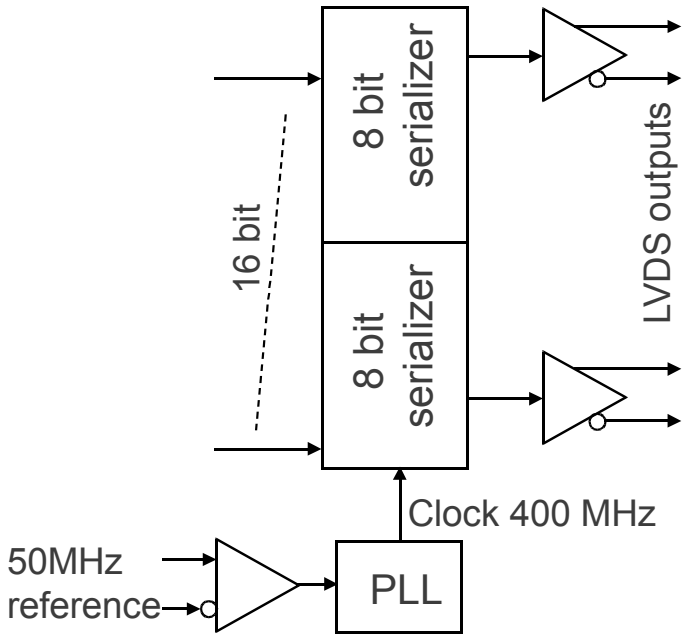
ASIC overview - analog part

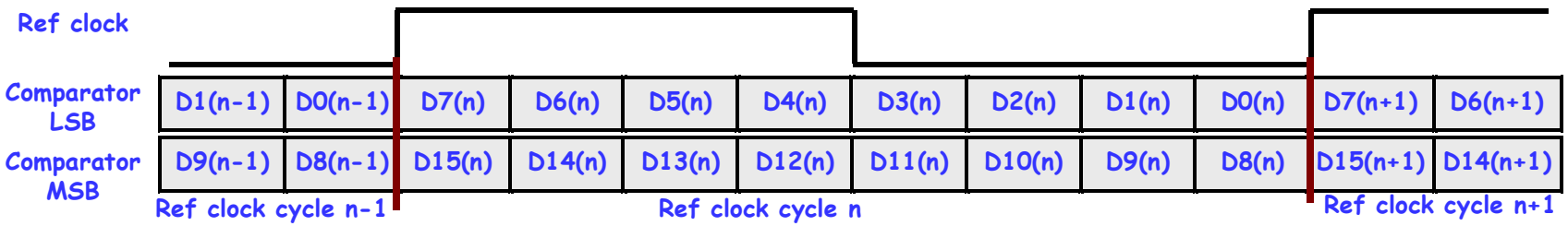


- ASIC composed of 4 groups of 16 channels
- Trade-off between DAC resolution and amplifier offset:
  - Offset cancellation → autozero amplifier (∼12 µs @ 1 Hz)
  - 5 bit DAC with 200 nA LSB (input equivalent: 13.3 nA)
- Fast comparator (modified CMOS inverter kept in linear region)

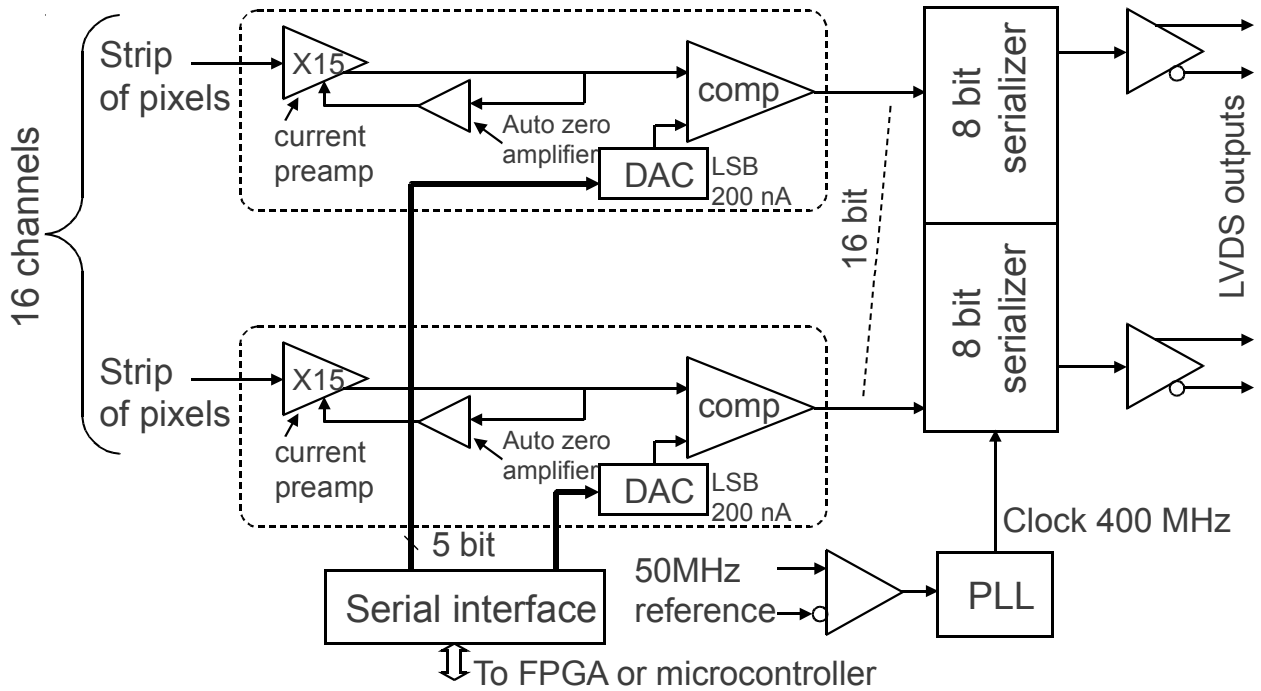
ASIC overview - digital interface

- Comparator output sampled and serialized
  - ⇒ interconnection reduced by a factor of 8
  - ⇒ **and** lower power consumption
- Using the same clock allows synchronous sampling between ASICs
- LVDS outputs (Low Voltage Differential Signaling) → lower noise





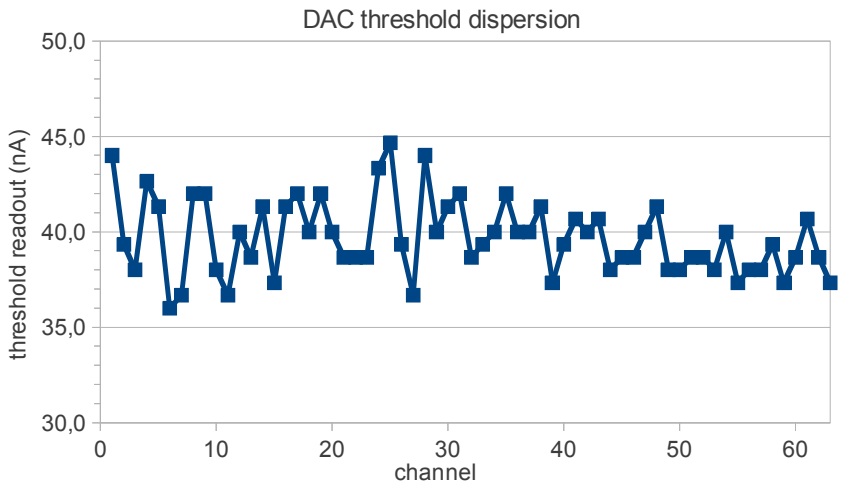
ASIC overview - slow control

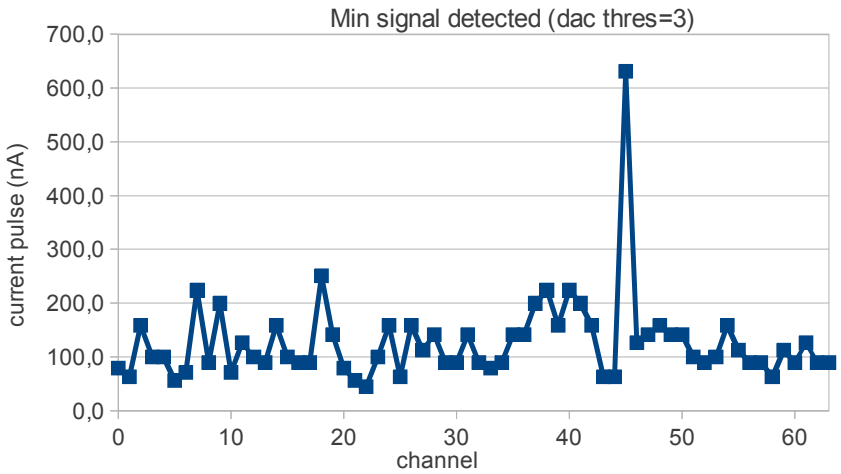


- Slow serial link is used to:
  - Configure the 64 DACs
  - Enable individually each channel (kill eventual dead channels, ...)
  - Provide the synchronization pattern (LVDS serial link)

ASIC performances (1/2)

- Total required power : 445 mW (110 mA @ 3.3 V, 55 mA @ 1.5 V)
- ASIC surface 3.9 mm x 5.8 mm = 22 mm^2 (AMS SiGe CMOS 0.35 µm)
- DAC threshold and minimal threshold dispersion over one ASIC

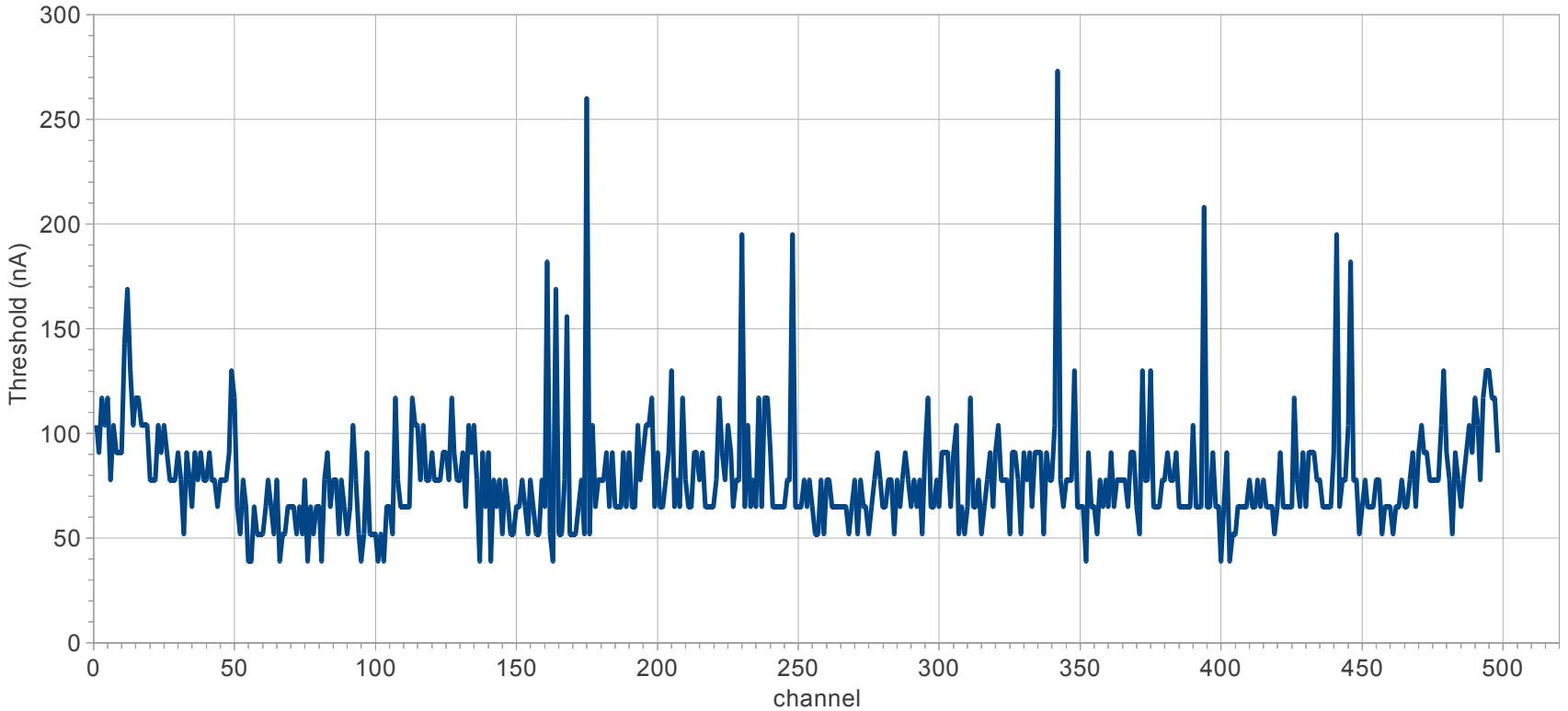




- Thresholds are homogeneous, but:
  - Offset correction dispersion influence on the minimum signal detected

ASIC performances (2/2)

- Minimal DAC threshold (above noise) in detector



- Excepted a few spikes (∼10), fairly homogeneous → allow proper operation
- All below maximum threshold of 413 nA (31 x 13.3 nA)

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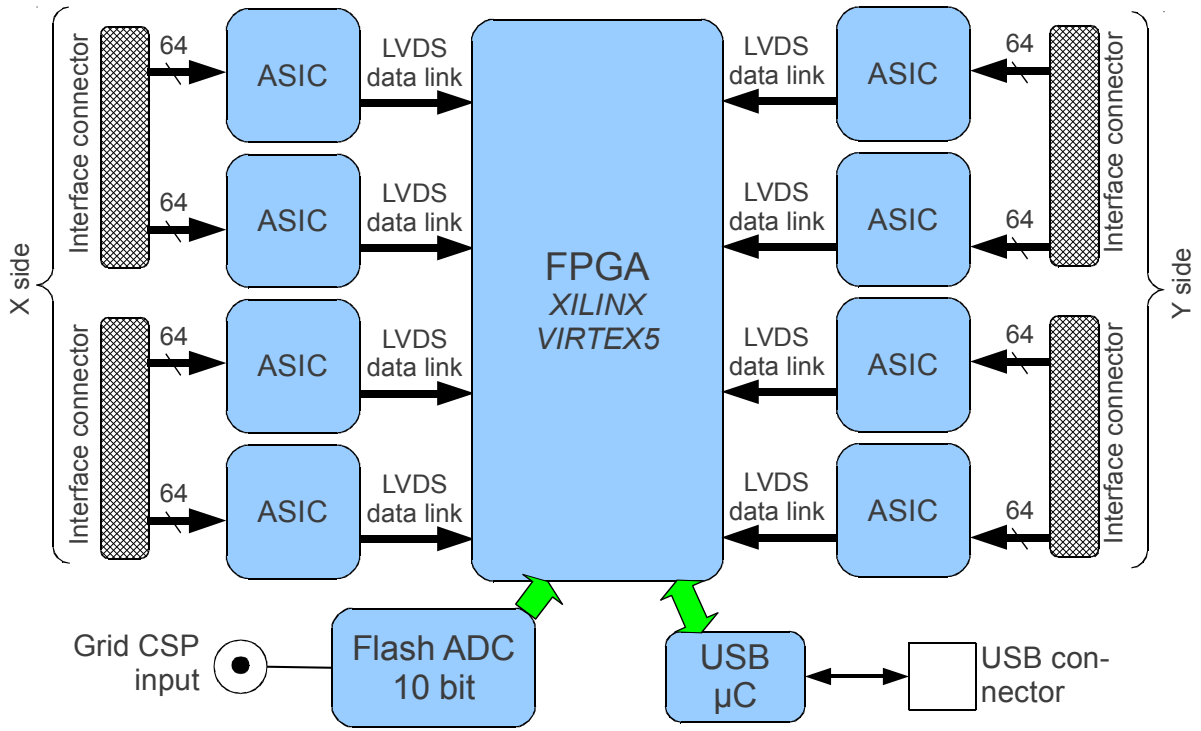
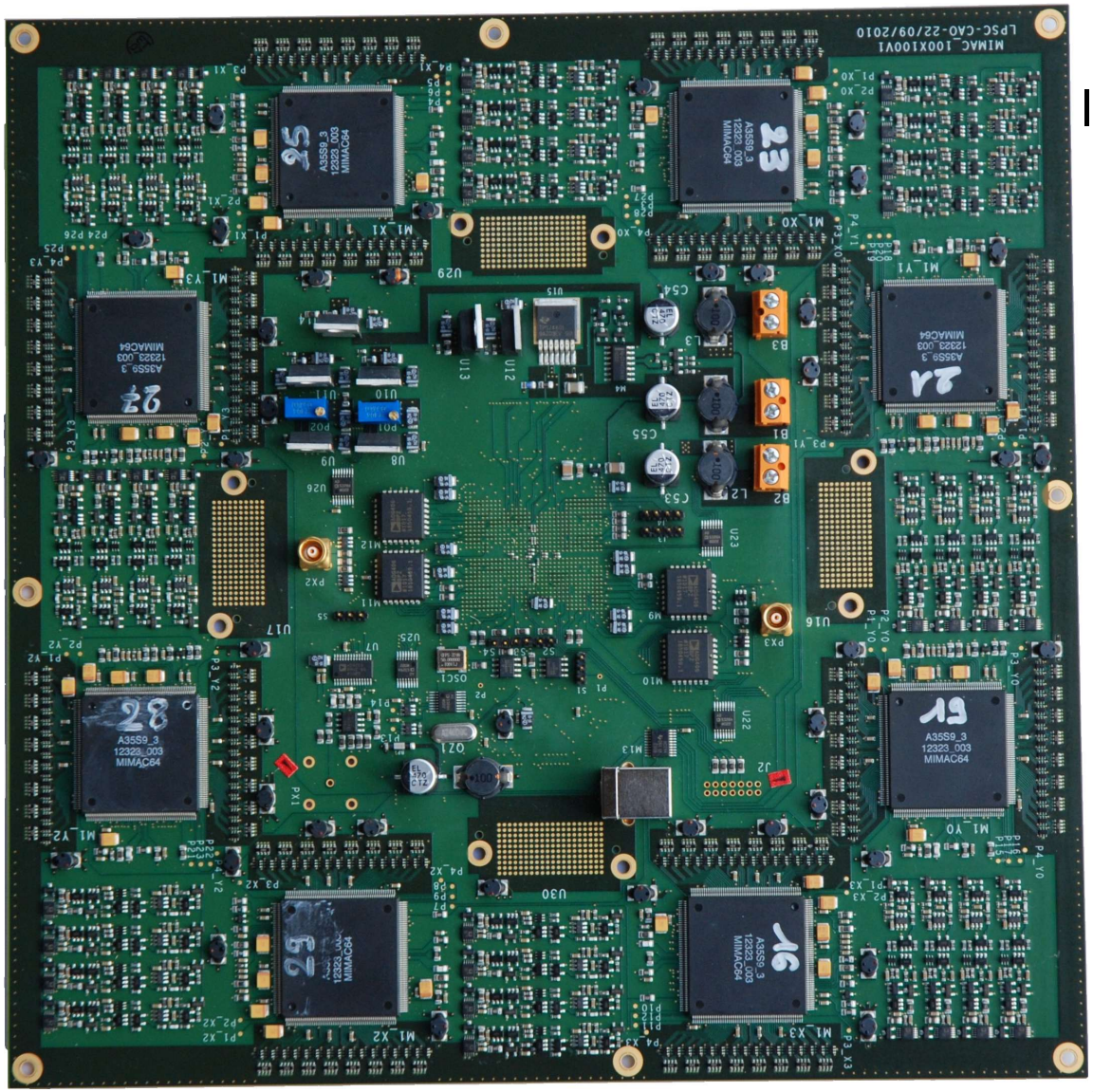
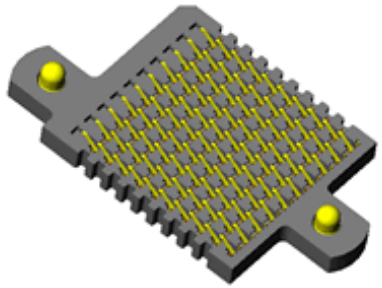
Acquisition board overview



- Auto-triggered system
- Grid signal is sampled at 50 MHz to have an **indirect** image of the energy deposit as a function of time (see J. Billard presentation)
- First level event building done in FPGA
- Readout and slow control performed via a USB interface

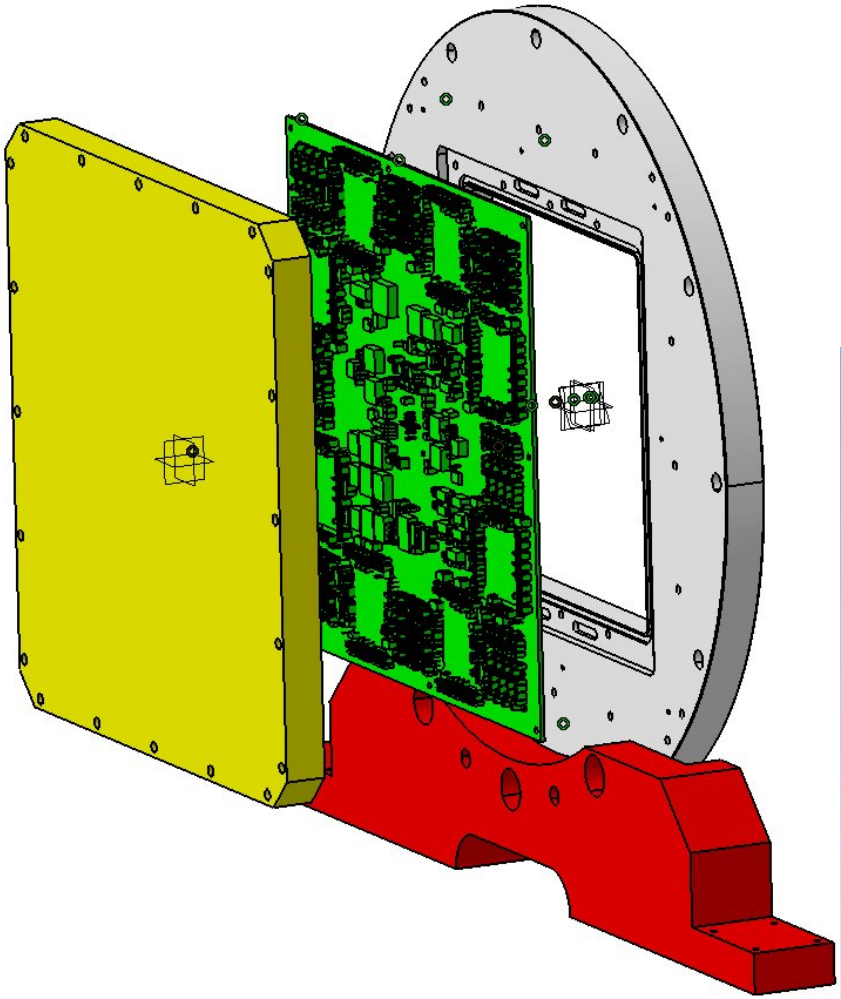


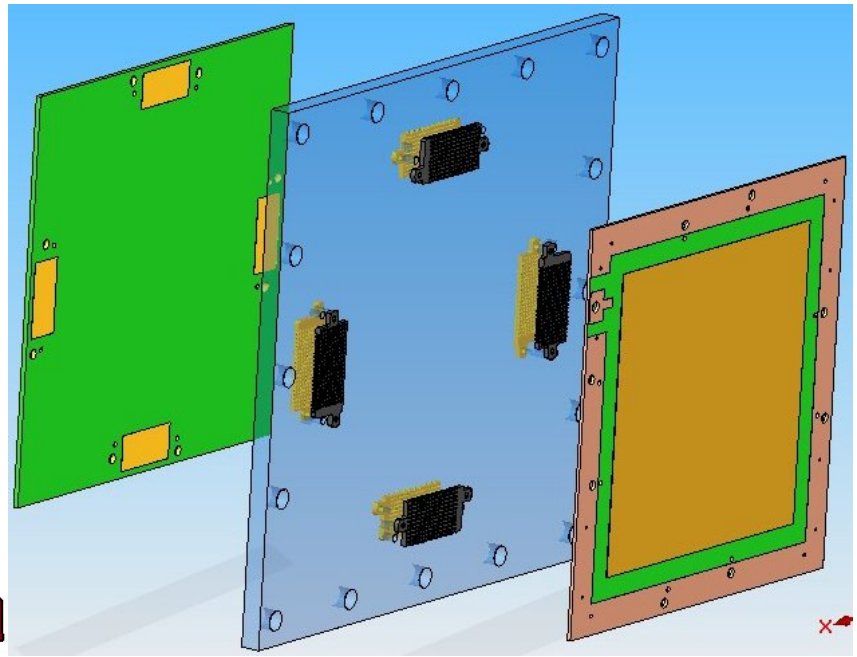
Interface connector between board and detector



- 25 cm×25 cm
- FPGA on the back side
- Discharge protection on each input
- 4 V @ 2100 mA
- 2 V @ 480 mA

⇒ 9.4 W

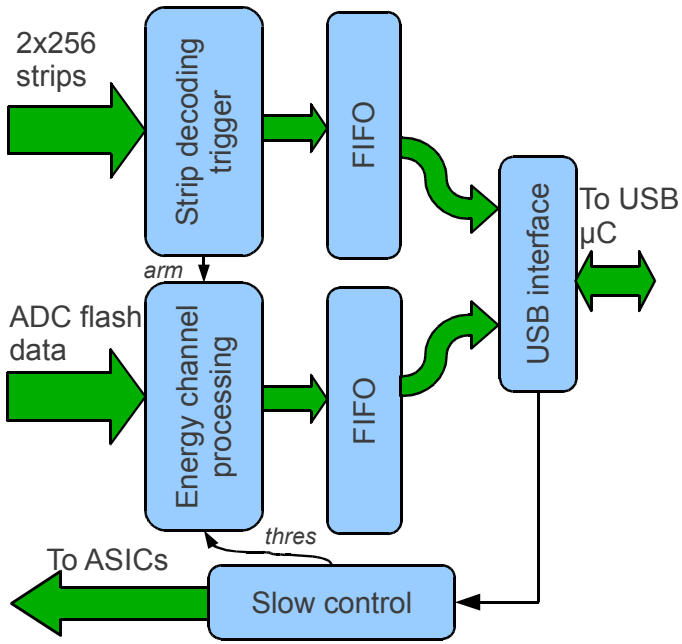




FPGA firmware overview

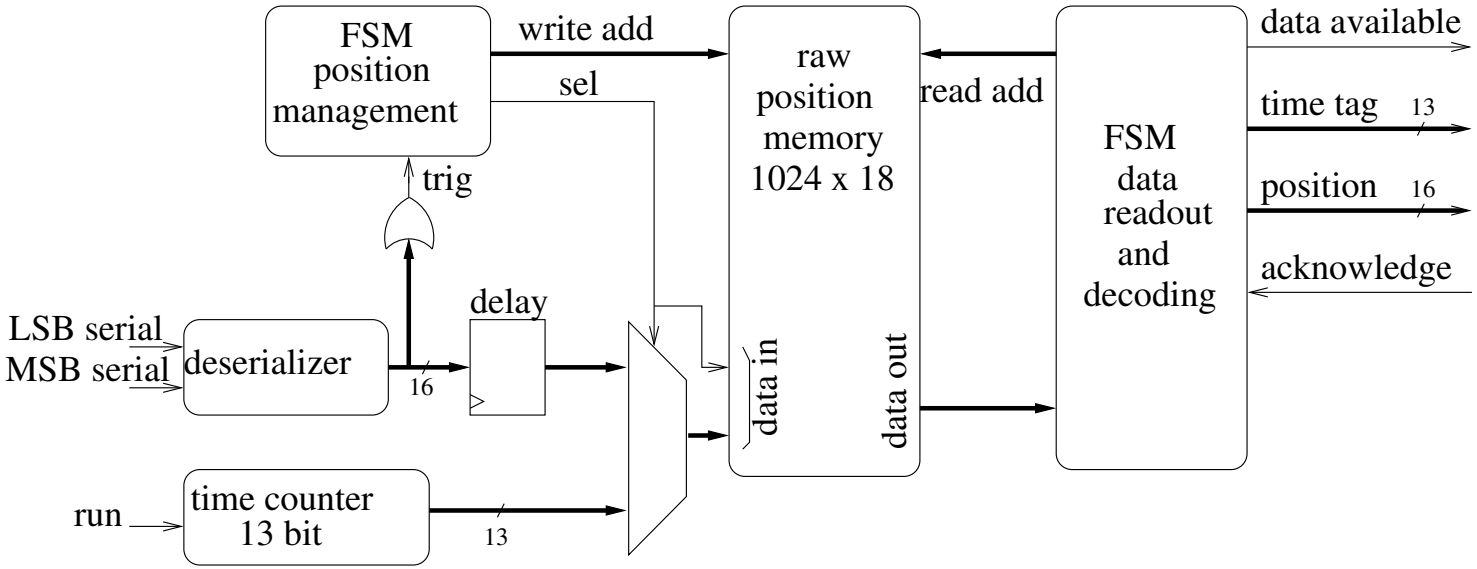
1. Current triggering strategy:
   - Trigger built with fired strips
   - X and Y strip coincidence required
   - Continuously triggering strips defines an event
2. Fired strips are recorded in intermediate buffers, decoded and written in output FIFO
3. Strip trigger used to arm energy measurement
4. Position and energy data recorded in separate FIFOs
5. Data readout and slow control by USB

Two parallel processing channels



ASIC interface and trigger

1. First level processing is done by group of 16 channels
2. The FPGA deserializes the data received from the ASIC
3. For each group of 16 channels a local trigger is built (OR)
4. If a coincidence exists between X and Y $\rightarrow$ local recording (start date + positions)
5. Primary electron distribution can be noncontinuous $\rightarrow$
   - Untriggered strips can split the track (clusters)
   - Stop recording condition $\rightarrow$ no trigger for more than n clock cycles



Position decoding (1/2) - Why?

- Most of the time a few strips only are fired $\rightarrow$ no need to transfer the unfired strips
- Data encoding implemented:

Bit #	12	[11..10]	[9..8]	[7..4]	[3..0]
Content	X or Y	ASIC#	Group#	0	ch#

- Example: for 2 strips fired in X and 2 in Y for the same time slice

X	Y
$(....0000000011000000....)_2$	$(....0001000001000000....)_2$

$\Downarrow$

$(0103)_{16}$	"X side, ASIC 0, group 1, strip 3"
$(0104)_{16}$	"X side, ASIC 0, group 1, strip 4"
$(1704)_{16}$	"Y side, ASIC 1, group 3, strip 4"
$(170A)_{16}$	"Y side, ASIC 1, group 3, strip 10"

$\Rightarrow$ Transfer 4 coordinates coded on 16 bits (=64 bit) instead of 512 bit

- Gain when less than 32 coordinates to transfer (for 2x256)

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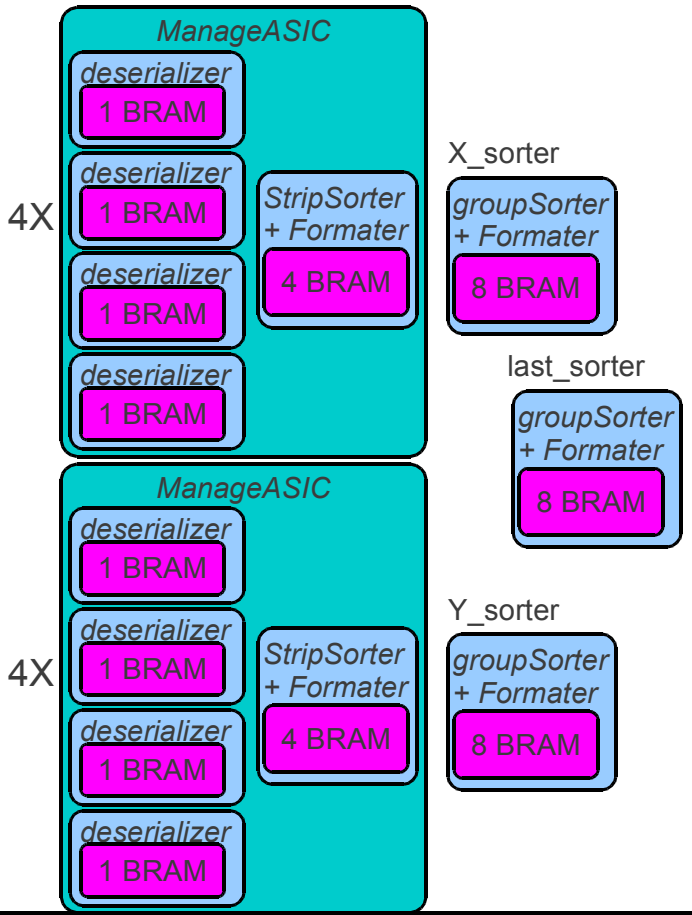
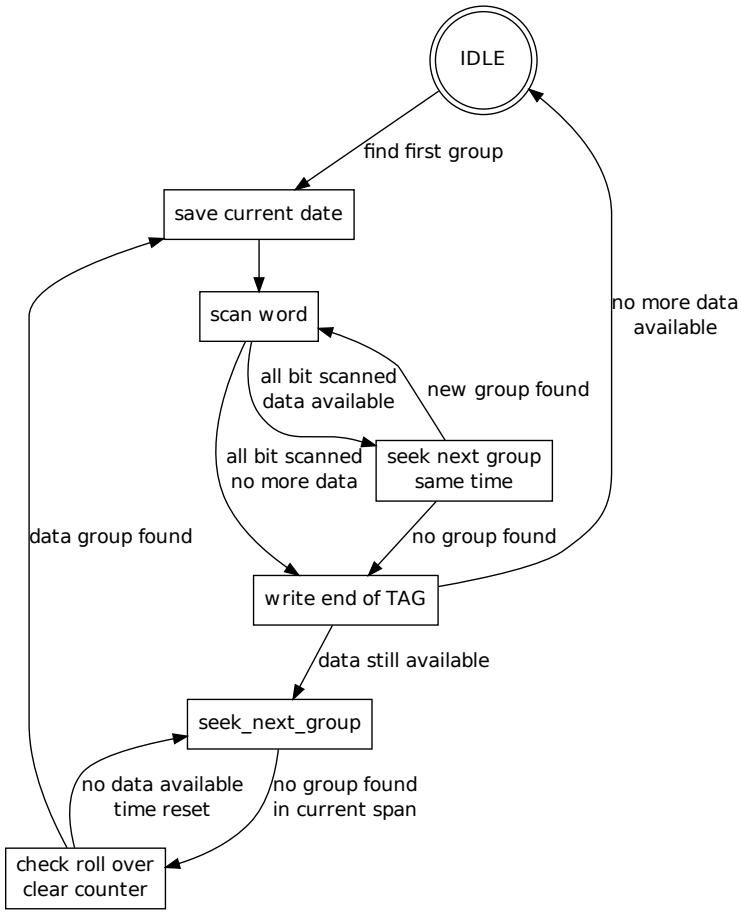
Position decoding (2/2) - How?

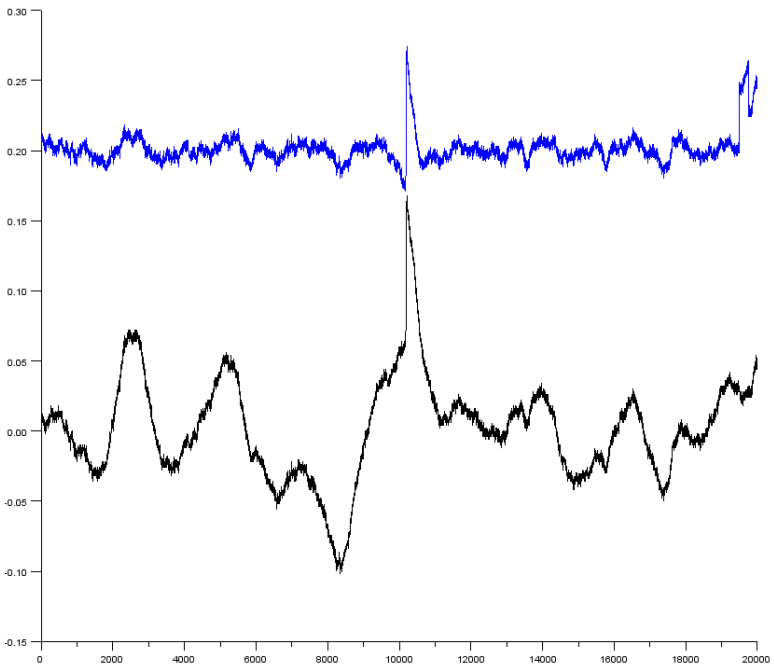
- X and Y parallel processing⇒ same time slice data association
- State machine search and aggregate data from the same time slice
- Decoding and association done in several stages

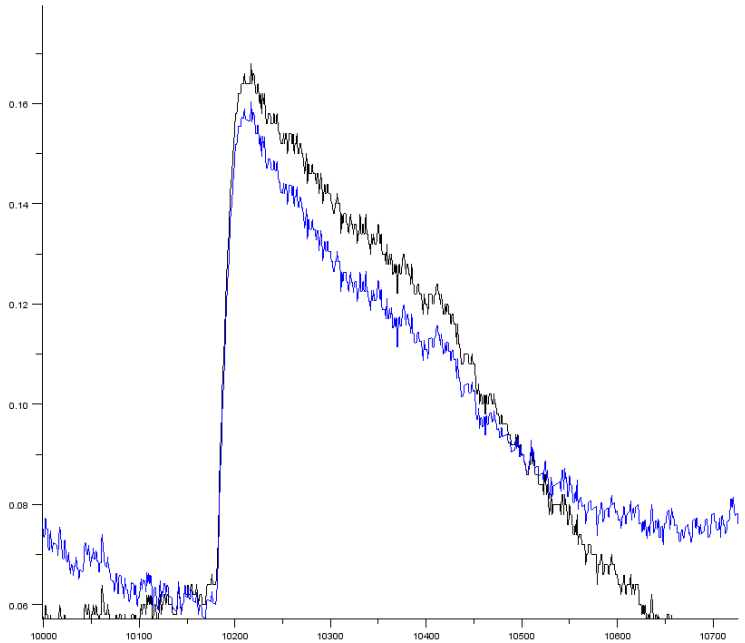




Focus on the energy measurement: filtering requirement

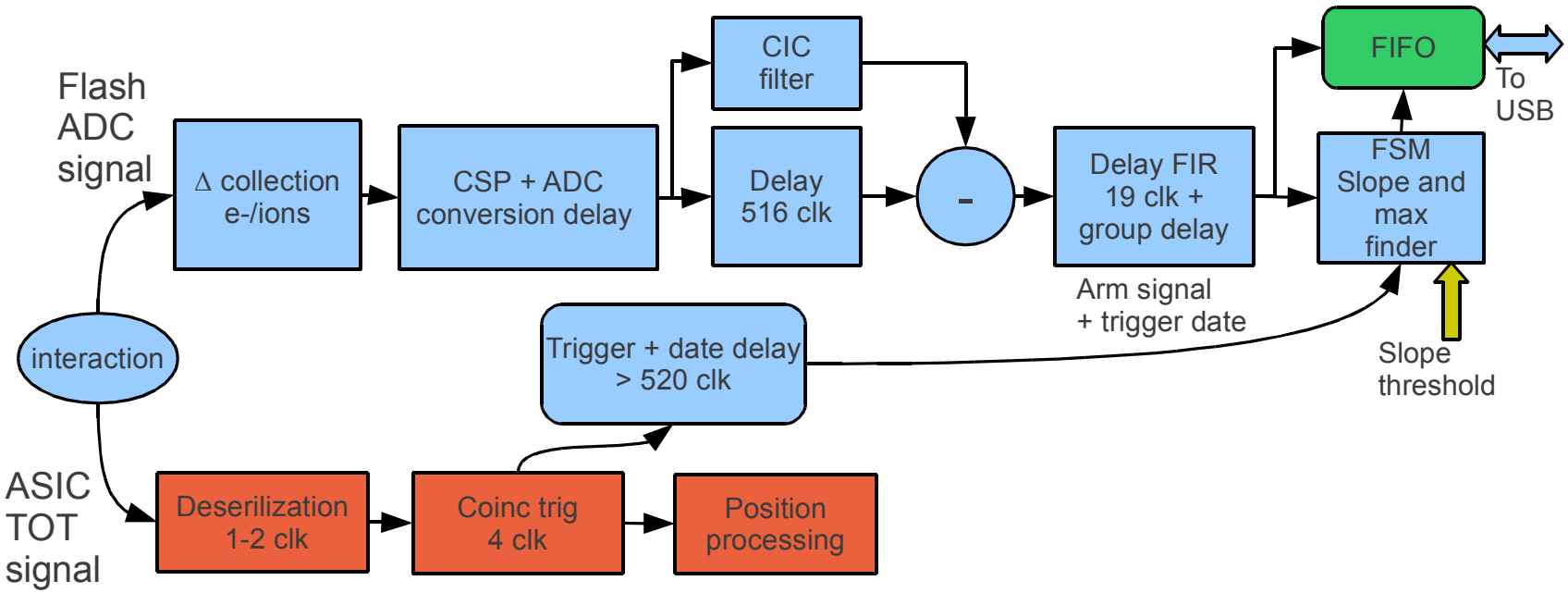
- Signal recorded is the integral of the charge deposit
- Due to the low level signal and noise, a simple discriminator is not enough $\rightarrow$ slope threshold, and frequency specific filtering
- Example of a filtering (CIC) with an extremely large noise level compared to the useful signal $\rightarrow$ no deformation





Focus on the energy measurement: implementation

- The energy recording is armed by the position triggering
- Actual recording performed when the grid integrated signal is steep
- Using slope condition is more robust and noise immune than using a simple level threshold.



- Time tag is delayed also to allow energy and position association

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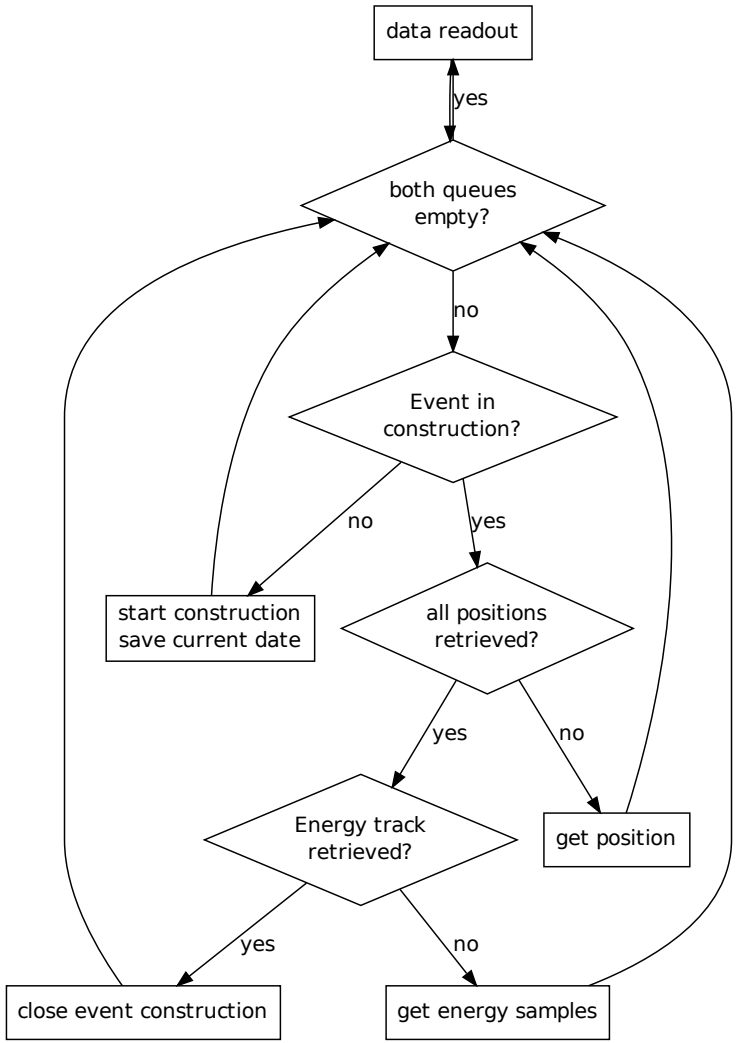
Hardware/software interface

- Readout through a USB2 micro-controller
- USB firmware and FPGA uploaded at start-up $\rightarrow$ flexibility for debug and update (remotely!)
- µC used only to transfer data as fast as possible $\rightarrow$ minimal complexity and great flexibility
- The board driver API is implemented in C++ and is called within an acquisition thread
- Read data are pushed in STL queues (FIFOs), one for position data and one for energy data
- Association between position and energy done at the computer level

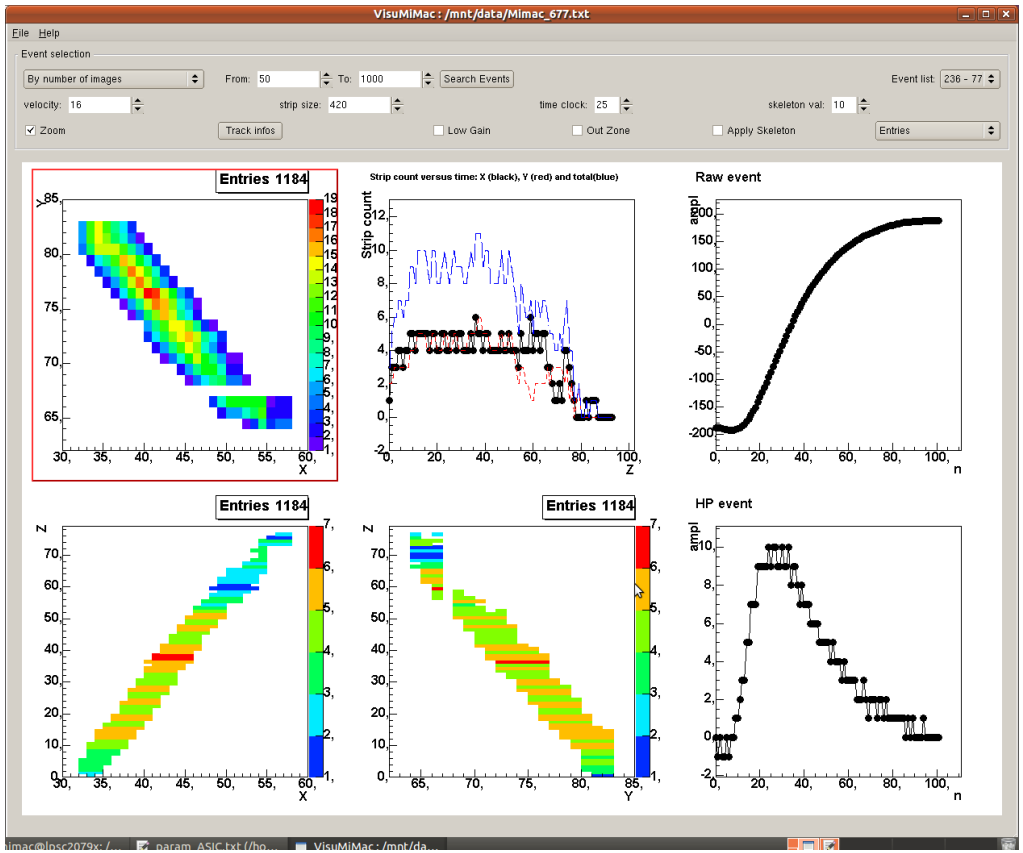
Event building

- Position information is provided in a list of X/Y coordinates fired per time slice
- Associate energy samples with positions
- An event is defined as (*almost*) continuously triggering strips
  1. Search continuous triggering position (in time)
  2. When time tag jumps by more than one look for energy with corresponding time tag



Real time display

- Graphical user interface developed in Qt, root and Qtroot layer
- 3 projections of the track are displayed
- Number of fired strips per time slice
- Track CSP signal and derivative displayed
- Possibility to search and display a recoil track (energy, duration, ...)
- Energy histogram of the run is built on line (other tab)



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Summary

- A complete solution was developed to instrument a MIMAC
- This solution can be extended to numerous chambers:
  - Several electronics connected per computer
  - The event building developed can be performed in several stages
  - BUT: need a common time tagging and synchronization upgrade (clock + start signal)
- Next steps:
  - Port this electronics to Modane underground facility (remote control software in development)
  - Develop the time synchronization hardware (long term)
  - Design the 2 x 512 (and final) version of the MIMAC DAQ board