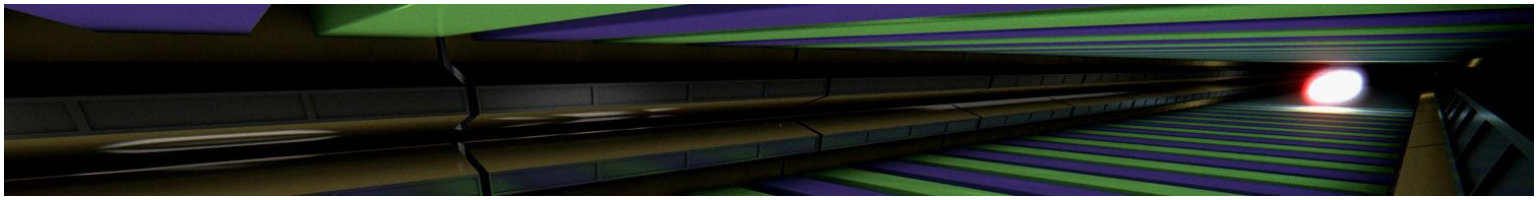


LLRF system for XFEL based on xTCA for Physics

Tomasz Jezynski
Frank Ludwig
for the LLRF - Team

Requirements

(...)
Standard for new accelerator for ALL subsystems
Support moder algorithms (distributed computation power)
High data throughput (DAQ)
Low latency links (control system)
Flexible configuration
Available for many years

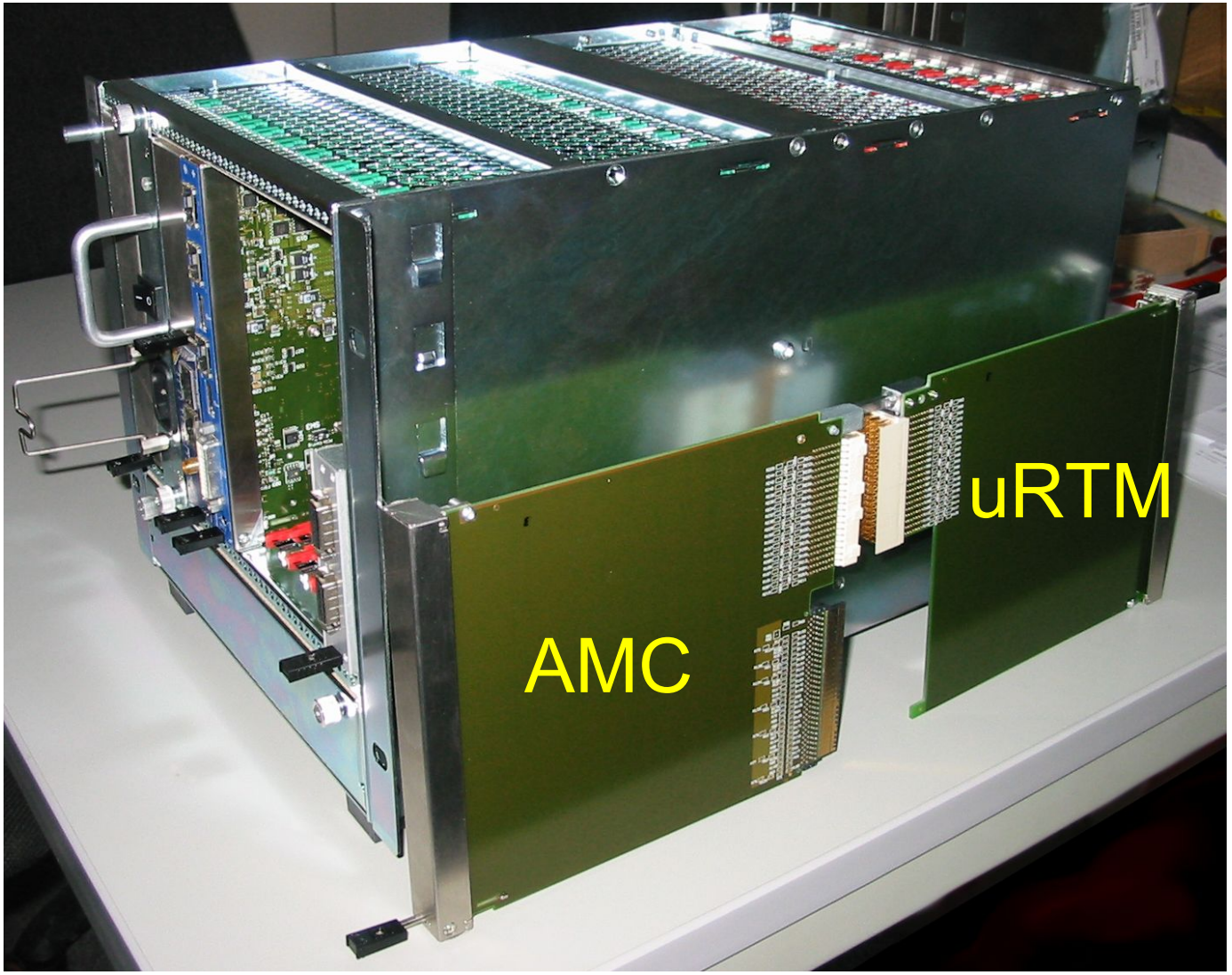
Standard (hardware and software)
* Flexible configuration
* In-build crate/board management
* Modern protocols

xTCA for Physics

Since xTCA has all attributes as standard, the Physics Community has initiated a Working Group to look at the specific requirements – PICMG **xTCA for Physics** Coordinating Committee

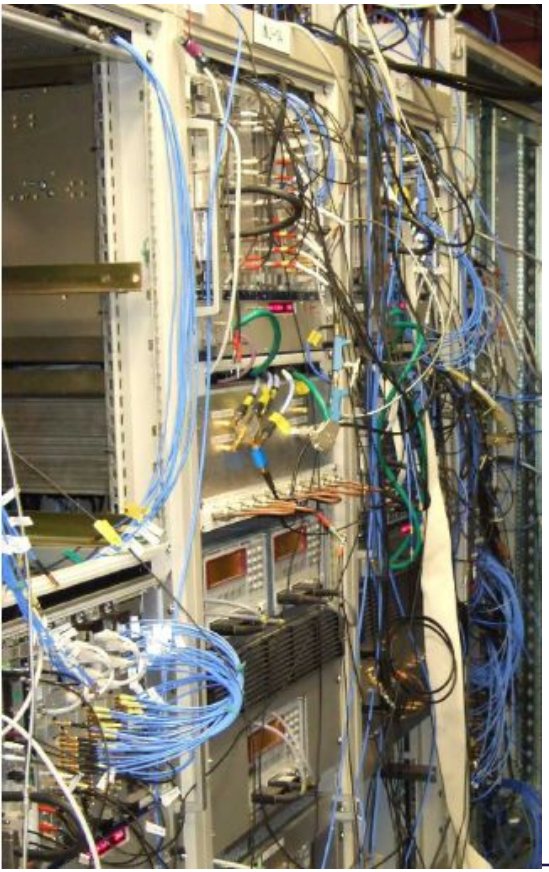
- **Goal:** to develop specification for physics community (instrumentation) and become a customer for industry (large number of orders according to existing specification)

xTCA crate for Physics

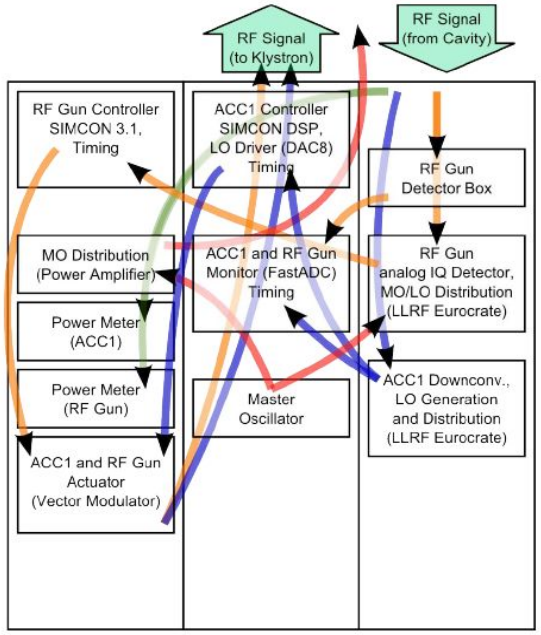


LLRF system for XFEL based on xTCA for Physics

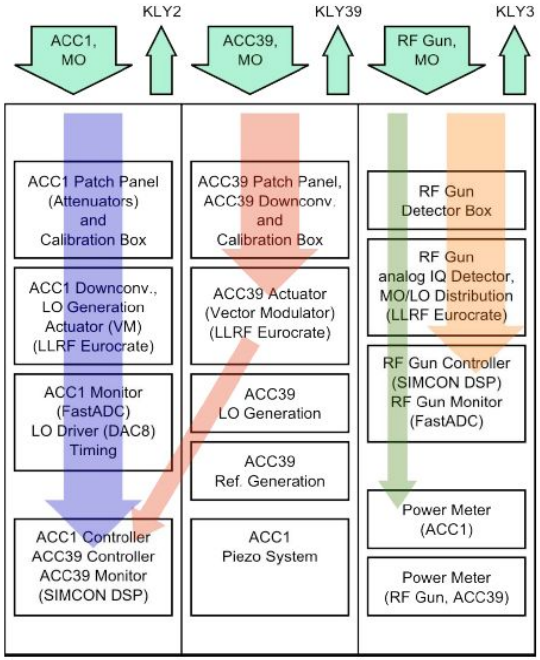
Upgrade of FLASHs LLRF System 2010



Previous LLRF rack layout



Current LLRF rack layout



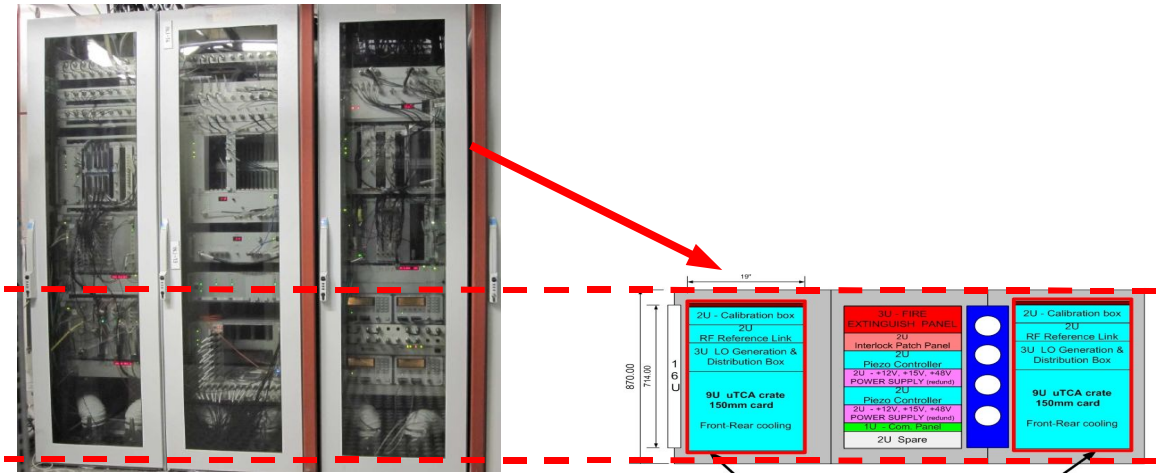
Energy stability improved
by factor of 3 to dE/E=0.5E-4.

Christopher Gerth, et. al.

FLASH & XFEL - differences

Actual FLASHs LLRF limitations

- Rack size is strongly limited (J0-16U, L1-26U) compared to (ACC1-42U)
- LLRF system is outside the tunnel
- Central FPGA concept (limited comp. power)
- Process only 8x3 cavity signals (P,F,R)
- SimconDSP 14-bit ADC limitation
- Baseband field detection
- No redundancy
- Pluggable connectors are not drift compensated
- No channel parallelization for more performance



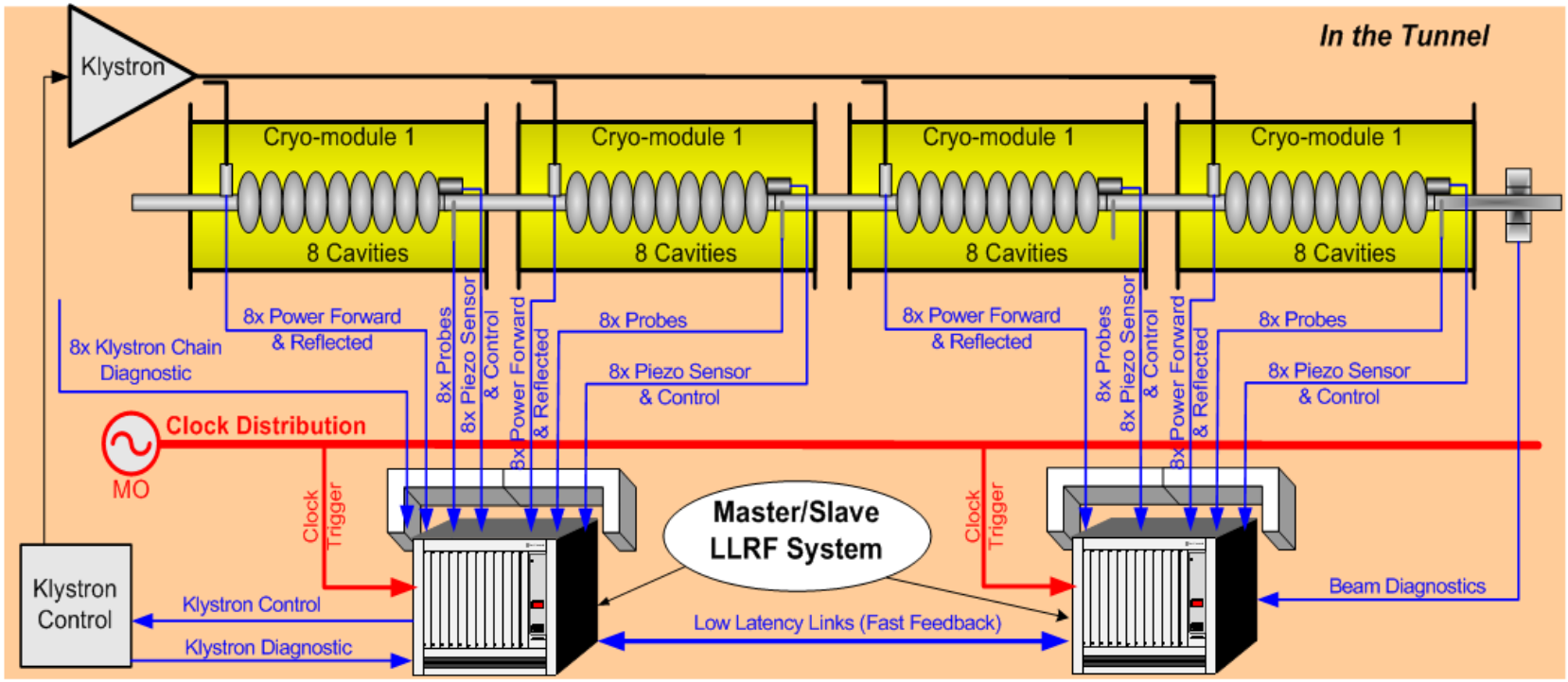
Roadmap for the XFEL LLRF

- VME -> uTCA (uAMC, uRTM) concept

- LLRF system is in the tunnel
- Distributed FPGA, DSP concept
- Process 2 times more signals
- Lowest spectral density (16-bit ADCs)
- Non IQ sampling scheme (no PM->AM)
- Redundant systems in the injector
- Rack will be fully drift compensated
- Scaleable system

LLRF for XFEL

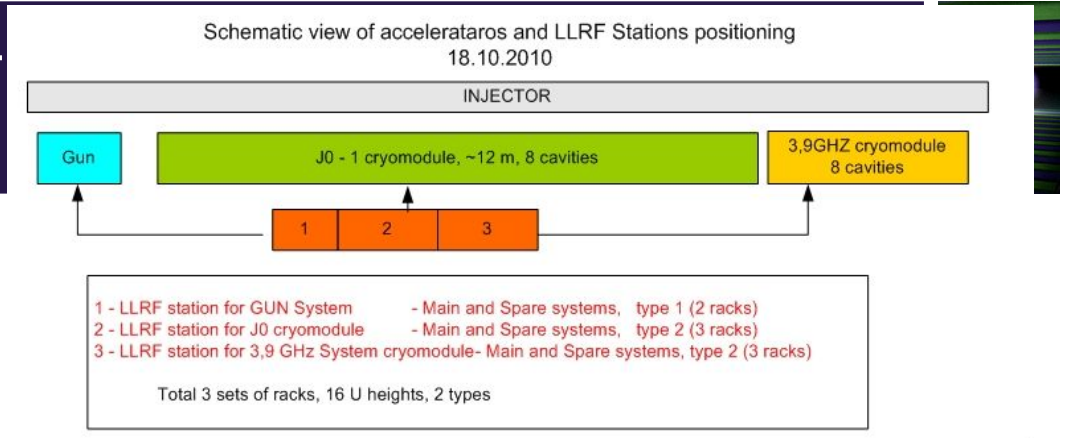
- **2 semi-distributed uTCA stations supply 4 cavity modules**



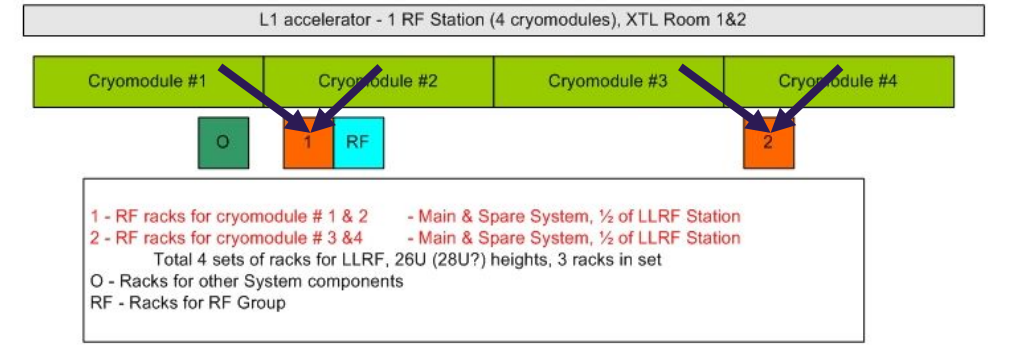
Driving Argument → Short pickup cables for low drifts (10fs/m/K) and prevent crosstalk from high power cables

LLRF system for XFEL

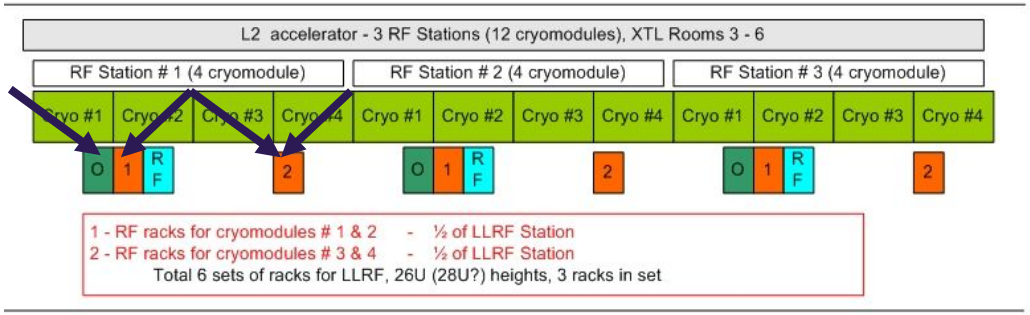
Semi-Distribution



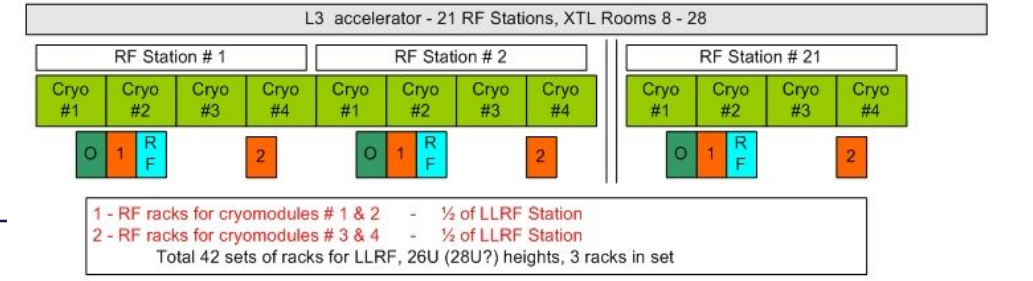
1 RF-station L1



3 RF-stations L2

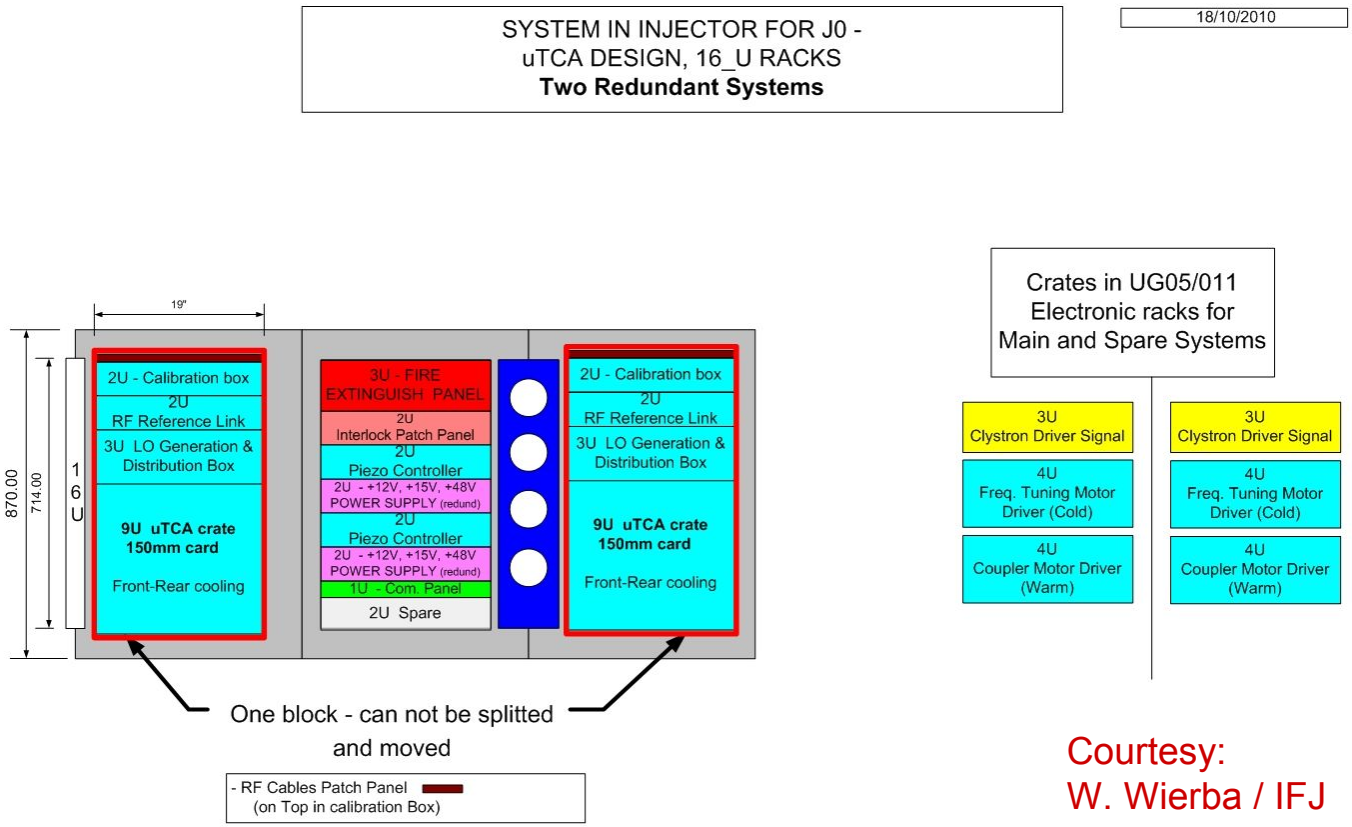


21 RF-stations L3



LLRF rack occupation

- **Injector (GUN, J0, 39) LLRF systems are completely redundant . . .**



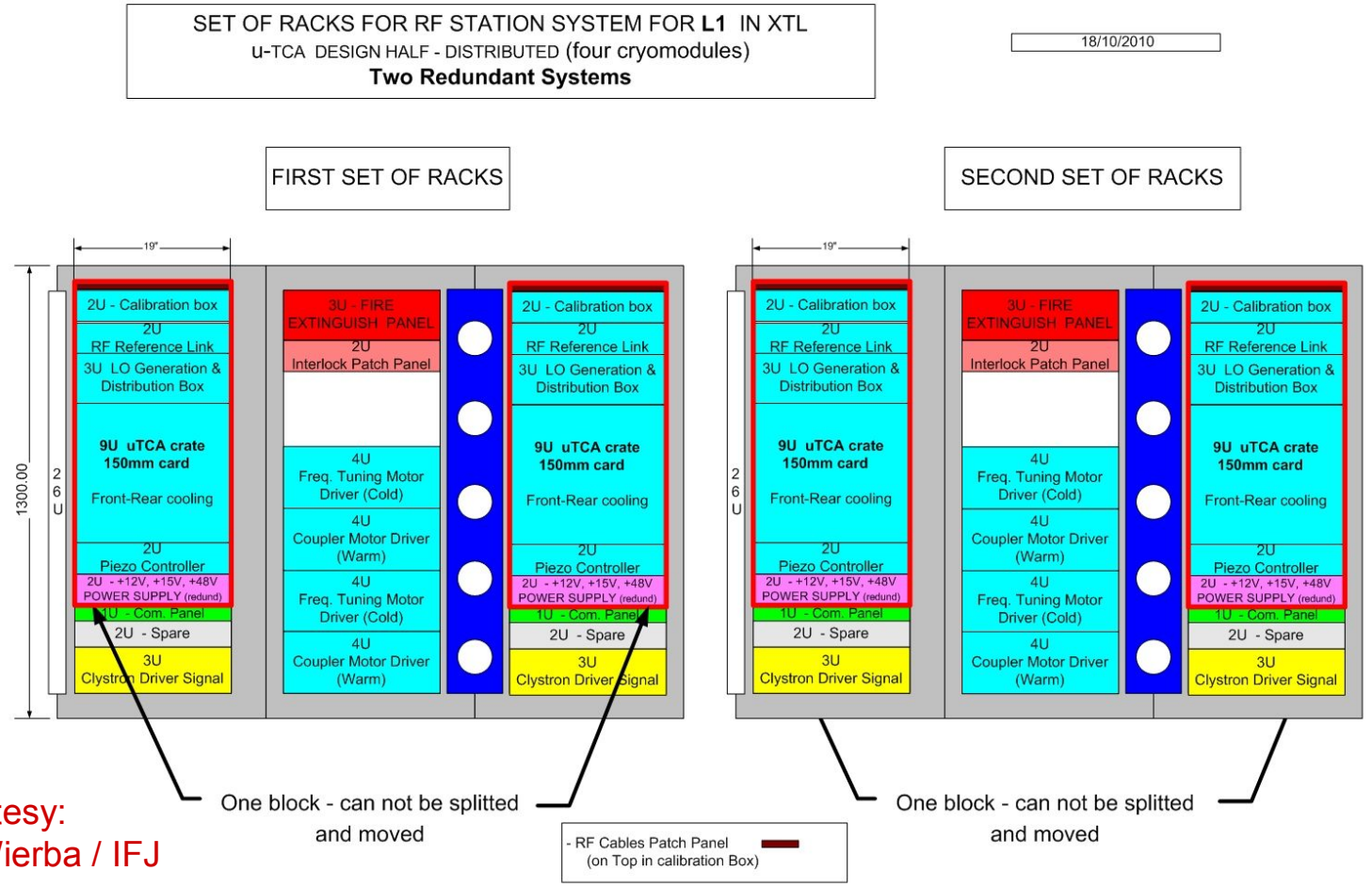
Courtesy:
W. Wierba / IFJ

→ Redundancy, LLRF performance measurement

FLASH 21/04/09, Beam Stability at FLASH - Update', F.Ludwig et. al.

LLRF rack occupation

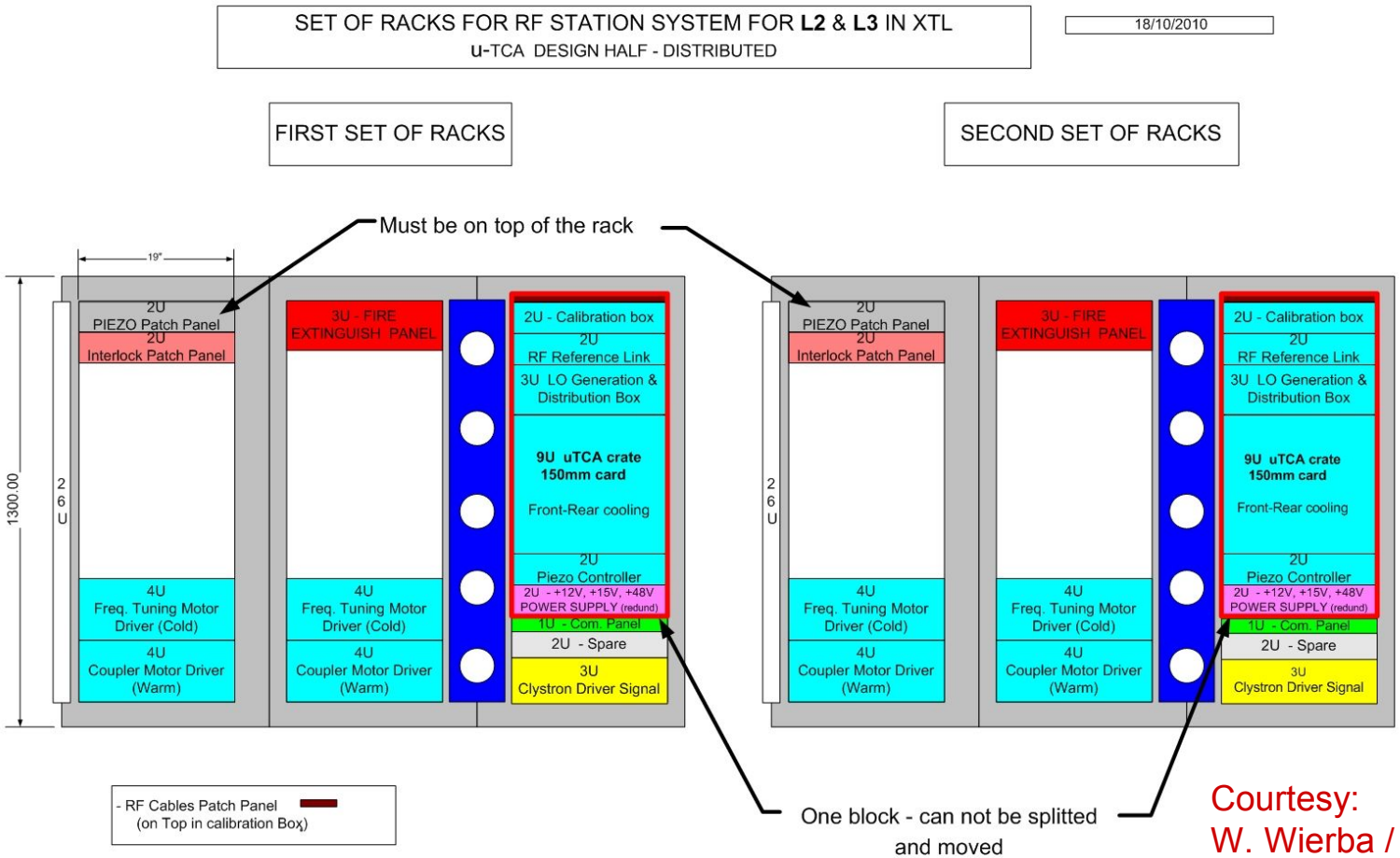
- . . . L1 is also redundant , . . .



Courtesy:
W. Wierba / IFJ

LLRF rack occupation

- . . . but L2, L3 are not redundant.

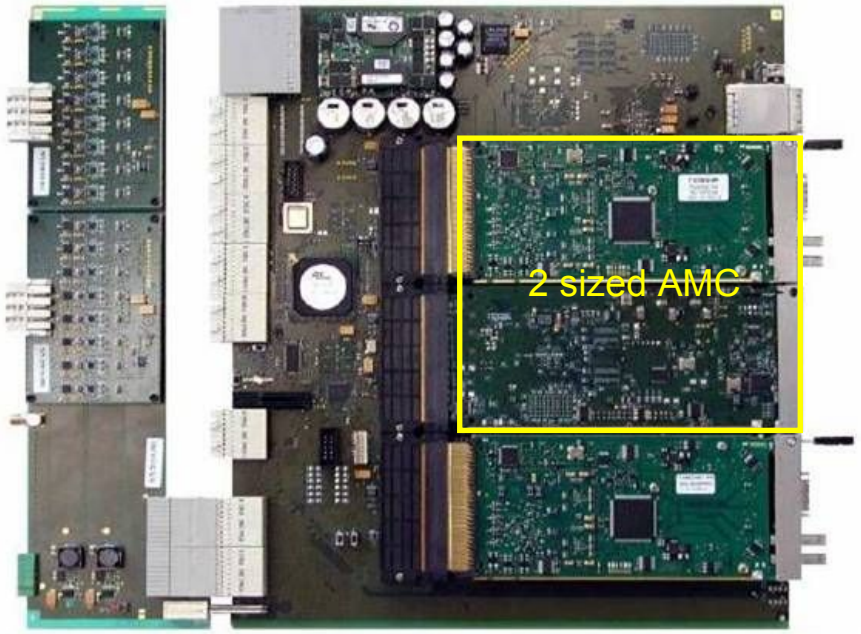


Courtesy:
W. Wierba / IFJ

Experience form ATCA system

Lessons learned from the ATCA ACC456 tests

- Moreless portable firmware between ATCA and uTCA
- Common Low Latency distributed FPGA concept
- Common IPMI handling
- Decoupling of PM to AM using the non-iq modulation scheme
- Fully modularity caused too complex system
- No sharing of 2 sized AMC modules with ATCA



. . . the xTCA crate is important, but only one part of the whole LLRF system . . .

uTCA Progress Status

- **Sharing resources within DESY and industry (status 10/2010)**

Application	AMC Type	RTM type
Timing	Timing receiver	---
Klystron	SIS8300	8 Rf receivers, 2 diff in
3.9GHz monitoring	SIS8300	9 RF receivers @ 3.9GHz
1.3GHz monitoring	SIS8300	9 RF receivers @ 1.3GHz
Coupler Interlocks	DAMC2	ADCs, tests, sources
BPM	DAMC2	---
Toroid	DAMC2	ADC
Beam Loss Monitor	DAMC2	ADCs
Wire Scanner	DAMC2	2 different signal conditioning
Beam Arrival Monitor	SIS8300	Optical in
EBPM	SIS8300	Optical in
Fs LASER sync	SIS8300	Optical in
Fs motors	DAMC2	Stepper card
Spectrometer	DAMC2	32 ch ADC
Machine Protection System	DAMC2	Signal conditioning
Kicker	DAMC1	---

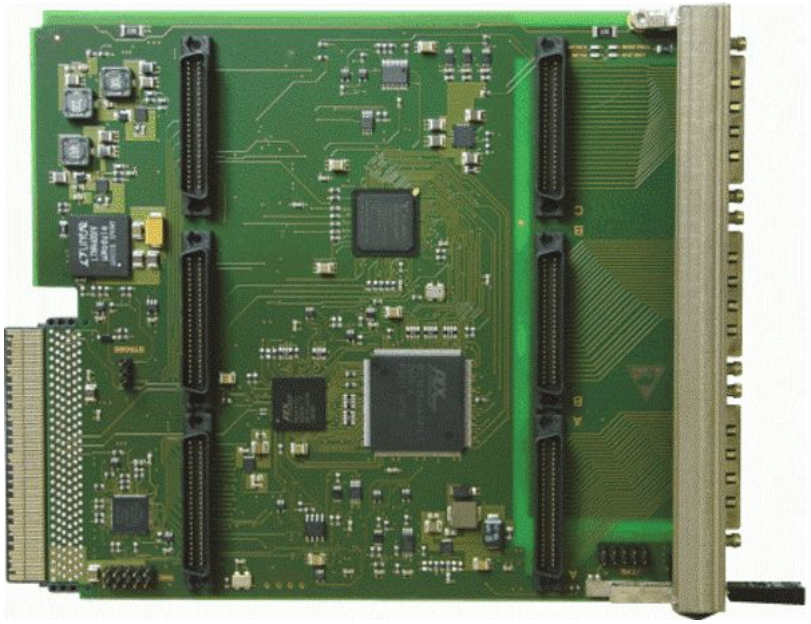
DESY partners :

MCS,
MSK,
FEB,
FLC,
FLA,
MDI,
MIN,
MHF-SL,
EXP-DAQ,
SLAC,
TDS, RAEGAE, AMTF

Industry partners:

struck innovative systeme
ELMA 50 years 1960-2010 Your Solution Partner
TEWS TECHNOLOGIES
Cryoelectra

Slow I/O



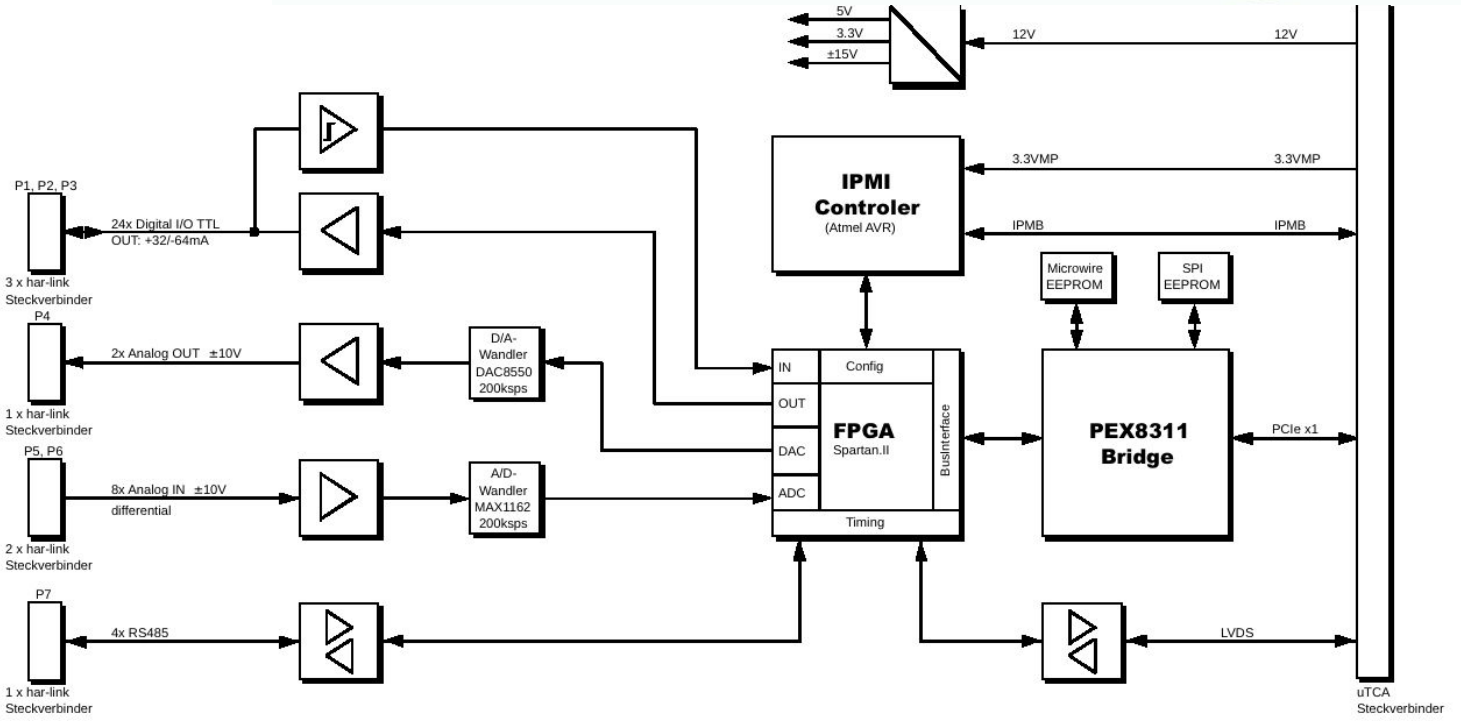
- TAMC 100
  - 1 slot IP carrier
- TAMC 200
  - 3 slot IP carrier

Available from Tews

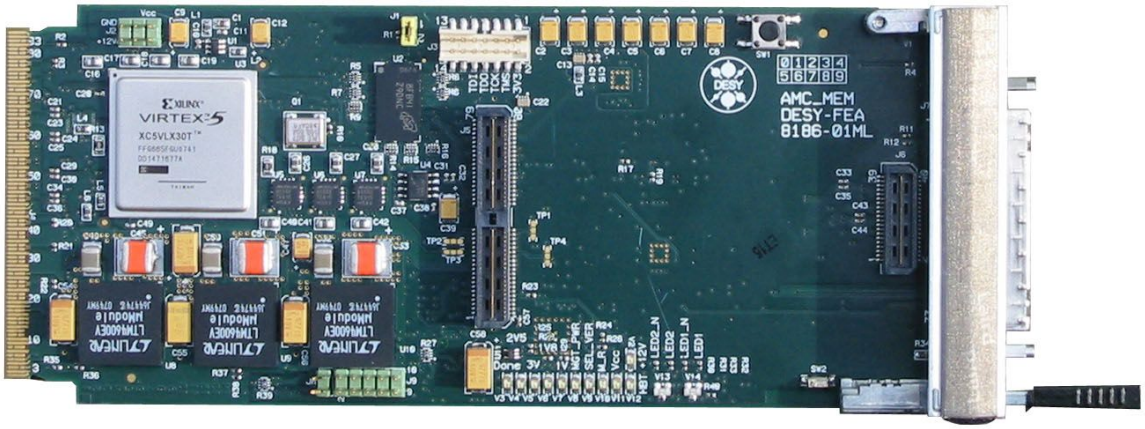
Slow I/O (2)

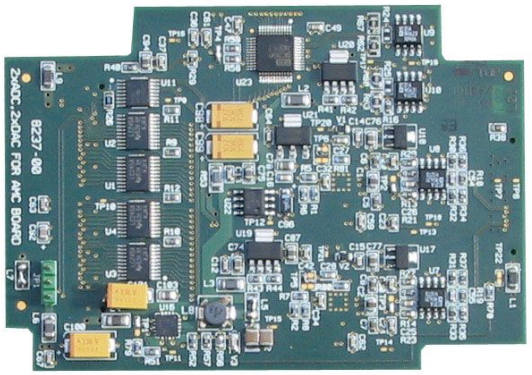
- A,D I/O
  - 8 ch ADC 200kHz
  - 2ch DAC
  - 24 I/O
  - 4 RS485
  - 1 lane PCIe

Available from ESD



Fast I/O: AMC Design





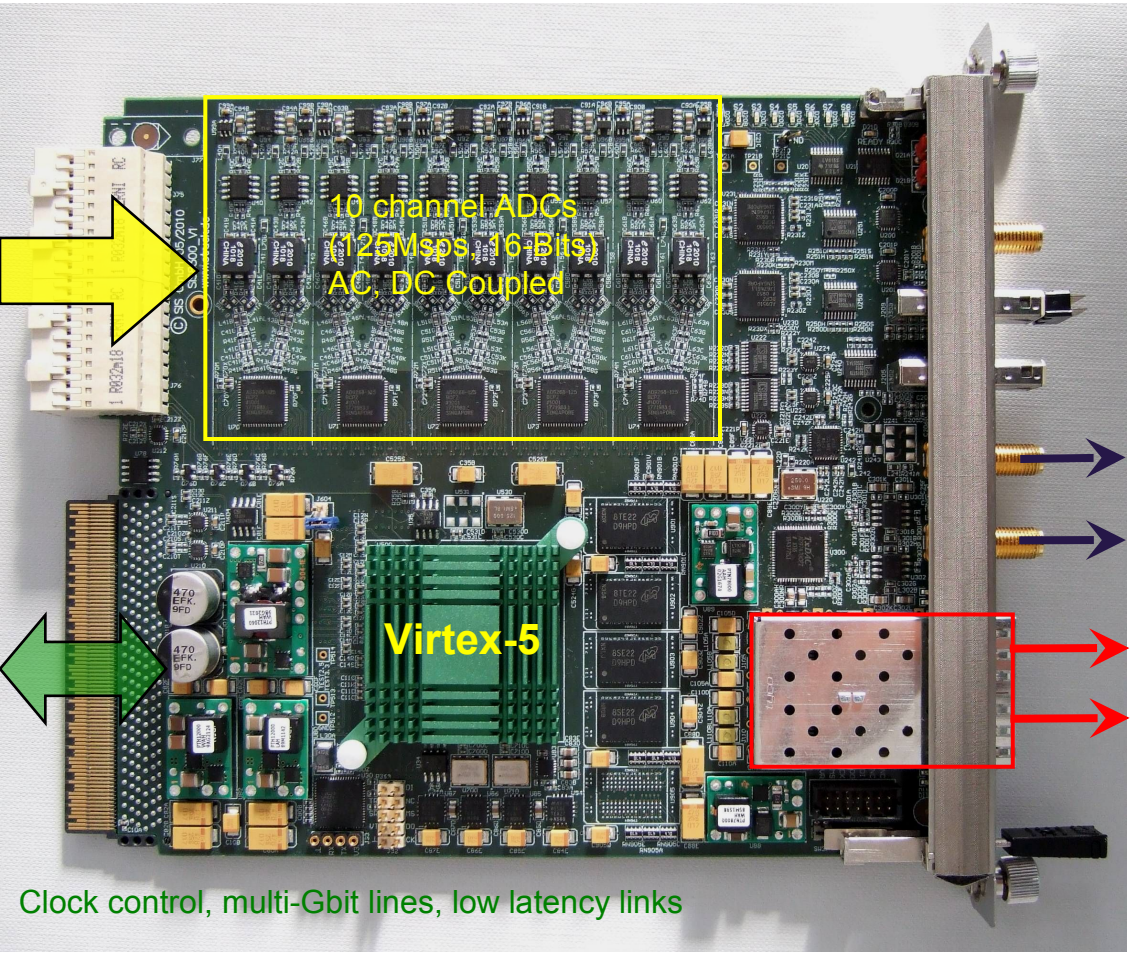
TEWS TECHNOLOGIES

- DESY AMC 1
  - Virtex5, 256MB
  - 2ch ADC, 125 MSPS, 2ch DAC
  - Tested: BPM and Toroid readout with 81 Mhz
- TAMC900 (Tews)
  - 8ch ADC, 125MSPS
  - Tested: LLRF ATCA

Fast I/O: AMC Design

- **Digitizer, Partial Vector Sum (SIS8300)** (delivered, test state)

struck innovative systeme



- 10 channel ADCs (125Msps, 16-Bits)
- FPGA partial cavity vector sum
- Low latency links via uTCA-backplane

2x DAC Outputs

SFP front I/O's
Fiber or cable

Down-converter for XFEL

- **How to package all this ?**

Distortions

Mechanical vibrations

Environment Temperatur, Humidity

Microwave Crosstalk

Packaging

- Short ½“ type pickup cables
- N-Type connectors -> PCBs
- Multi-Layer Rogers RF Boards
- Component Distribution ?
- IF separation recommended
- Active calibration methods

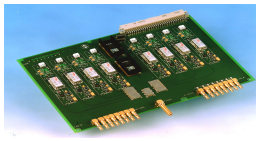
2006 DESY / Passive 8-channel:

(+) Performance 0.003% (1MHz)
(+) 16-bit ADC
(--) ADC near to Receiver
Complicated design

2007 FermiLab / Passive 8-channel:

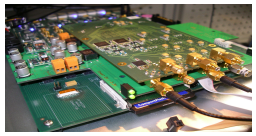
(+) Performance
(+) IF separation
(14-bit ADC limited – not this board)

2007 DESY / Active 8-channel:



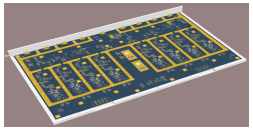
(+) Noisebalanced
(+) IF separation
(--) VME based
(--) SimconDSP 14-bit limited

2009 PSI / DESY / Passive 6-Channel:



(+) Performance
(+) IF separation
(+) 19“ mech. package
(+) 16-bit ADC

2010 DESY / PSI / Active (Passive) 8-channel:

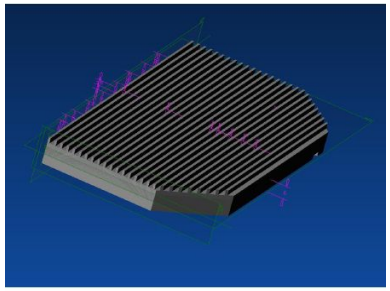


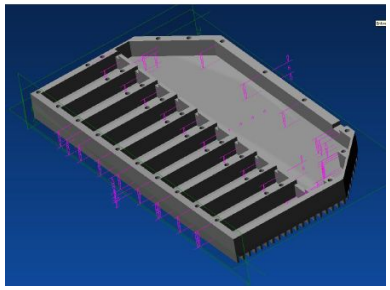
(+) Noisebalanced, ACC39
(+) IF separation
(+) 19“ mech. package
(--) SimconDSP 14-bit limited

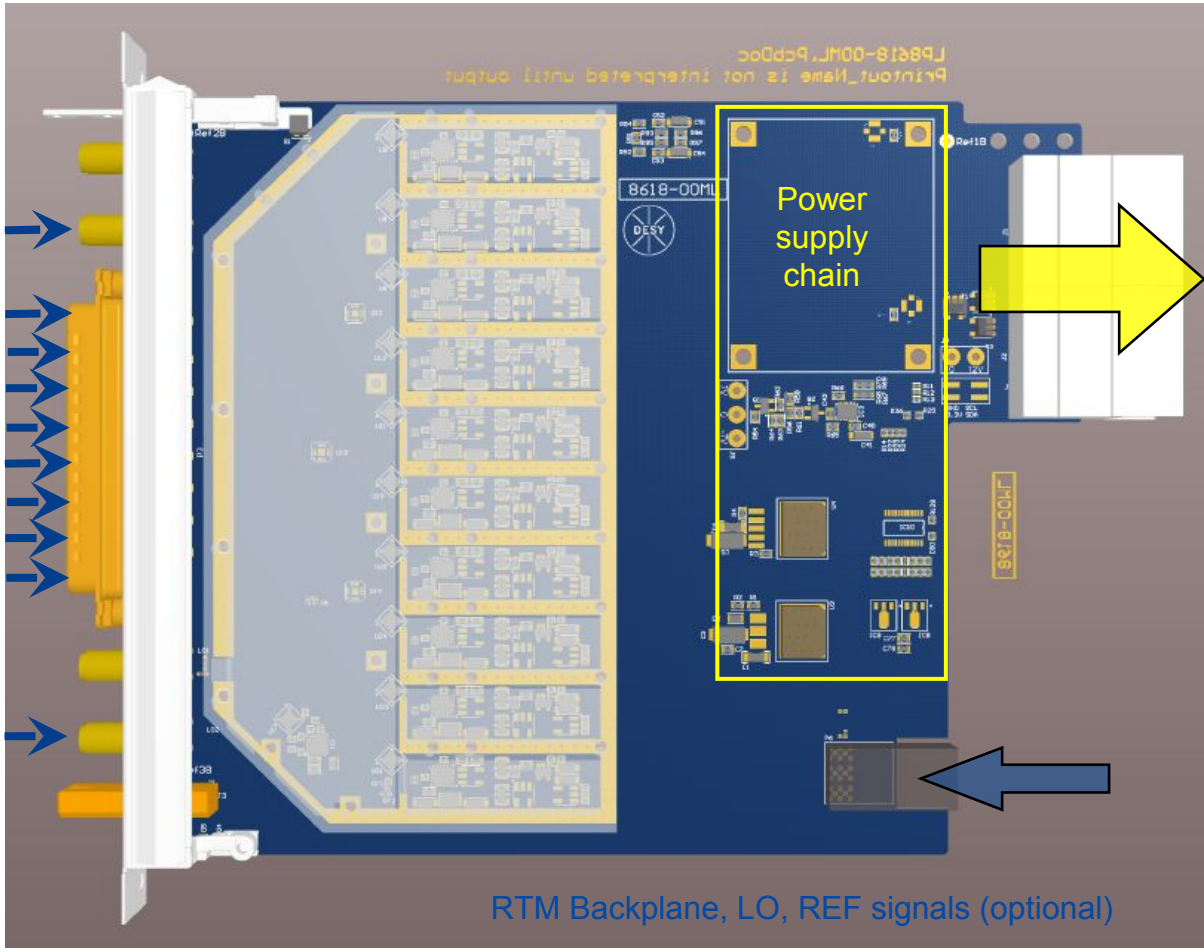
Down-converter for XFEL

Multi-channel Down-Converter (DWC8300) (delivered, test state)

- 10 channel field detection
  (1.3GHz … 3.9GHz version)
- Rear / Backplane RF access



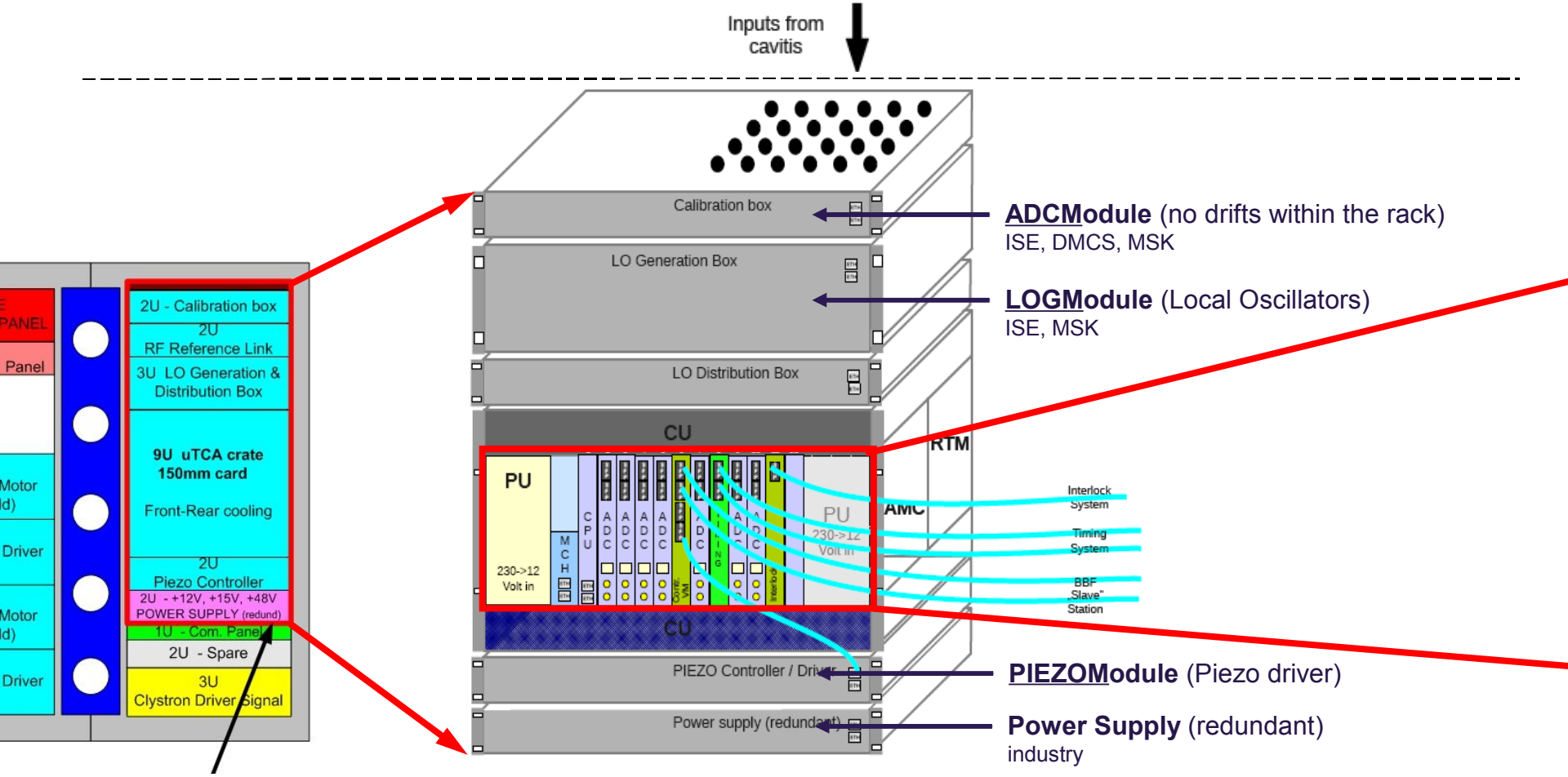




Courtesy:
J.Piekarski / ISE
M.Hoffmann, D. Kühn / DESY

crate & rack

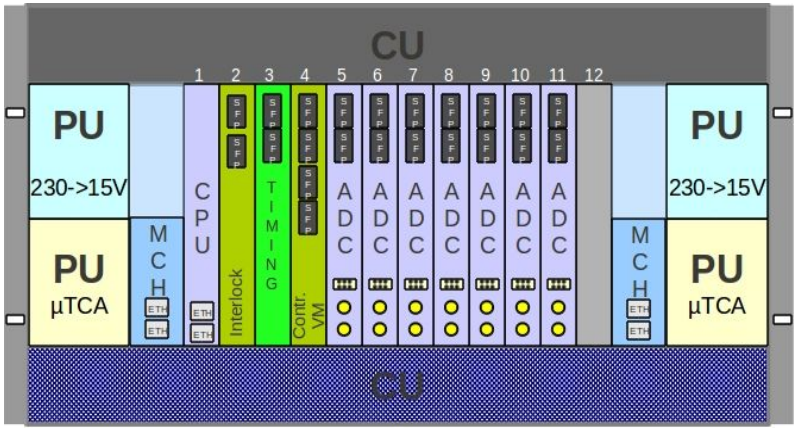
- **How will a LLRF System look like inside . . . 19“ modules . . .**



LLRF system for XFEL based on xTCA for Physics

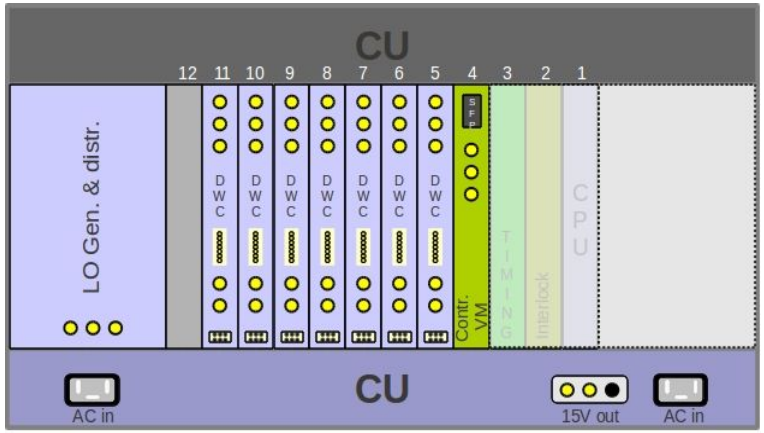
… and the crate

AMC front occupation



Slot #01: CPU	(Industry)
Slot #02: Interlock	(MCS)
Slot #03: Timing	(MCS)
Slot #04: **LLRF Controller**	**(uTLC / DMCS, MSK)**
Slot #05: ADC, Klystron Chain	(SIS8300 / Struck, MCS, MSK)
Slot #06: ADC, VS Reflected	(SIS8300 / Struck, MCS, MSK)
Slot #07: ADC, VS Reflected	(SIS8300 / Struck, MCS, MSK)
Slot #08: ADC, VS Forward	(SIS8300 / Struck, MCS, MSK)
Slot #09: ADC, VS Forward	(SIS8300 / Struck, MCS, MSK)
Slot #10: ADC, VS Probe	(SIS8300 / Struck, MCS, MSK)
Slot #11: ADC, VS Probe	(SIS8300 / Struck, MCS, MSK)
Slot #12: free	

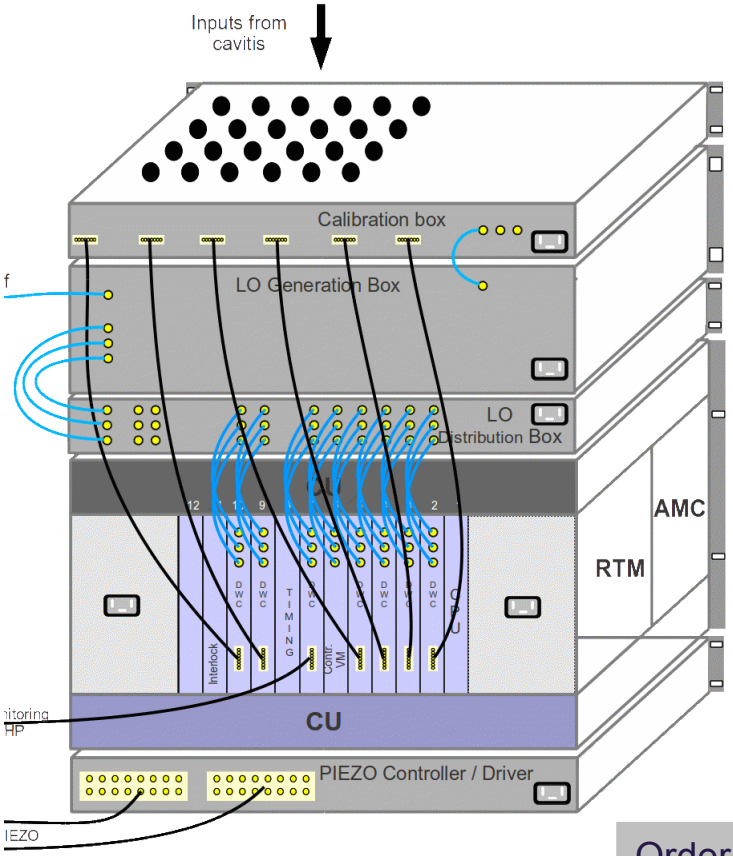
RTM rear occupation



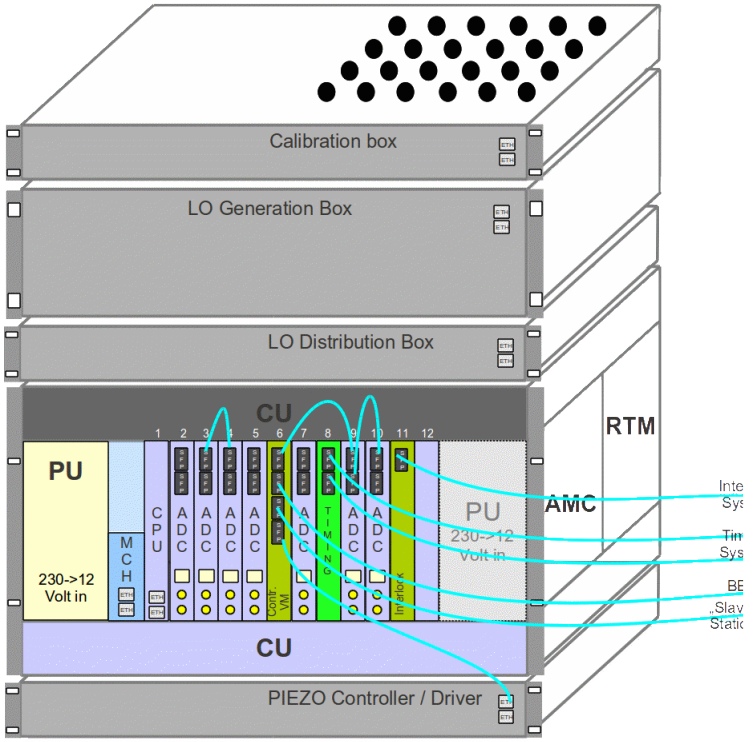
Slot #01: -	
Slot #02: -	
Slot #03: -	
Slot #04: **Klystron Driver**	**(uTLC VM / DMCS, ISE)**
Slot #05: **DWC, Klystron Chain**	**(DWC8300 / ISE, MSK)**
Slot #06: DWC, Reflected	(DWC8300 / ISE, MSK)
Slot #07: DWC, Reflected	(DWC8300 / ISE, MSK)
Slot #08: DWC, Forward	(DWC8300 / ISE, MSK)
Slot #09: DWC, Forward	(DWC8300 / ISE, MSK)
Slot #10: DWC, Probe	(DWC8300 / ISE, MSK)
Slot #11: DWC, Probe	(DWC8300 / ISE, MSK)
Slot #12: free	
Slot #15: **LO-Generation**	**(uLOG / ISE, MSK)**

uTCA Progress Status

- **LLRF system (Prototype test desired at FLASH 01/2011)**



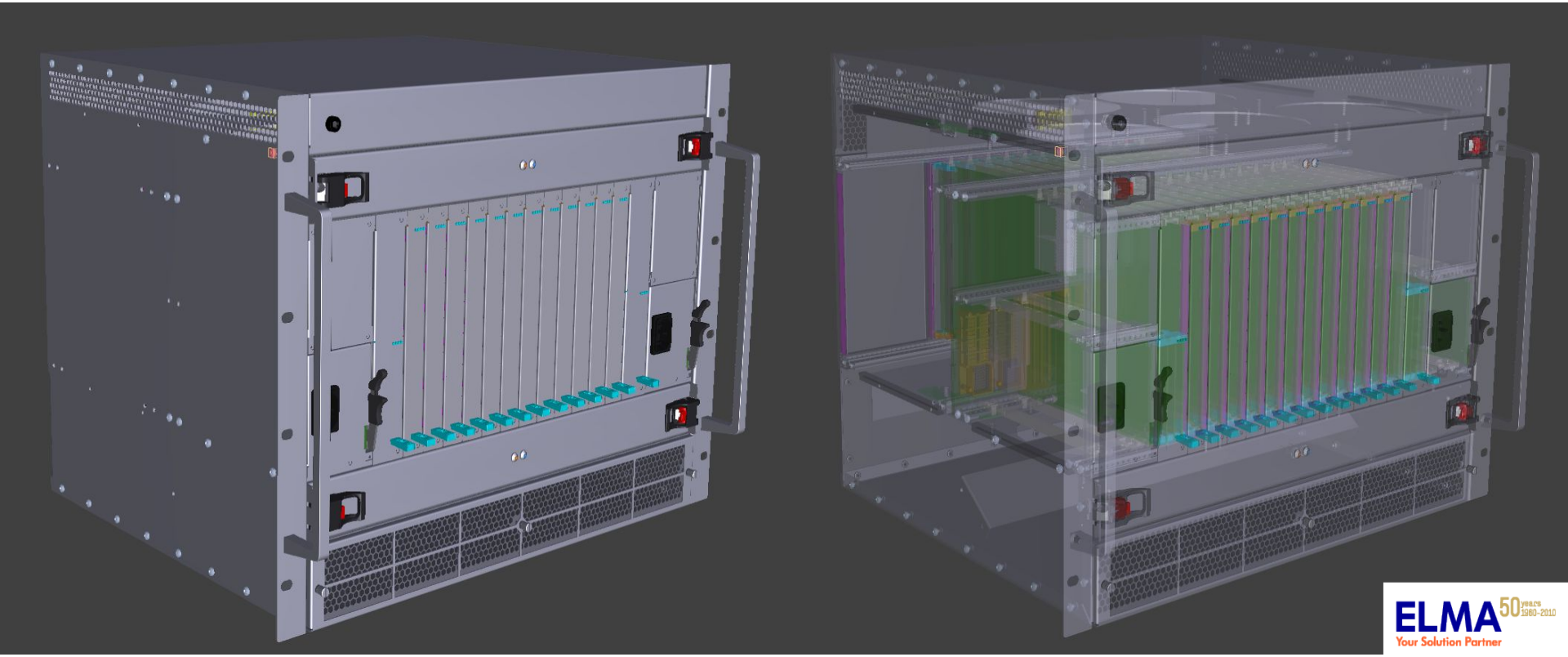
1. CPU
2. ADC – Pref
3. ADC – Pref.
4. ADC – Prob
5. ADC – Prob
6. Contrl.+VM
7. ADC – Monitoring
8. Timing
9. ADC – Pfor.
10. ADC – Pfor.
11. Interlock



Order of boards for low distortions concept → - LLRF AMC backplane

Complicated cable management concept → - LLRF RTM backplane

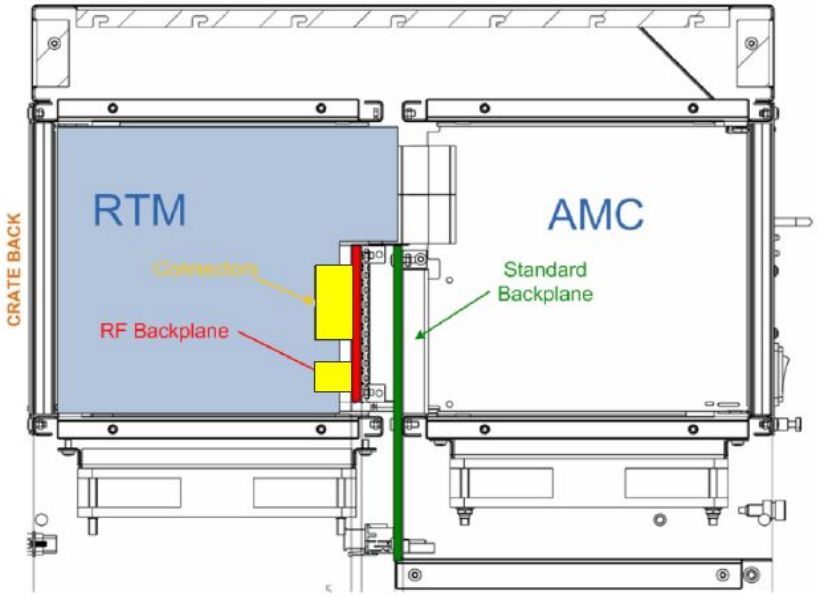
Looking for free space in the crate

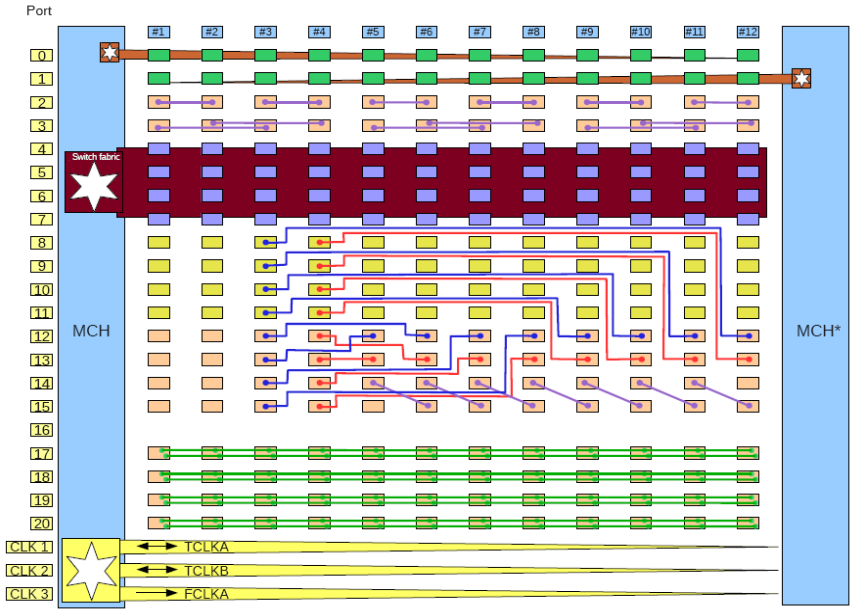


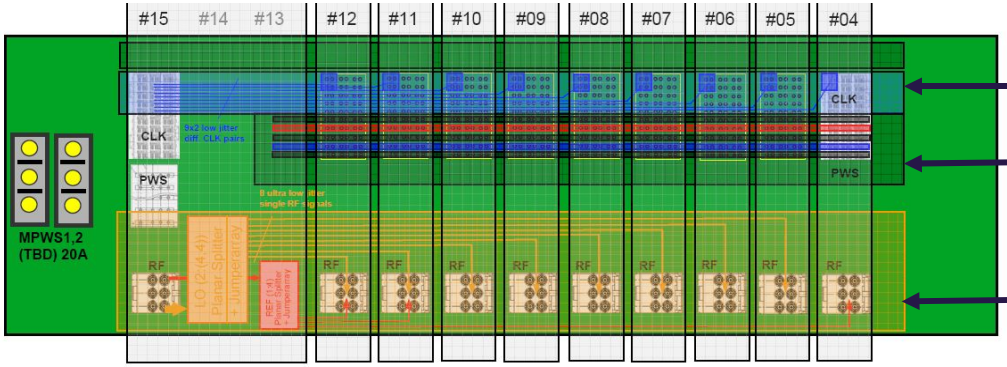
Courtesy: ELMA

Backplanes ...

- **uRTM, uAMC and LLRF backplanes**





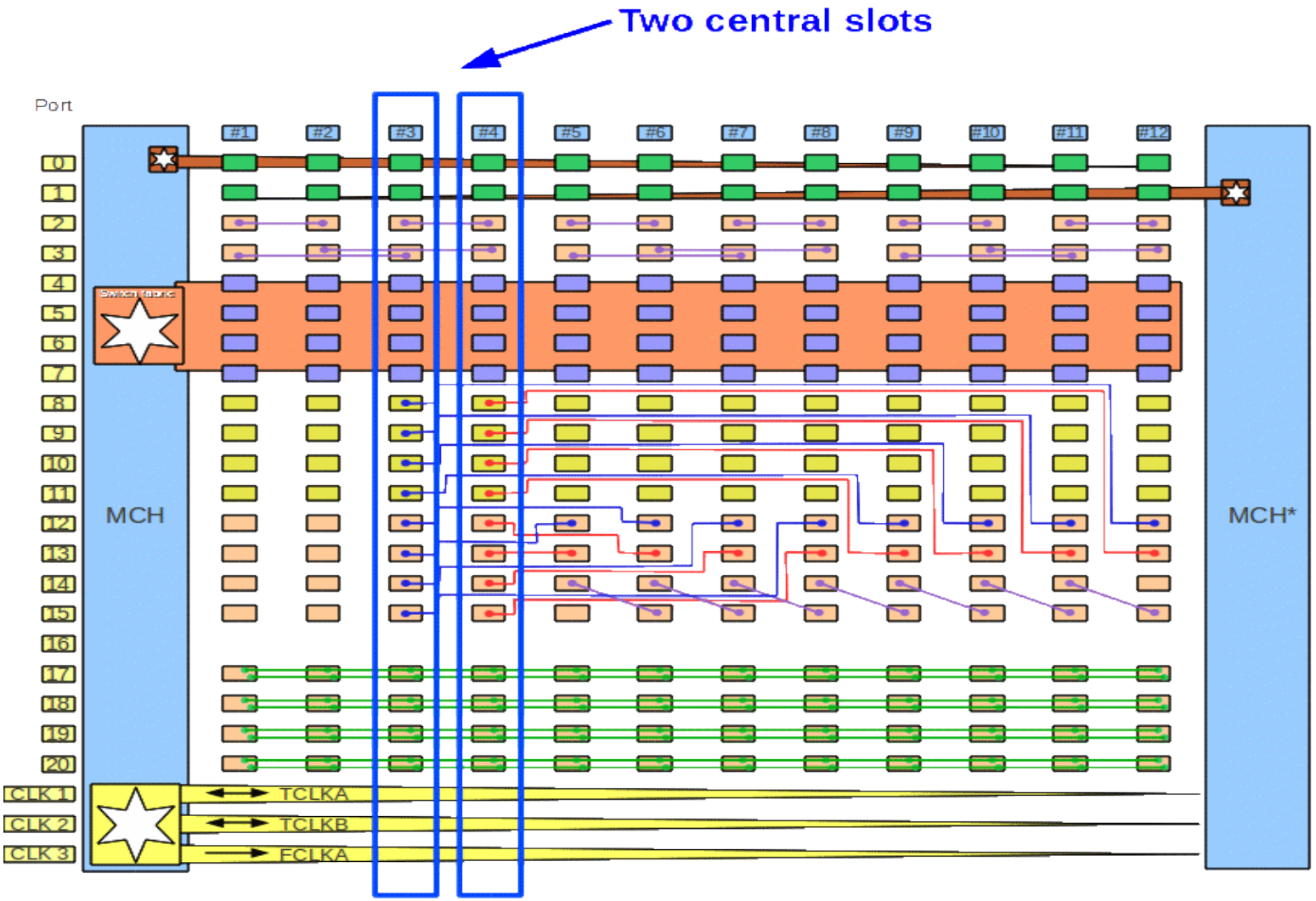


Low jitter clock distribution < 200fs
(e.g. ADC-Clocks)

Independent redundant power supplies
(e.g. +15V, -15V)

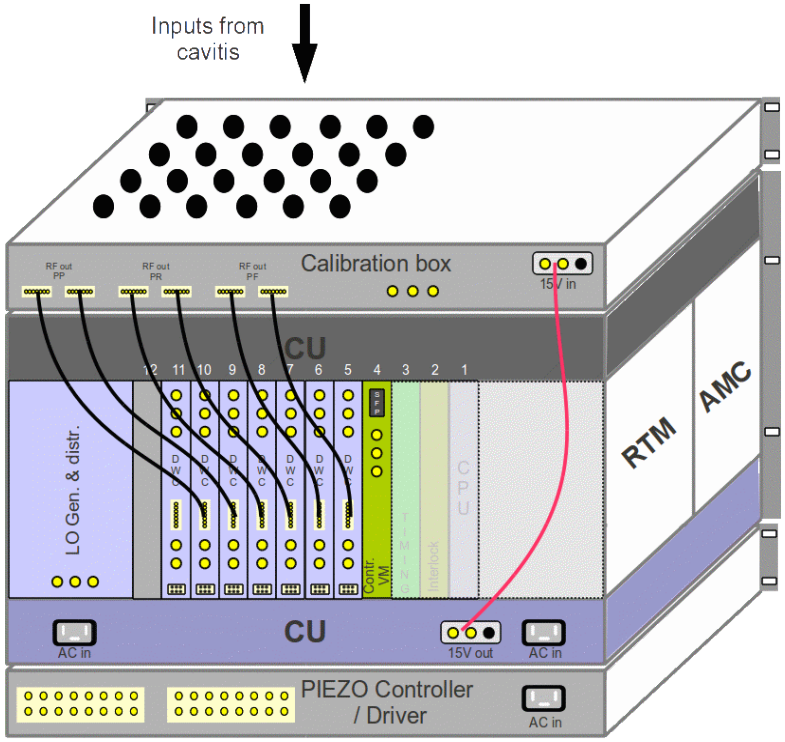
Low jitter RF-signals <10fs
(e.g. LO-Distribution)

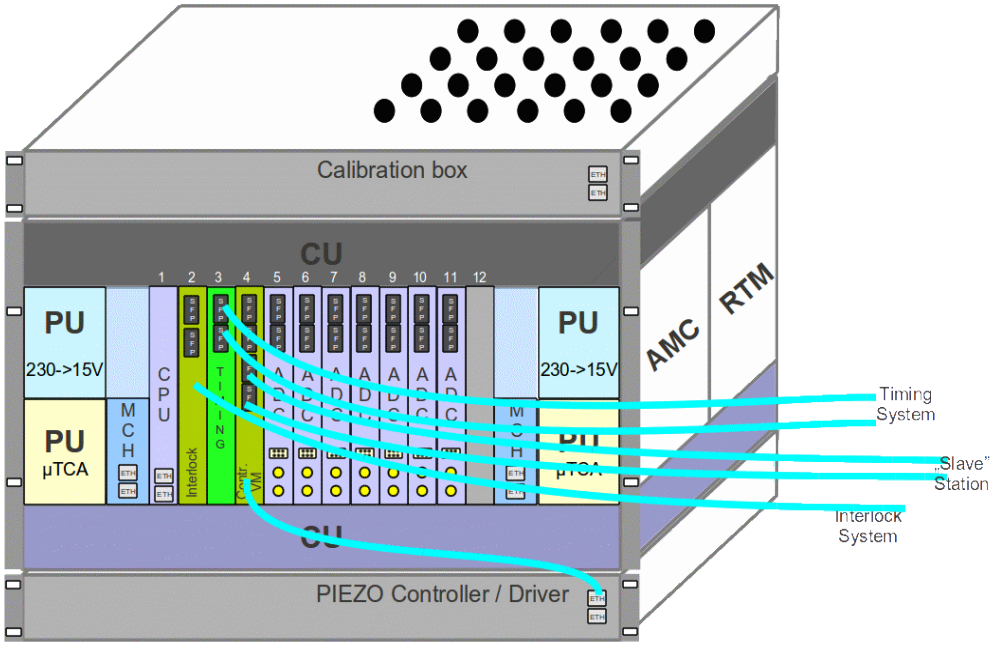
Low Latency Links



LLRF System - prototype

- **LLRF system (Prototype XFEL desired at FLASH 06/2011)**





. . . to be tested . . .

Injector Stations – RF separation

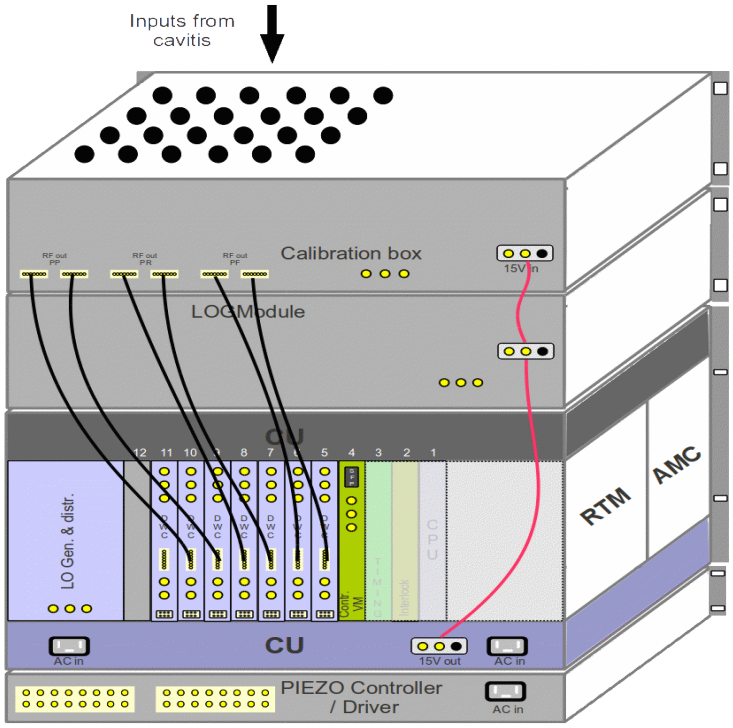
- Performance has to be characterized
- Channel parallelization upgrade possible

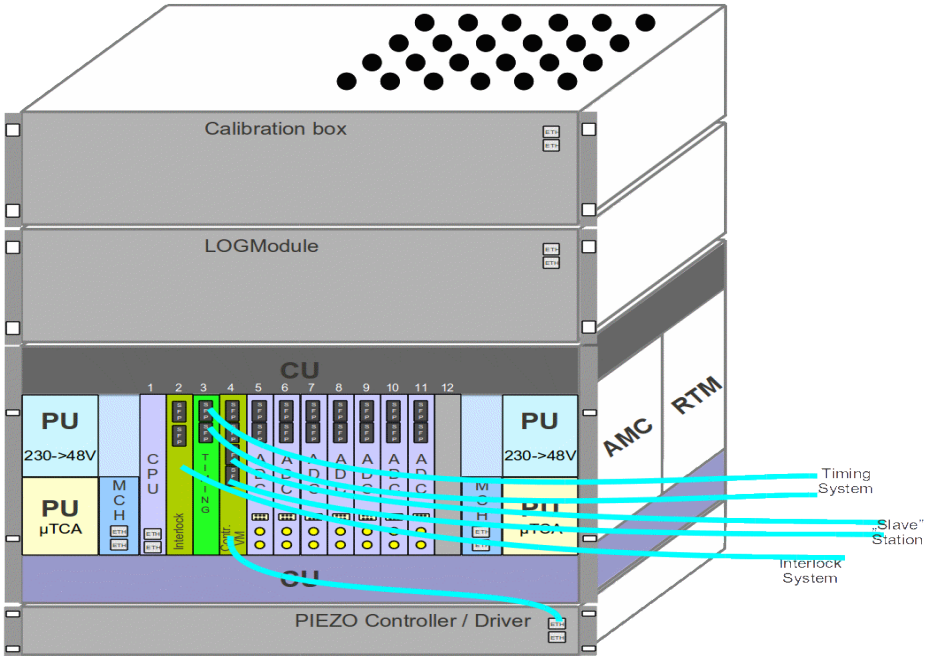
Main Stations – IF separation

- Very robust machine operation
- Low cost version

LLRF system for XFEL based on xTCA for Physics

LLRF System - prototype

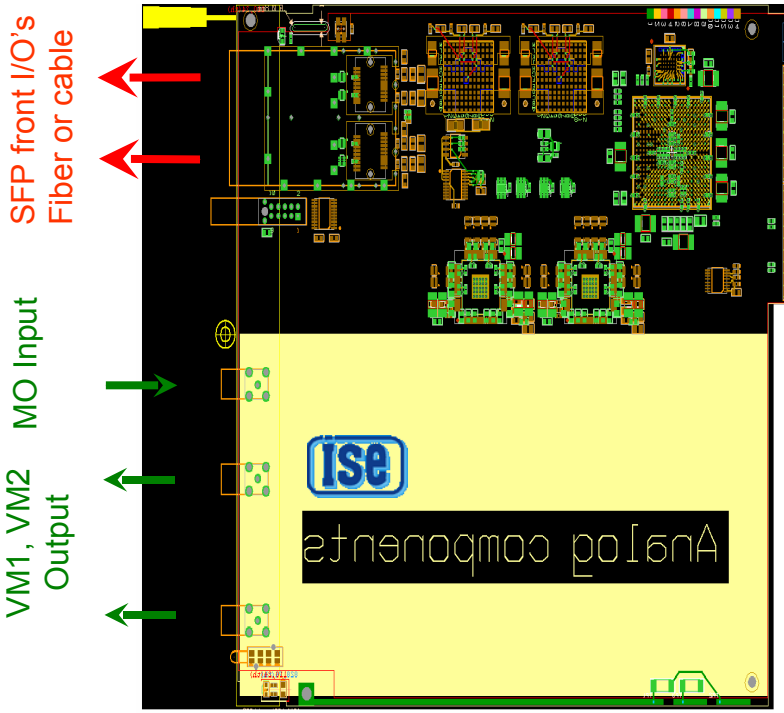




Contoller and vector-modulator

Klystron Driver (uTLC VM)

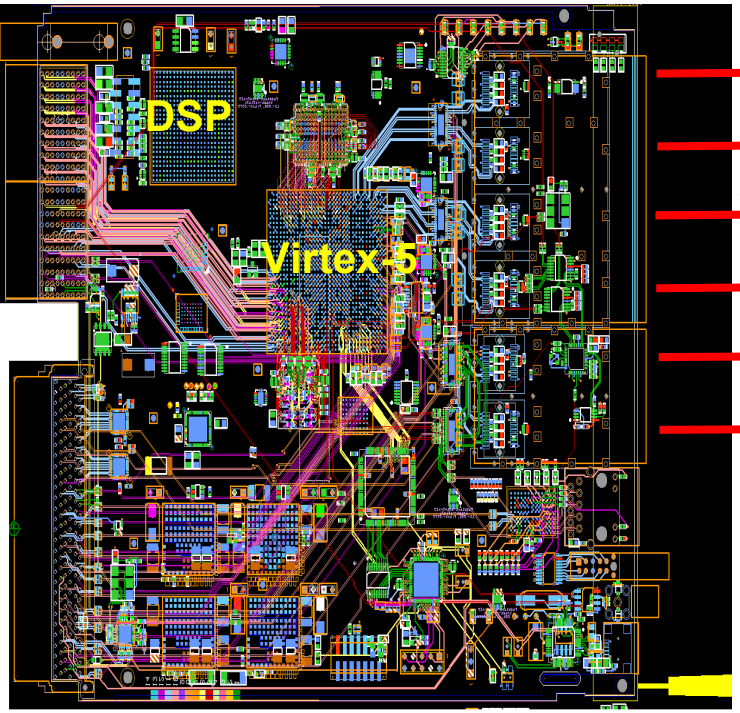
(Schematic state)



- 2 channel vector modulator (108MHz, 216MHz, 1.3GHz…3.9GHz)
- 16-bit DAC

LLRF Controller (uTLC)

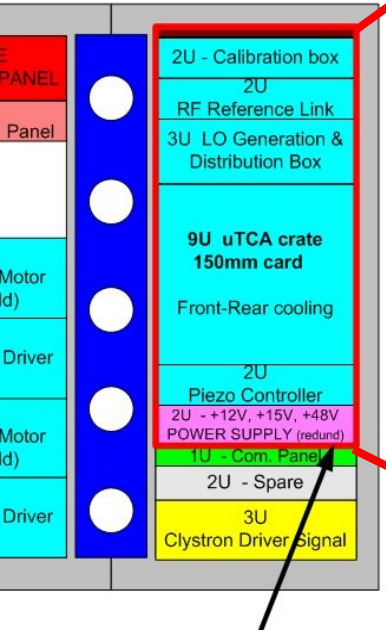
(Routing state, 95%)



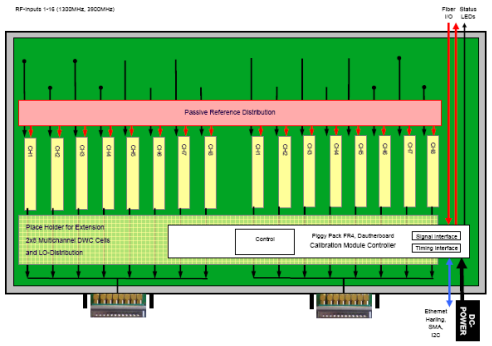
- LLRF Controller, 6 Fiber Ports, 2 GB-Links
- FPGA, DSP

Courtesy: D. Makowski / DMCS

Summary



- **Summary of LLRF module and uTCA progress status:**
  - ADCM (Advanced Drift Calibration Module): Design state
  - REFM (Reference Module): Design state
  - LOGM (LO-Generartion Module): Design state
  - uTCA – Rack (LLRF boards): Delivered, test state
    - DWC8300 (Down-Converter): Delivered, test state
    - SIS8300 (ADC Digitizer): Delivered, test state
    - uTLC (LLRF Controller): Routing state (95%)
    - uTLC VM (LLRf Controller): Schematic state
    - uRFB (RTM backplane): Schematic state
  - PIEZOM (Piezo driver): Assembly state
  - Power Supply: Specification / Ordering state



Summary of the XFEL LLRF Roadmap

Installation and infrastructure decisions

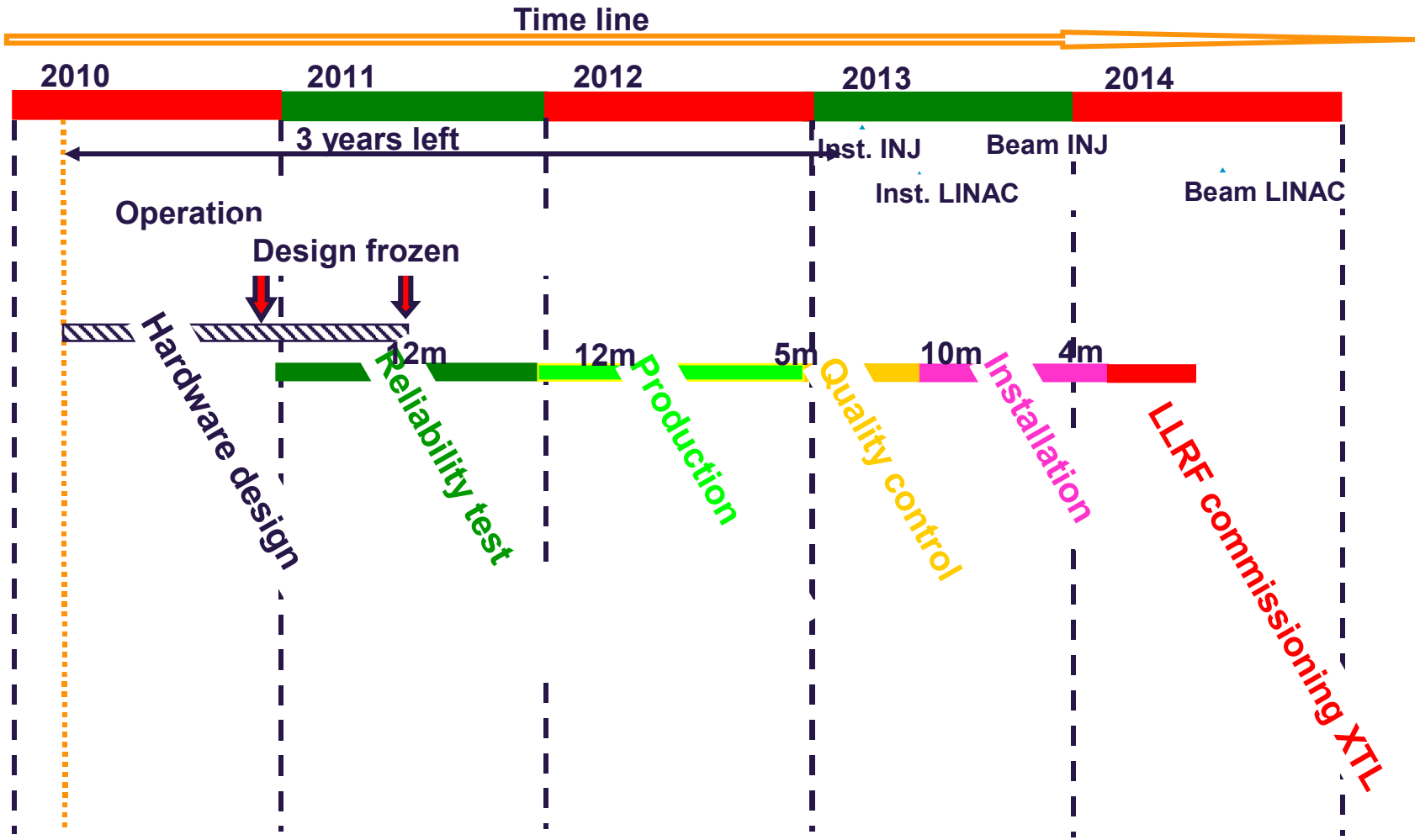
- 2 uTCA stations, 1 klystron supply 4 cavity modules for the whole XFEL
- Injector systems are doubled for redundancy and crosschecks

LLRF rack decisions

- VME -> uTCA common shared crate standart
  - Support 12 slot standart double sized uAMC and uRTM boards
  - Low latency LLRF AMC backplane, distributed FPGA & DSP support
  - 10 channel, 16-bit ADC 130Msps support (SIS8300)
  - Customer backplane for 10fs RF-signals and 100fs low jitter clocks
  - Separate redundant power supplies for analog & digital boards
  - Ready for channel parallelization for future demands
  - Separation of algorithmic and hardware firmware for easy software support
- Multi-channel field detection
  - Non IQ sampling method for easy servicing
  - 1.3GHz, 3.0GHz and 3.9GHz operation for all customers
  - 16x3 channels for Probe, Forward, Reflected signals
  - Multi-pluggable coax cables for RF-signals or IFs for easy maintenance
- Reference injection for a long-term stable machine operation
  - Fixed N-type 1/2” Heliax cables for Probe signals
  - Fixed N-type 3/8” Heliax cables for Forward, Refleced signals

LLRF system for XFEL based on xTCA for Physics

Timeline



Courtesy: H. Schlarb / DESY

Thank you for your attention