Development of the analog section and the digitizer for the new Front-End of the Surface Detector Electronics Upgrade

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The test setup consists from

1. Development kit with Cyclone® V (5CEFA7F31I7) (Altera - DK-DEV-5CEA7N)
2. HSMC – ADC – BRIDGE (Texas Instr.)
3. Evaluation Module with ADS4249 (Texas Instr. – ADS4249EVM) – 2-channel ADC with 250MSps/14-bits

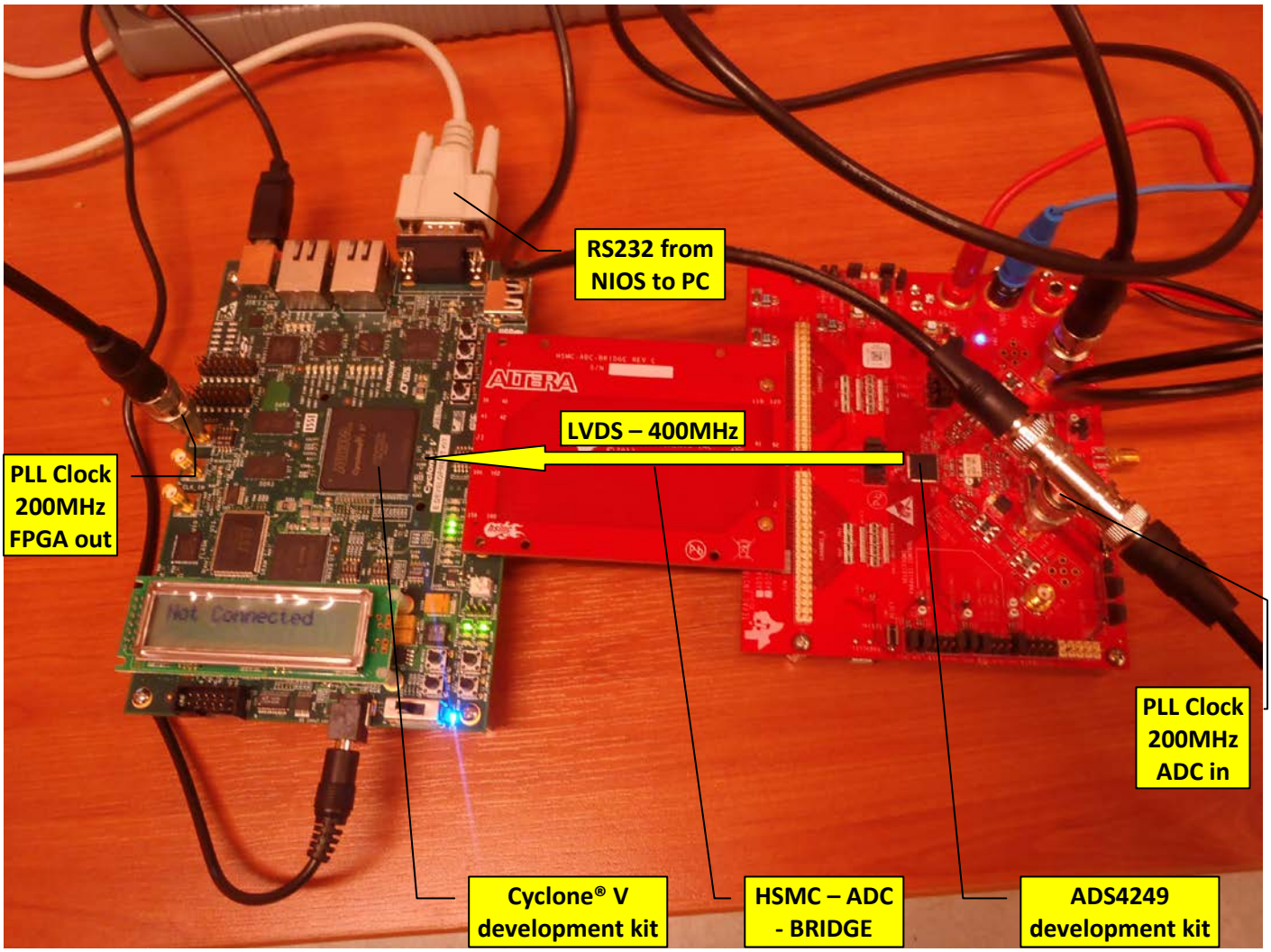


Fig. 1 – Test setup with Cyclone® V and ADS4249

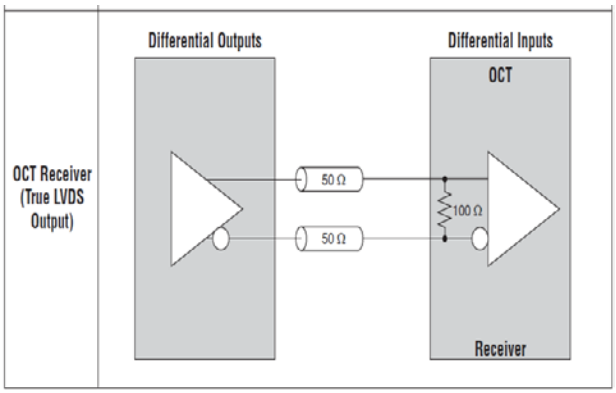


Fig. 2 - On System Termination (OCT) in Cyclone V

Cyclone V has been configured by the Quartus II software to terminate the LVDS lines inside the LVDS receivers on the FPGA. External termination resistors (100 Ohm) were not needed.

Programmable termination fully passed the exam. A distance between the ADC and the FPGA is ca. 20 cm and data is transmitted via the LVDS lines at 400 MHz without errors.

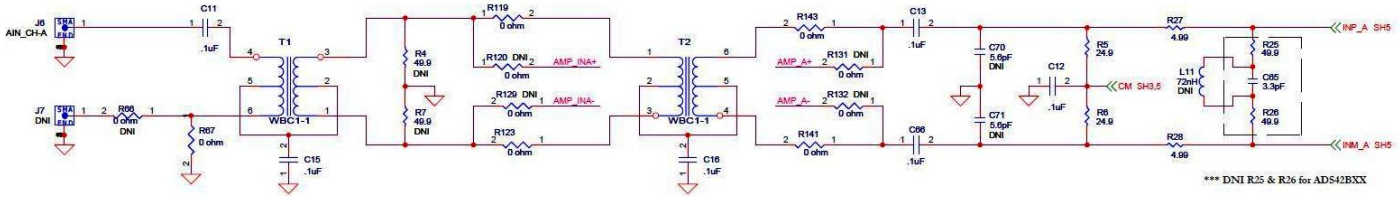


Fig. 3 – The analog section with transformers on the ADS4249EVM

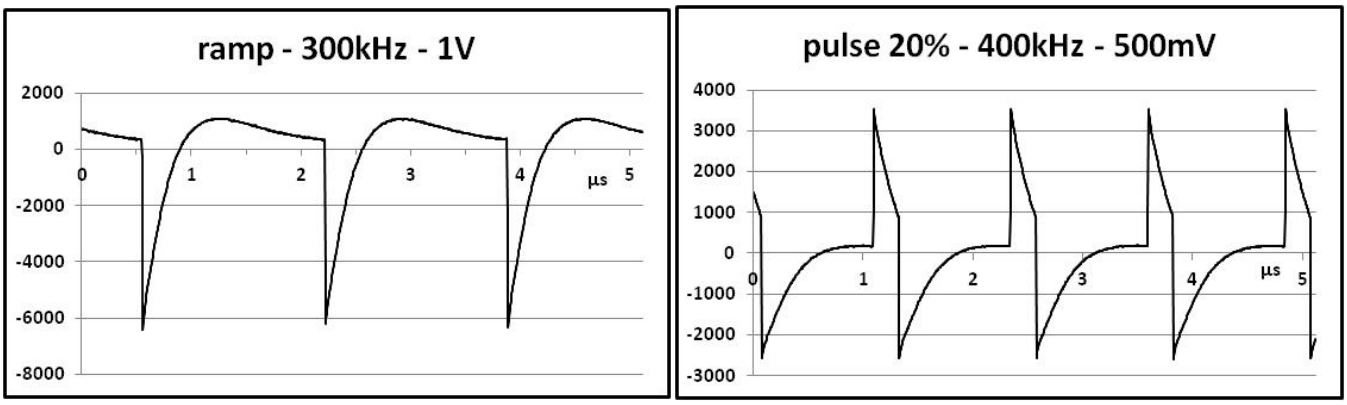


Fig. 4 - Due to differentiation on the transformed the above circuit has been disqualified for pulse sources like PMTs.

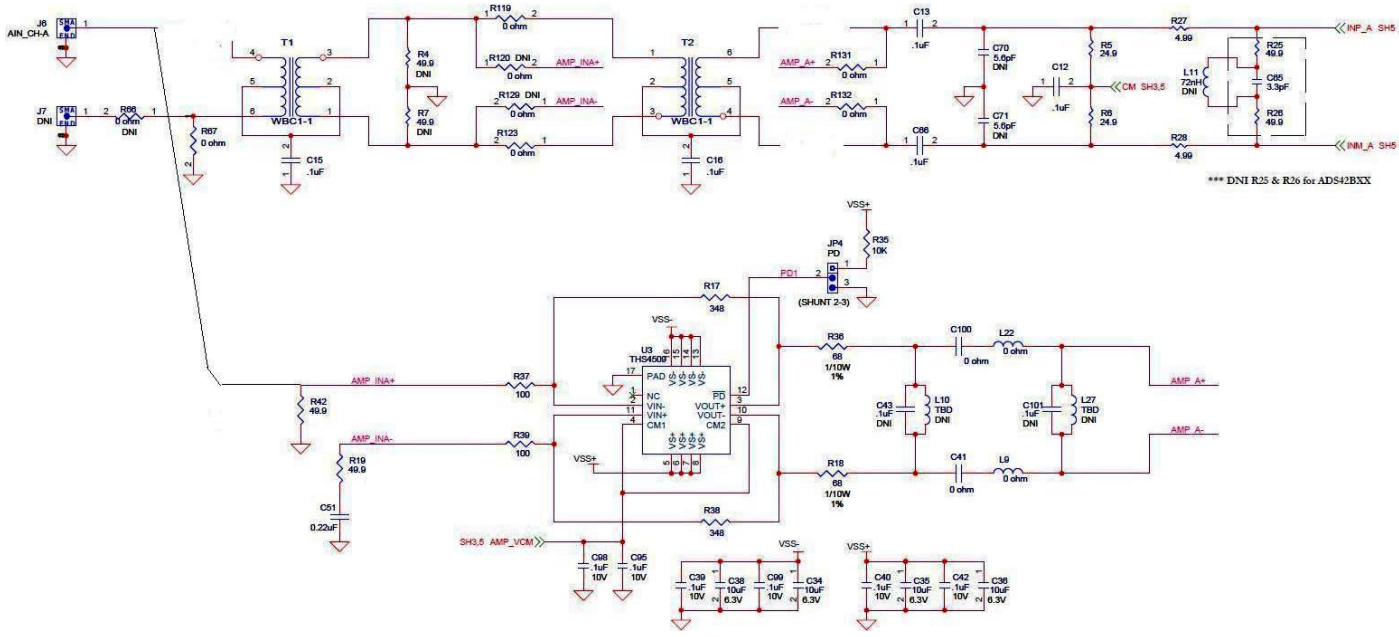


Fig. 5 – Differential driver THS4509 used instead of the transformer. R19 and R42 used according to TI recommendation.

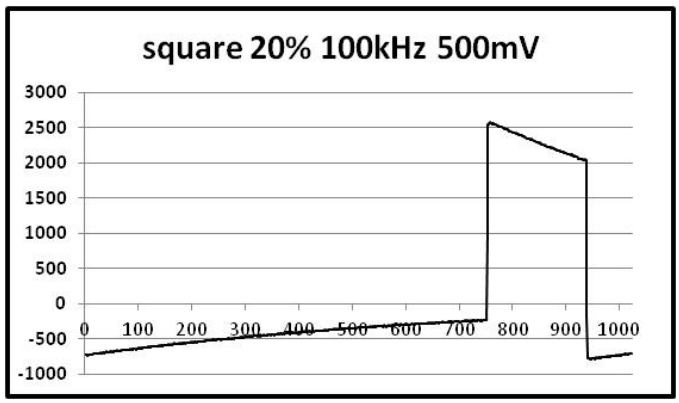


Fig. 6 – Still a differentiation on the C16/C66 and R5/R6 AC connection. This RC circuit has been removed.

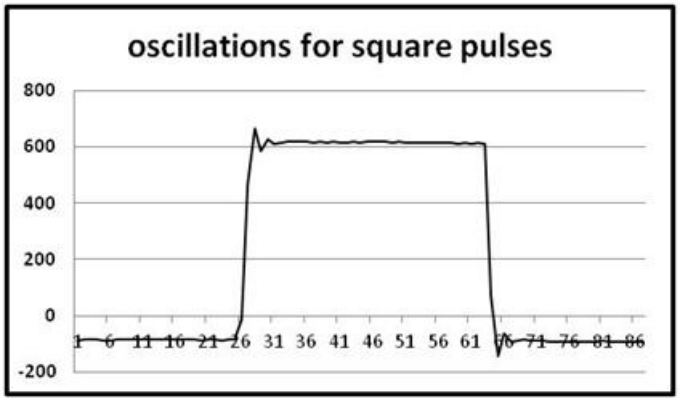


Fig. 7 – Oscillation due to not correctly termination and an adjustment of the input impedance (49.9 Ohm used according to the documentation).

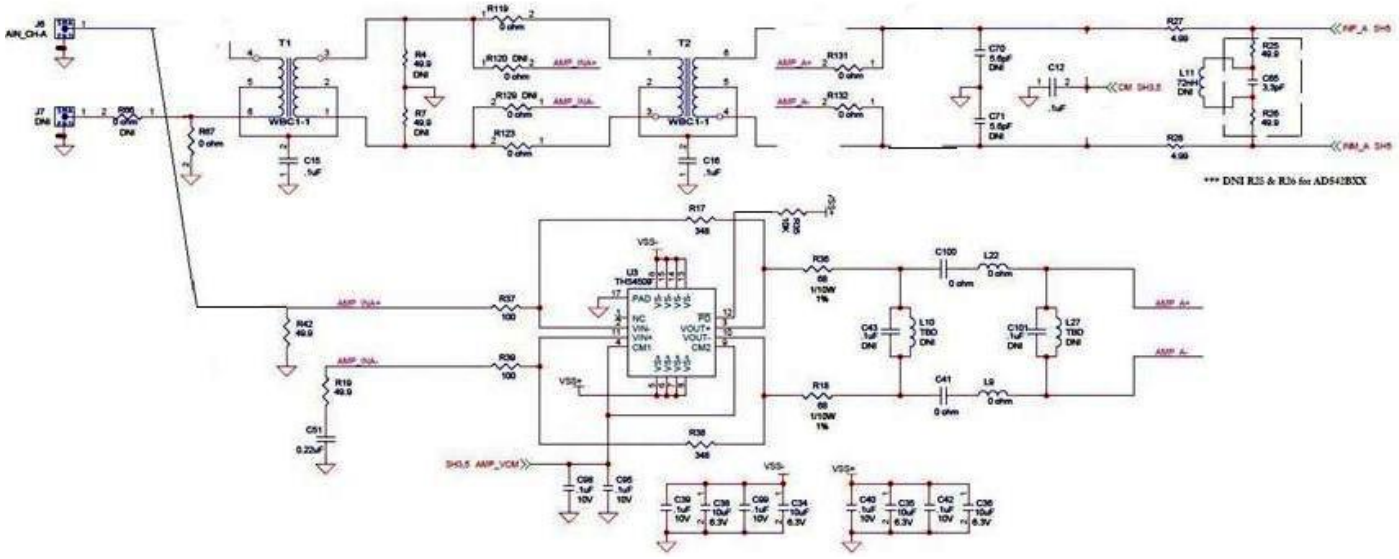


Fig. 8 – The setup without differentiation components

ELECTRICAL CHARACTERISTICS: $V_{S+} – V_{S–} = 3$ V

Test conditions at V_{S+} = +1.5 V, $V_{S–}$ = –1.5 V, G = 10 dB, CM = open, V_O = 1 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

ELECTRICAL CHARACTERISTICS: $V_{S+} – V_{S–} = 5$ V (continued)

Test conditions are at V_{S+} = +2.5 V, $V_{S–}$ = –2.5 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

According to Texas Instr. specification the THS4509 can be supplied from $+V_{s+}$ - V_{s-} = 3 – 5 V. However, for a single voltage supply (+3.3V only) huge differential nonlinearity is observed. For a symmetric supply +/- 2.5V, we observe saturation on ca. +/- 1500 ADC-units (full range = +/- 8192 ADC-units : 14-bits ADC) and very suspicious spikes.

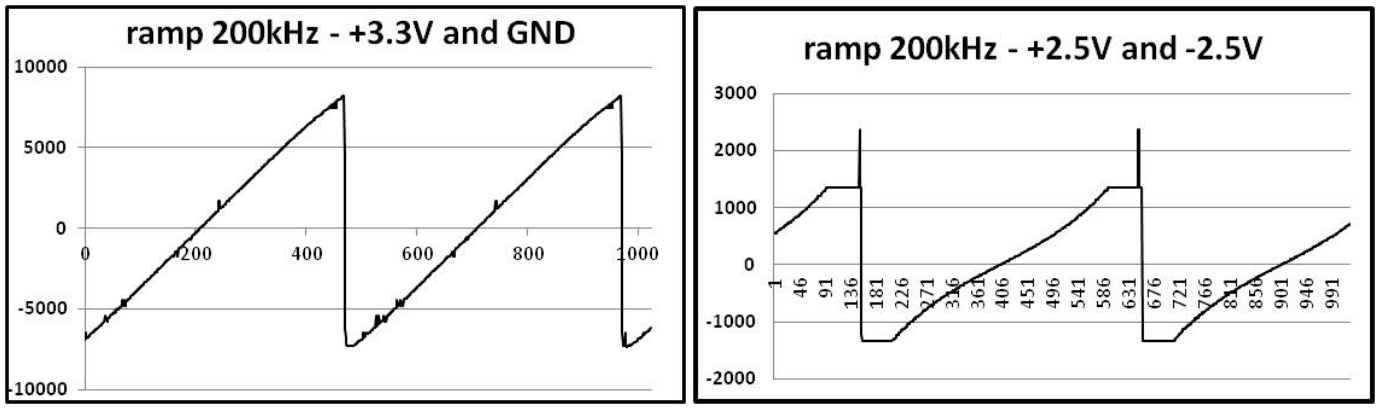


Fig. 9 – Huge differential non-linearity for a single power supply +3.3V and a saturation on ca. 20% of range. A integral nonlinearity is also visible. Both configurations recommended by Texas Instr. do not operate correctly on the Texas ADS4249 Evaluation Module.

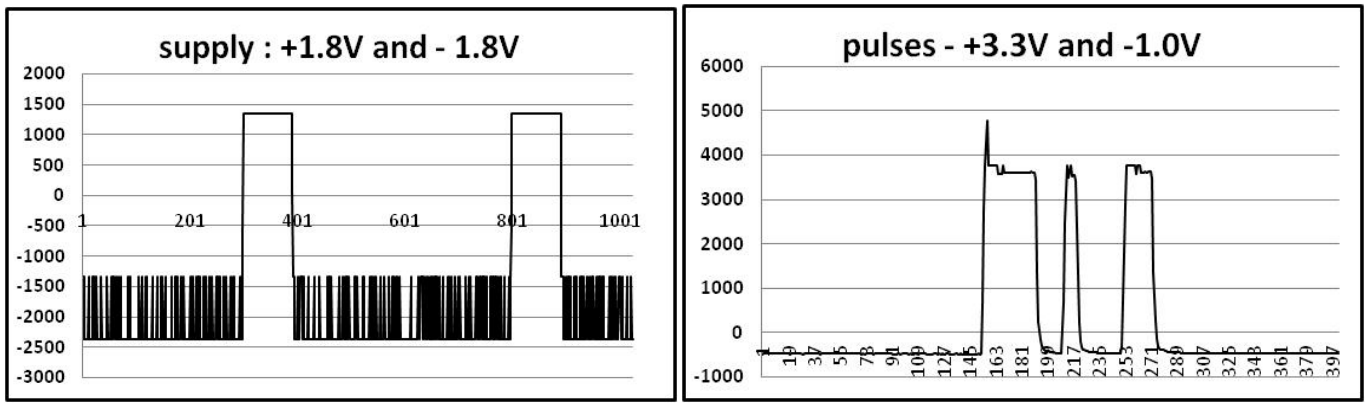


Fig. 10 – Oscillations for a symmetric supply +/-1.8V. Suspicious spikes and pulse distortions for an asymmetric supply: +3.3V and -1.0V.

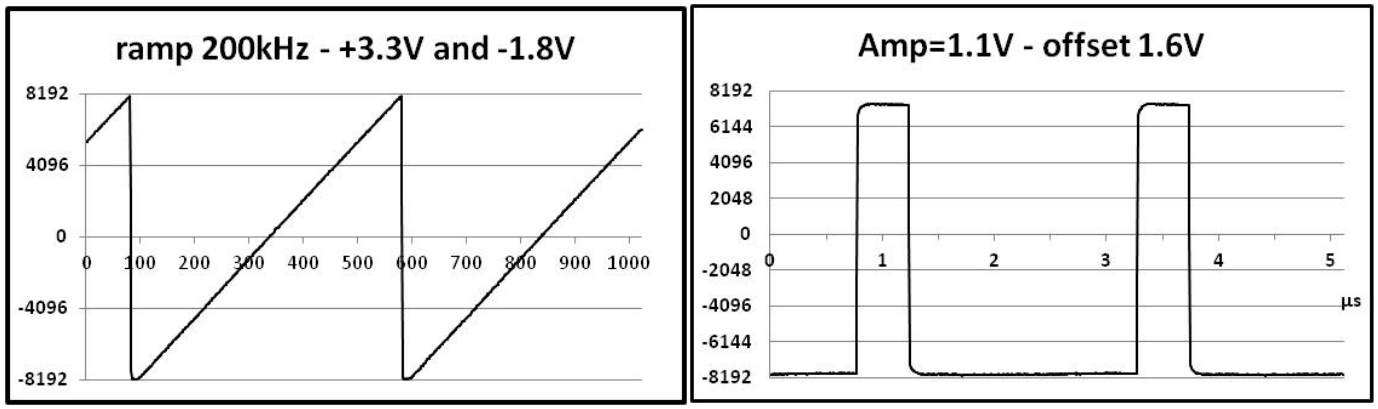
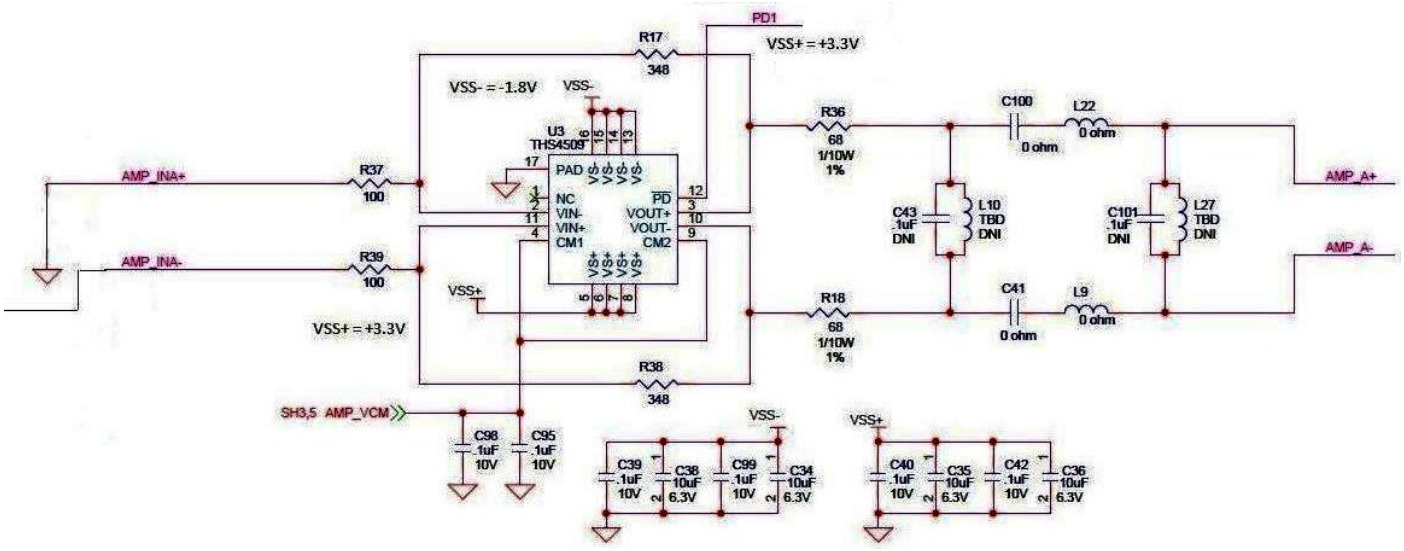


Fig. 11 – A perfect digitalization obtained finally for the asymmetric supply: +3.3V and -1.8V



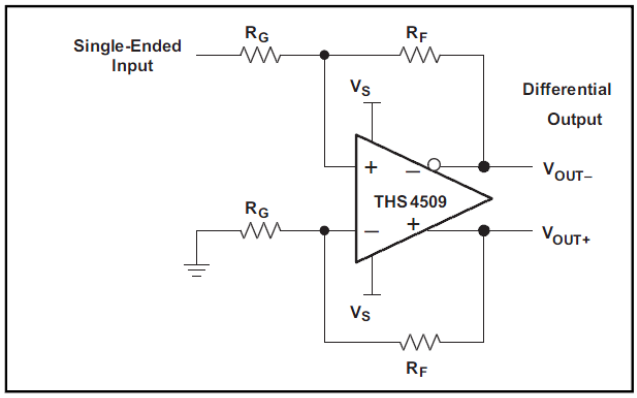


Figure 82. Single-Ended Input to Differential Output Amplifier

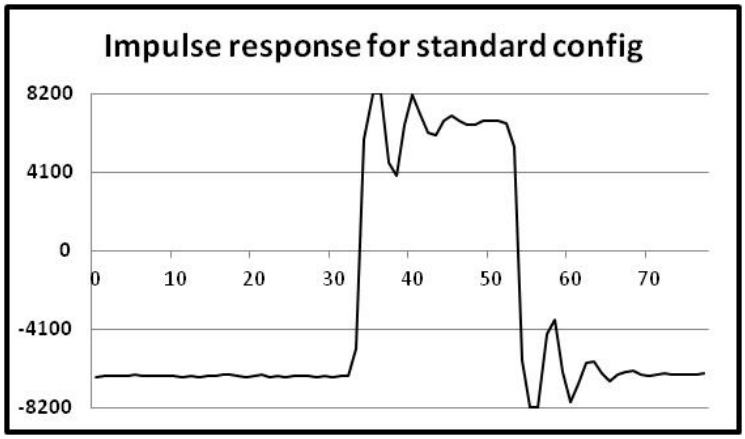


Fig. 12 – Recommended configuration (Figure 82 from ADS4249 documentation) implemented on the ADS4249EVM gives a distorted pulses

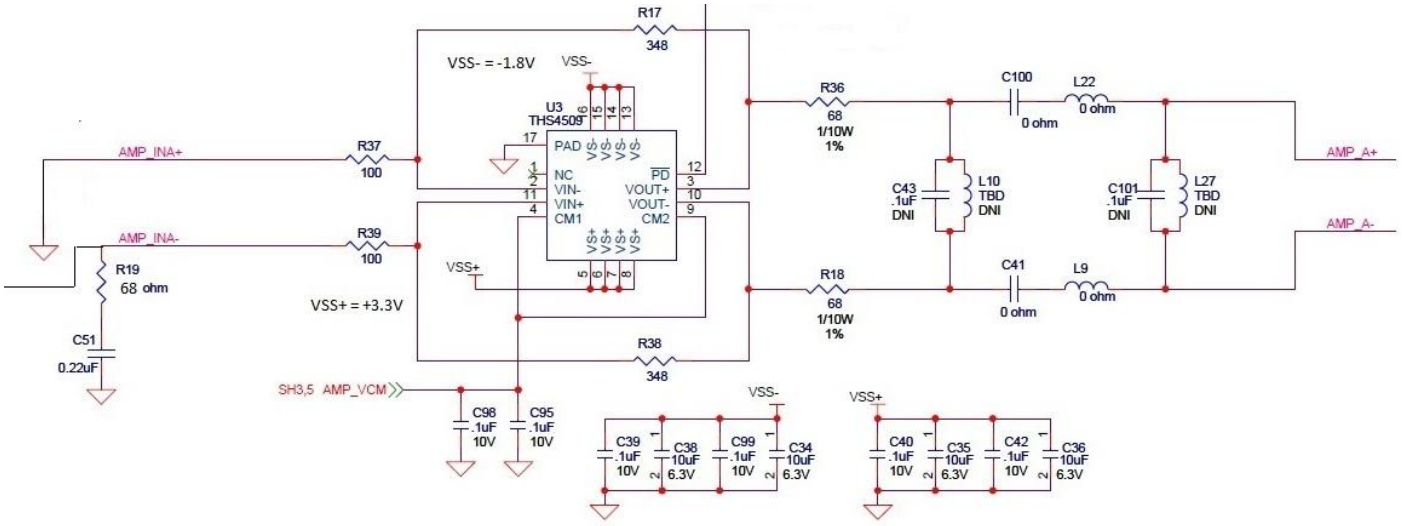


Fig. 13 – A compensation with R19=68 Ohm and C51=0.22uF

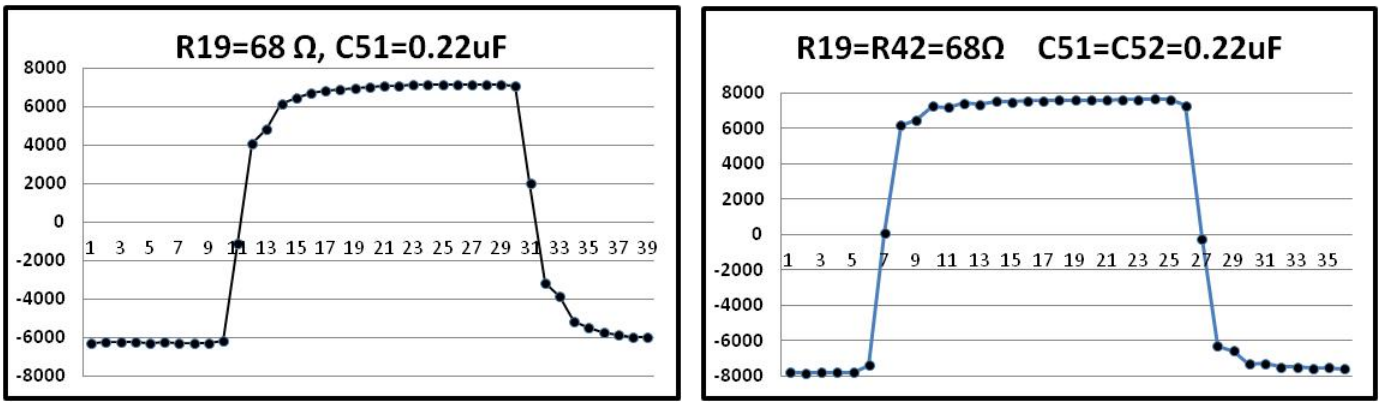


Fig. 14 – An additional high frequency compensation (according to Fig. 15) improves a rising and falling edges time crucial for precise timing analysis.

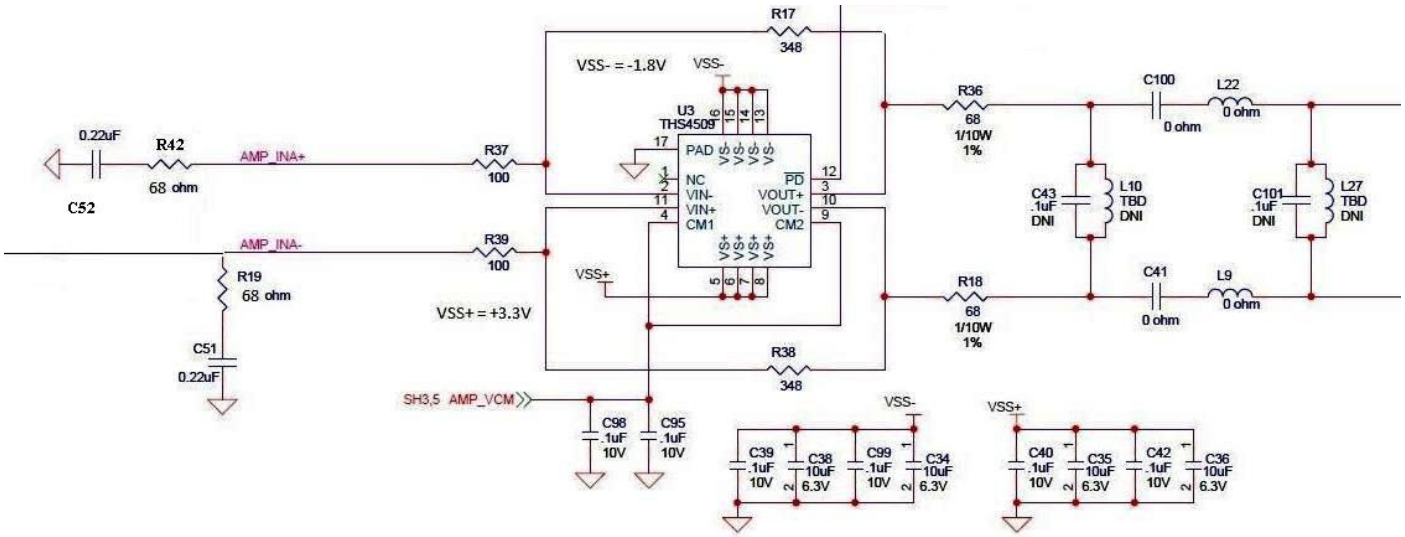


Fig. 15 – Additional compensation In VIN- line. C52 significantly changes the pedestal for the ADC.

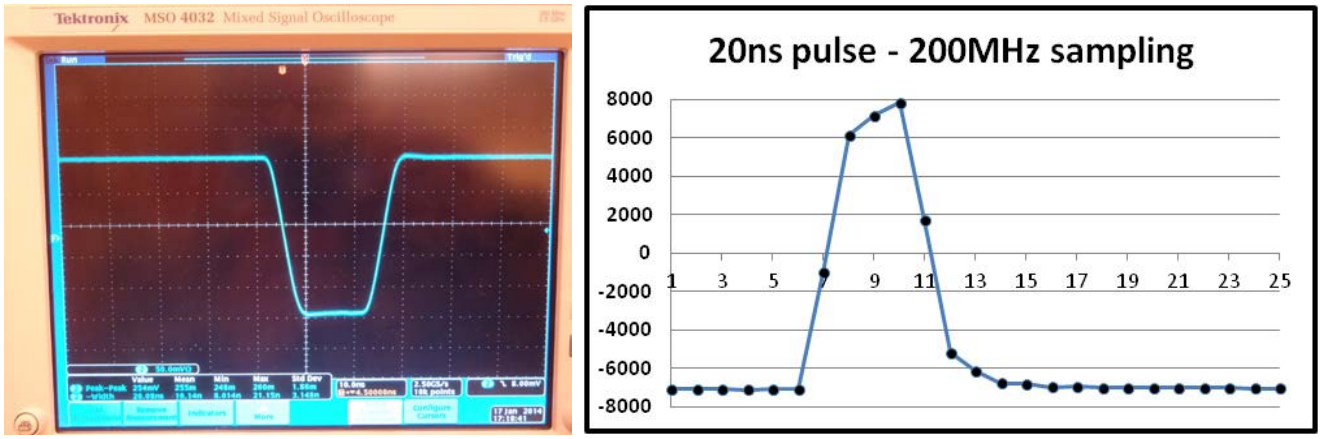


Fig. 16 – A response on 20 ns pulse

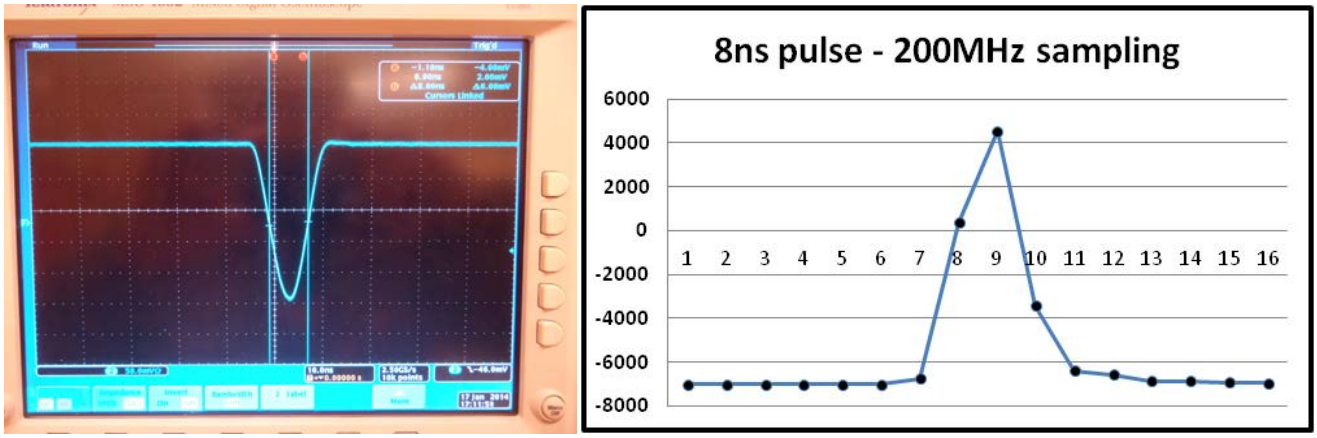


Fig. 17 – Response for very short pulses.

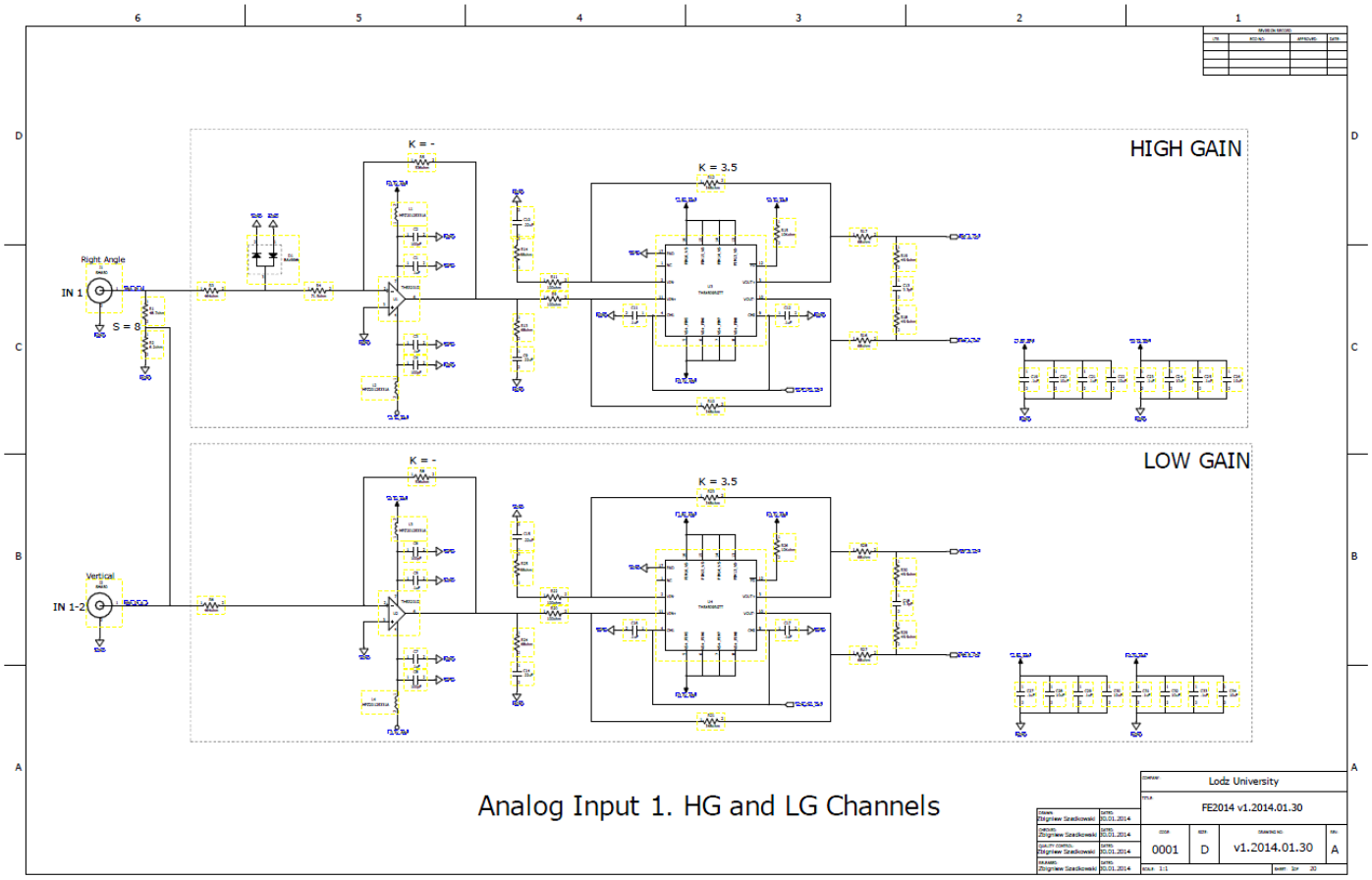


Fig. 18 – Final design of the analog section. No internal anti-aliasing filters.

Fig. 19 – Ordered filters for the prototype. Bessel low-pass

Attention: Filtronetics, Inc.

Date: 2014-01-23

End User Statement

Type all information. Do Not Leave Blanks in any section above.
When completed print on your Company Letterhead and return to Filtronetics, Inc. in a PDF Format.

Reference Quote or Purchase Order Number:	6 Dated: 2014-01-23
Purchasing Company Name, Address Phone Number:	Faculty of High-Energy Astrophysics, University of Lodz 90-236 Lodz, Pomorska 149, POLAND +48 42 635 56 59 Tax ID:724-000-32-43
Purchasing Company Contact Name and Title Email Address	University of Lodz zszadkow@kfd2.phys.uni.lodz.pl
What is the role that the Purchasing Company has in this transaction?	Development of the prototype of the Front-End for cosmic rays experiment
Ordered Part Number and Description Quantity	FN-3126WF, Bessel – Low Pass, cutoff - 60MHz/1dB, 80MHz/30dB 6 – proposed price : 5USD/piece
Program Name/Platform Name:	ASPERA-2, ERA-NET
Military or Commercial Use If Military, give name of branch, *i.e.*, Navy, Army	No -
Will the end product be used in planes or ships or both? **If yes, give as much detail as possible.**	No
Will the system go into or communicate with a satellite? **If yes, give name of satellite.**	No
Will program be in relationship to NASA Programs ? Yes or No **If yes, name of NASA Program**	No -
Description of Application (What is the application for?) Provide names or model name of product.	Anti-aliasing filter in the Front-End for the surface detector of the Pierre Auger Observatory
End User Company Name Address Phone Number	Faculty of High-Energy Astrophysics, University of Lodz 90-236 Lodz, Pomorska 149, POLAND +48 42 635 56 59
What is the role that the End User has in this transaction?	Developer of the prototype of the next generation Front-End based on the Altera Cyclone V FPGA with 120MHz sampling and 14-bit resolution of ADC
Ultimate Consignee CompanyName Address Phone Number	Pierre Auger Observatory (http://auger.org/contact/) *Observatorio Pierre Auger, Av. San Martin Norte 304 (5613) Malargue, Prov. Mendoza, Argentina* - Tax ID:-
What is the role that the Ultimate Consignee has in this transaction?	Prototypes will be deployed in the real surface detectors on the Engineering Array for testing. The observatory plans to exchange full electronics in all 1680 detectors on the entire array. Prototypes will verify all assumptions for physics and technology.

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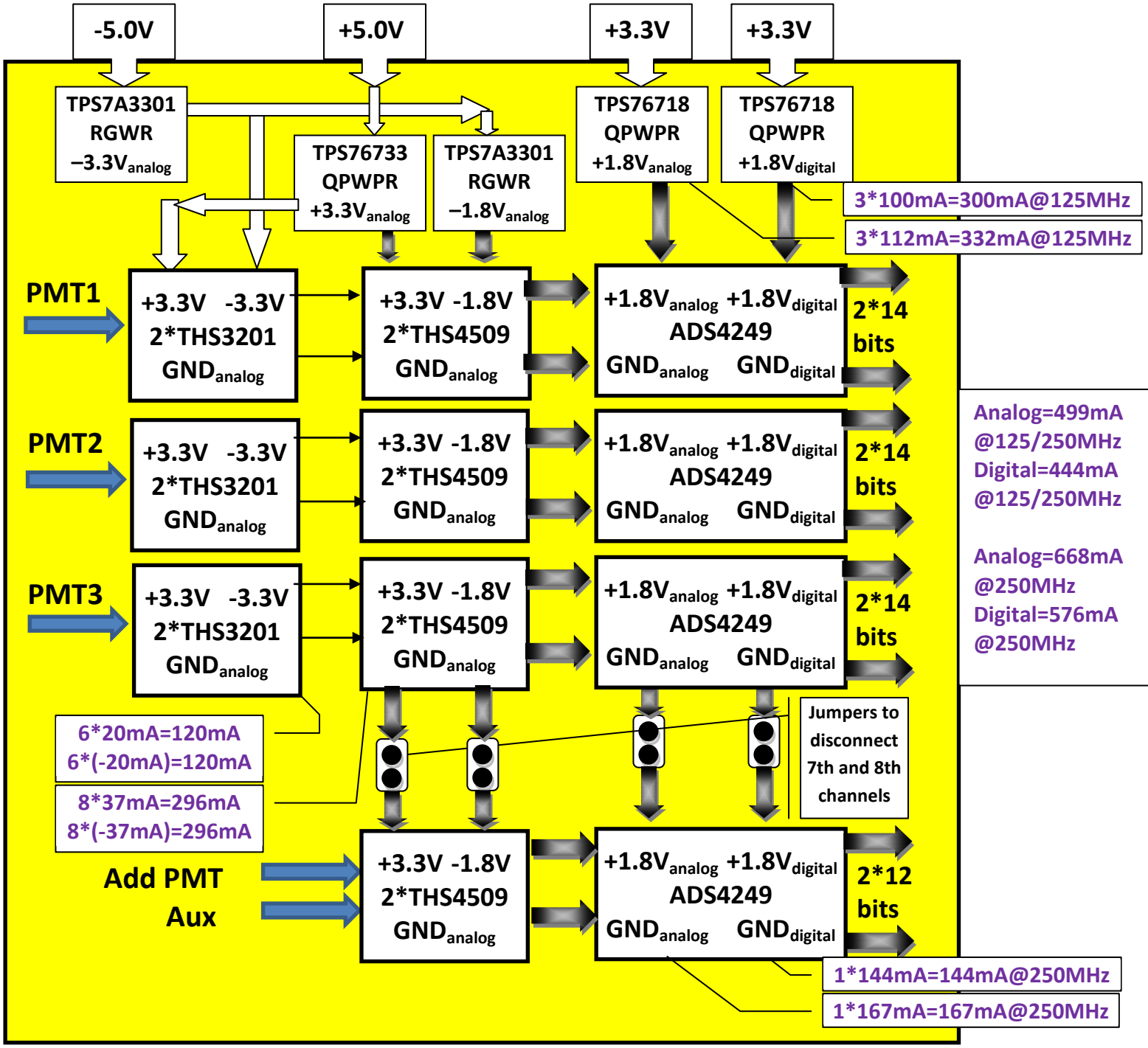

Fig. 20 – Schematic of the power supply. The analog section of the FEB does not use the internal UB analog supply +/- 3.3V. The FEB will be supplied from external DC-DC converters driven directly from the battery (+24V) .

Schematics finished.

PCB design in progress.

We resigned from the FHD video filters THS7372 as anti-aliasing ones. THS7372 supports 3 channels (RGB). However, if two channels HG and LG are connected to a single THS7372, a saturation in the HG channel makes a huge distortion of the signal in the LG channel. HG and LG channels should be implemented in a separated chips. This is uneconomic solution. A single chip (for 3 channels) takes 17 mA. We should use a single chip for each channel. It means 2/3*17=12mA in each chip would be wasted. Totally 72mA @ 3.3V => 230 mW. For this reason we ordered passive external filters to be able e.g. to increase sampling to e.g. 160 MHz.