Architecture of the front-end electronics interface of low and high gain channels for Auger upgrade

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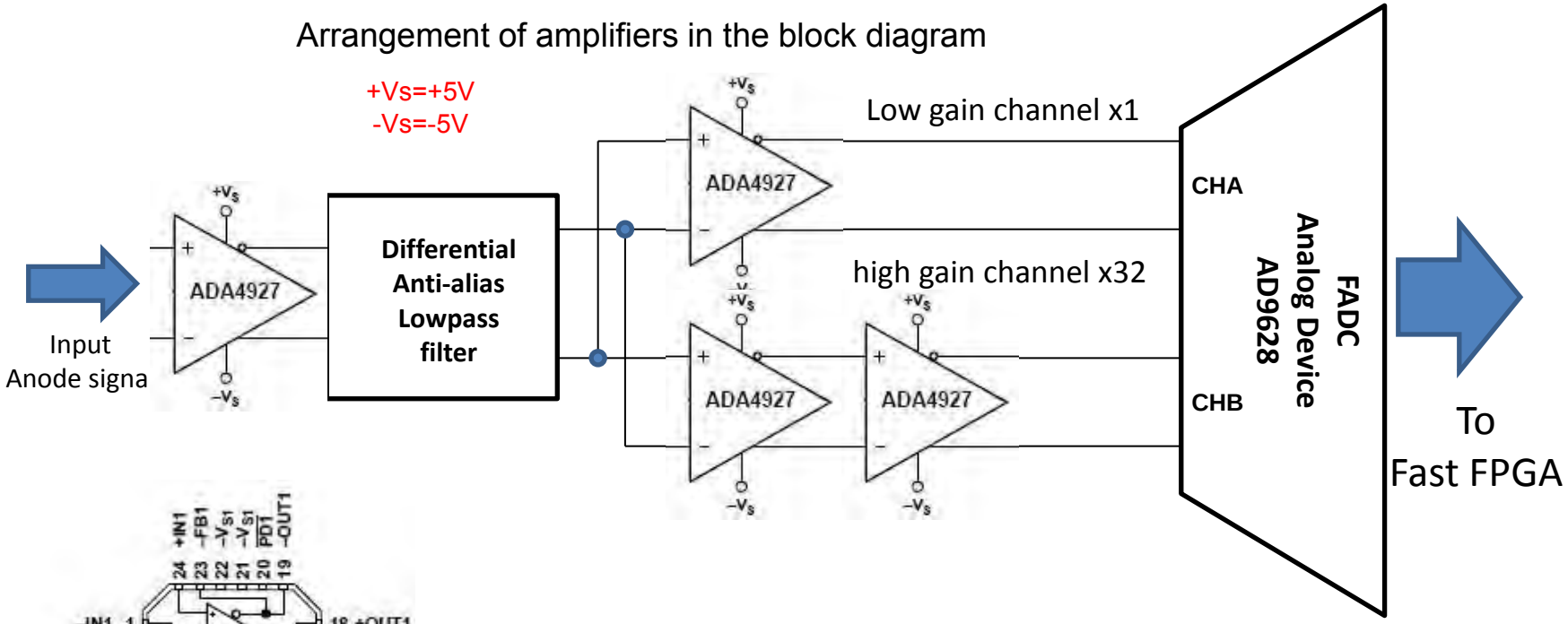
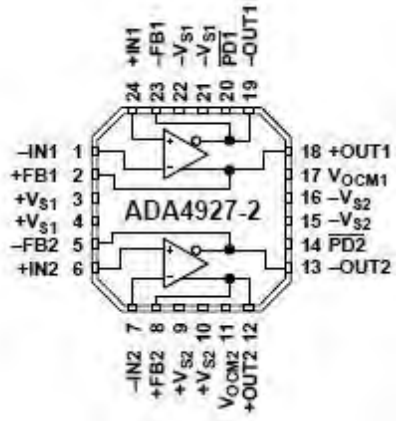
Front-end interface - Low Gain and High gain channels

Arrangement of amplifiers in the block diagram

+Vs=+5V
-Vs=-5V





ADA4927-2 is the final Analog Device microchip chosen.
four stages, two microchips

Features
Extremely low harmonic distorsion
Very Low noise 1.4nV /√Hz
Bandwith -3dB 2.3GHz
Differential line drivers

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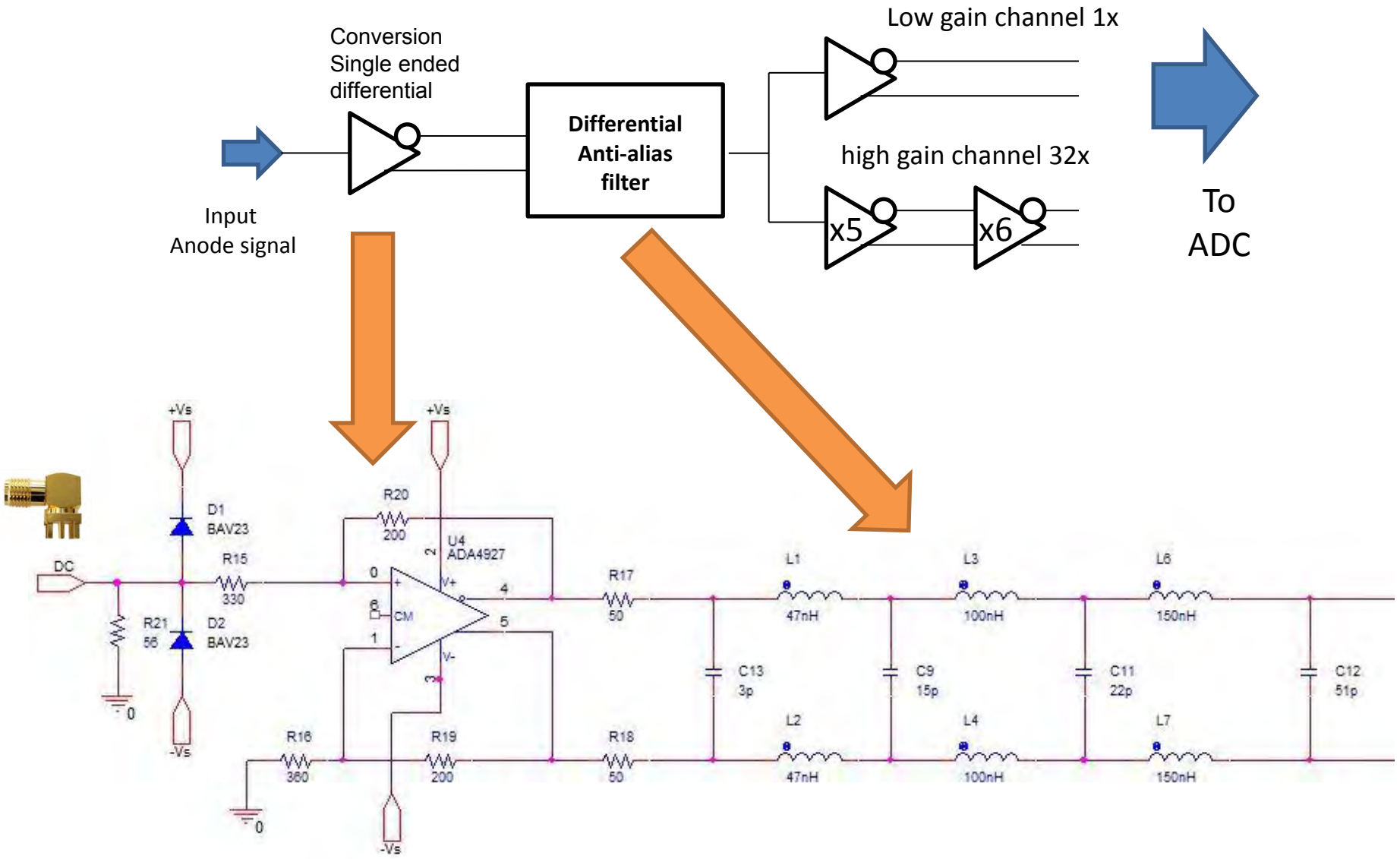
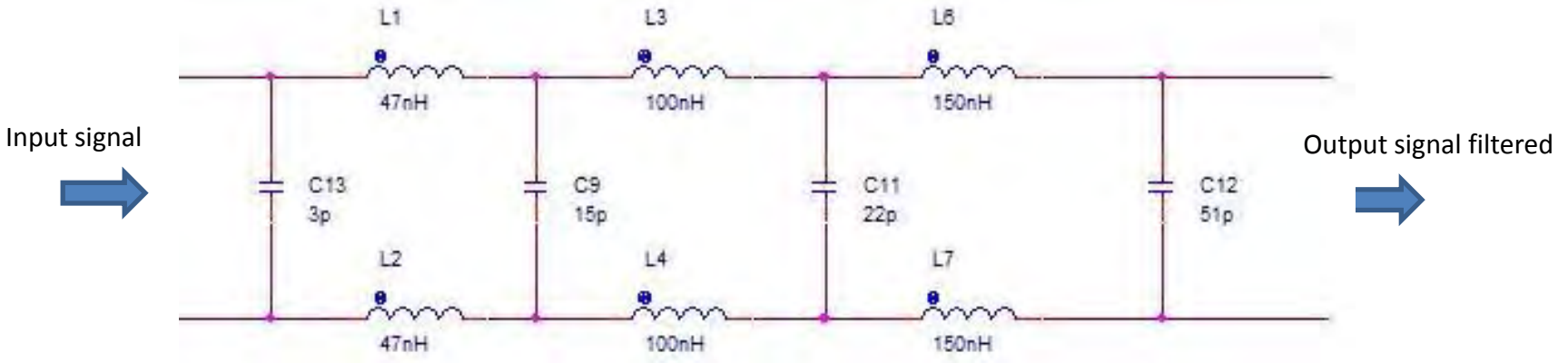
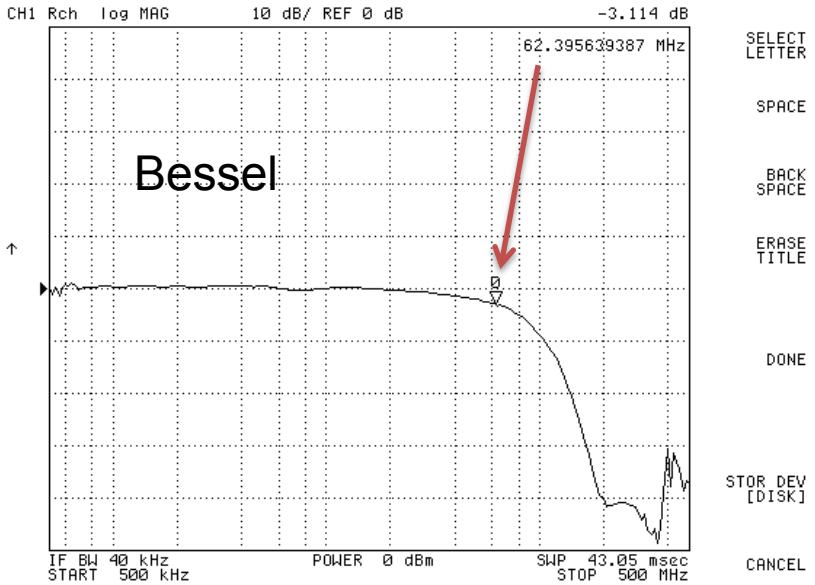
Differential convertion and anti-aliasing filter

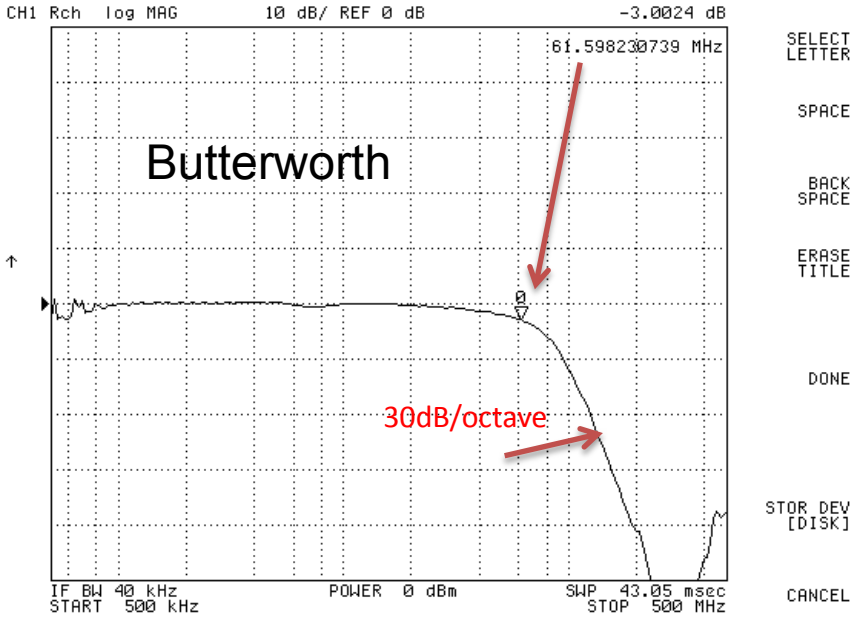


Anti Aliasing differential filter



We have calculated the anti aliasing filter in two modes Bessel and butterworth with 5 poles at 60MHz with the same circuit





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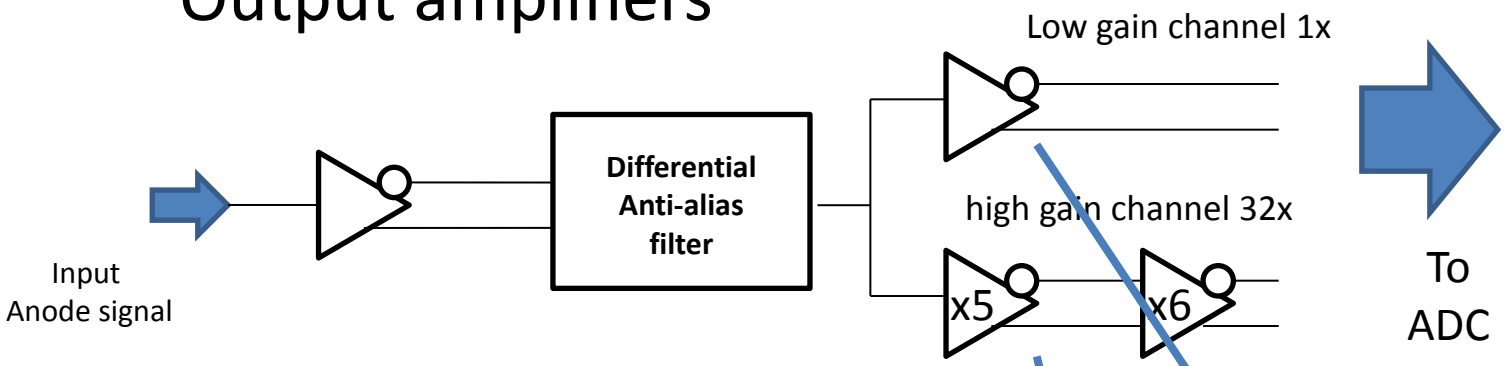
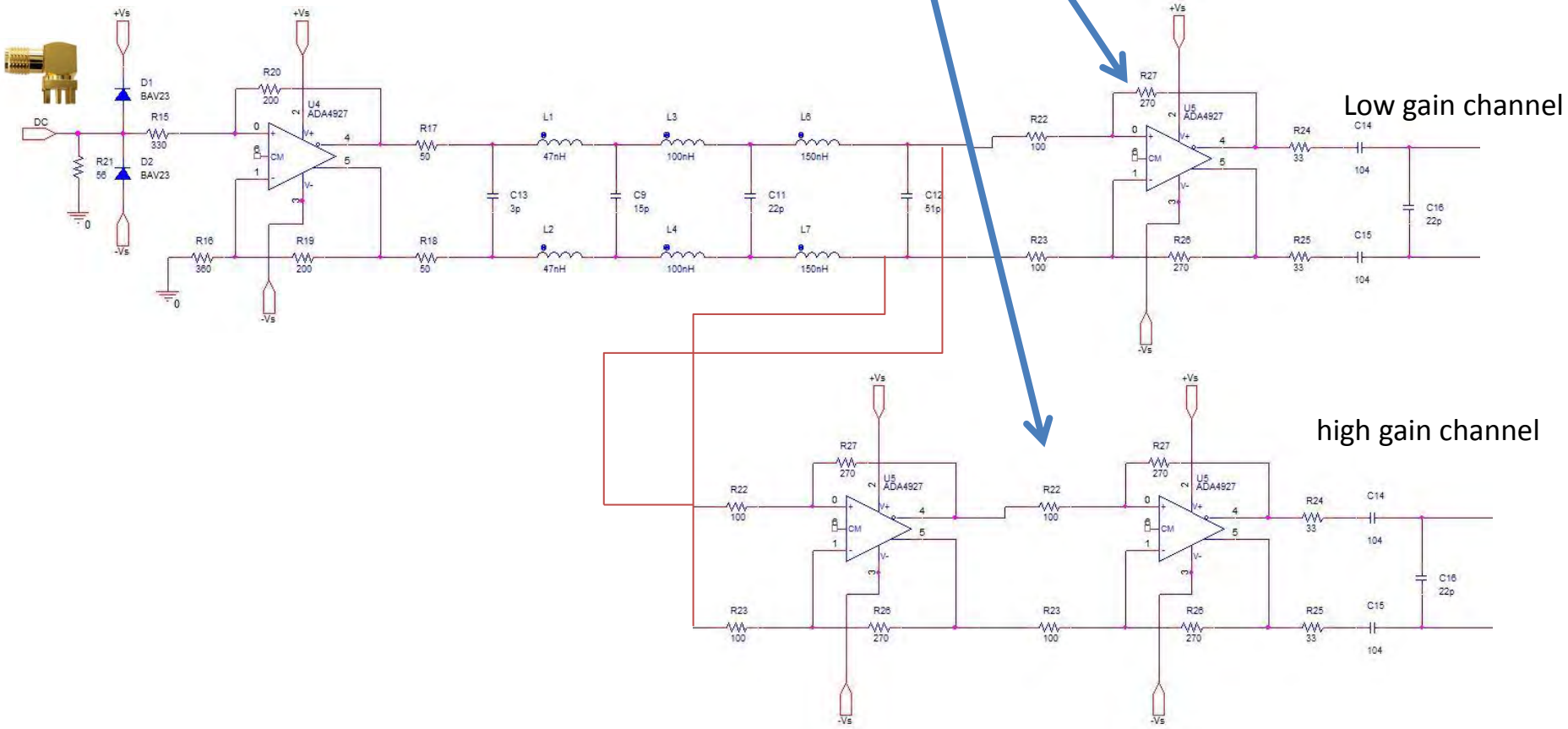
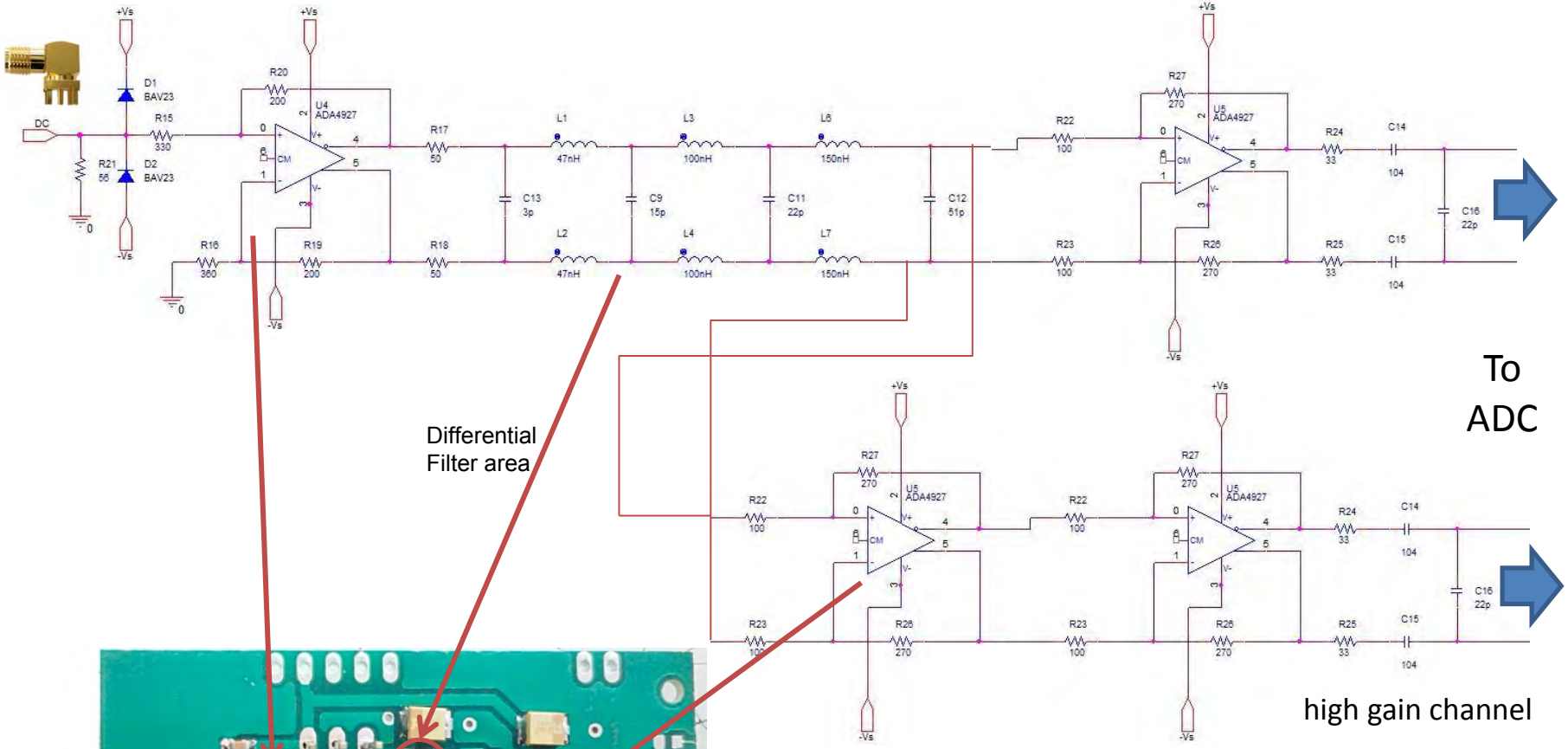
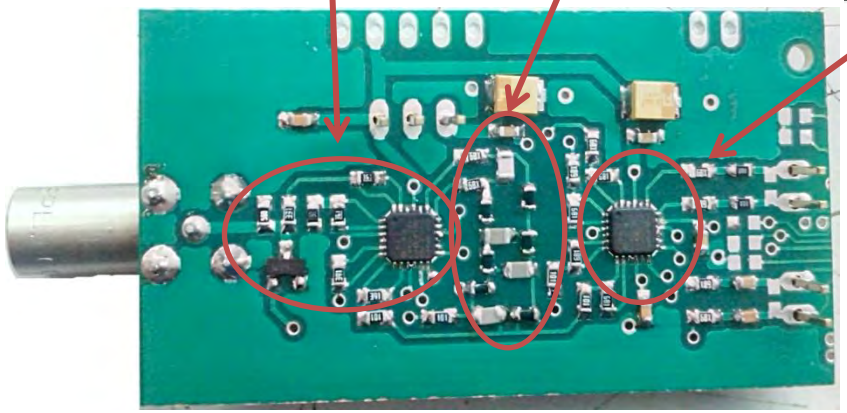
Output amplifiers



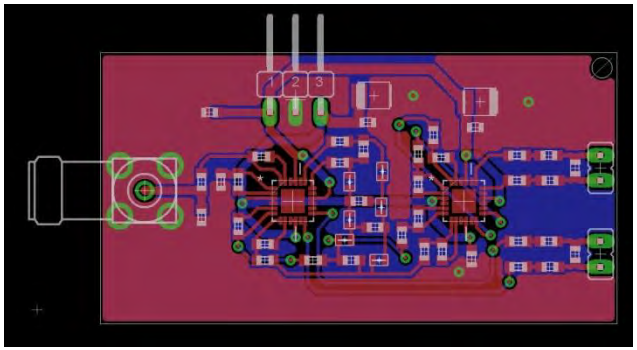


Prototipe of Front-end interface



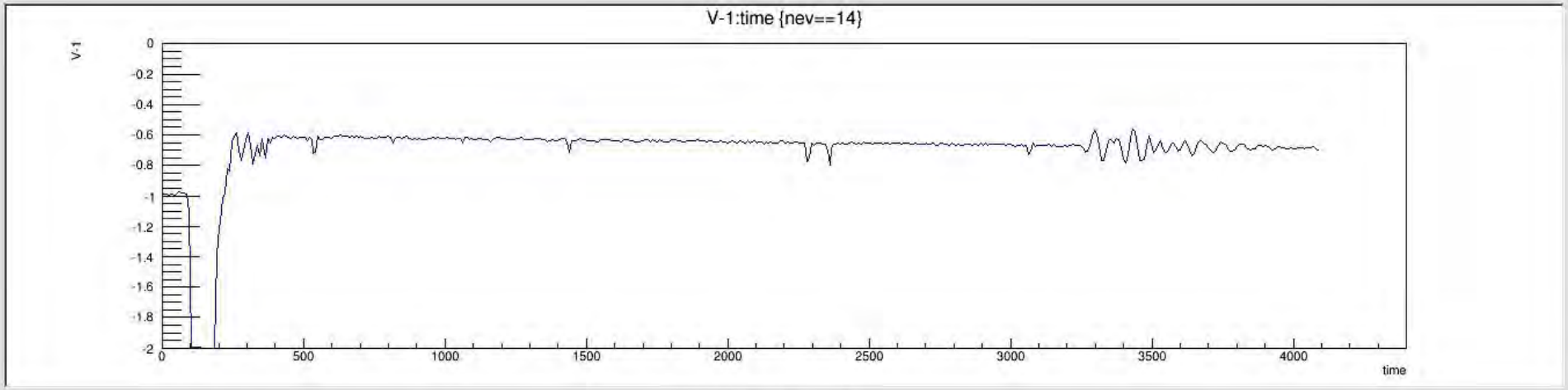


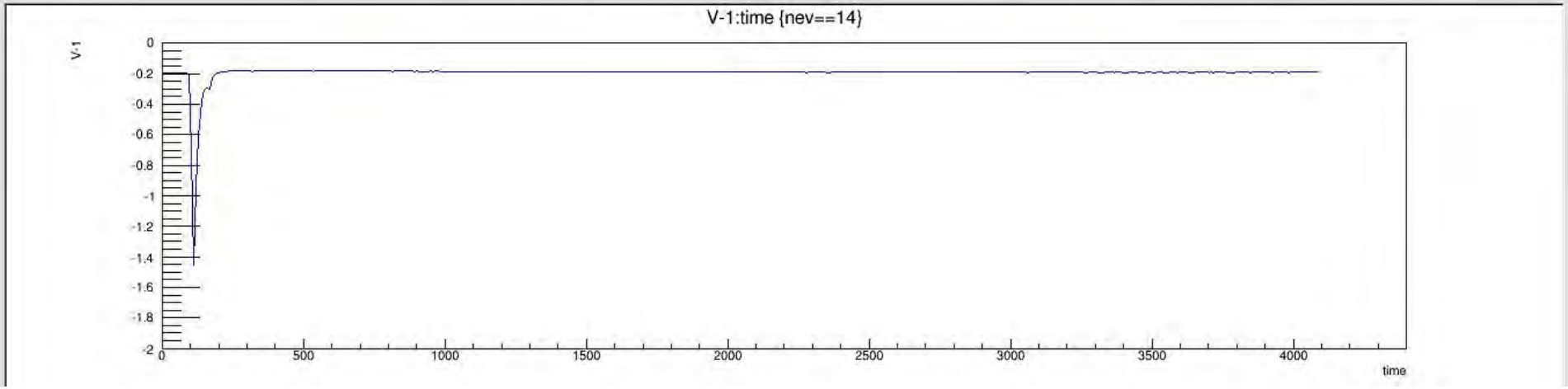
To
ADC



Placement of components on P.C.B. into the area reserved by WP5

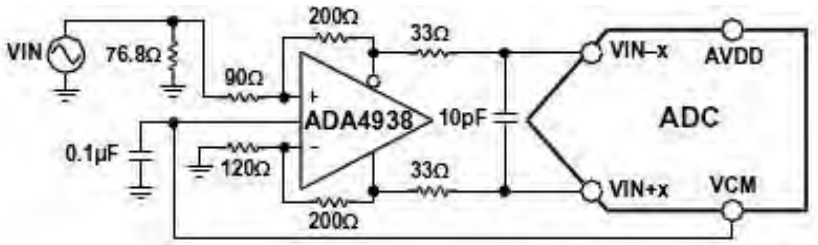
BASELINE DEFINITION

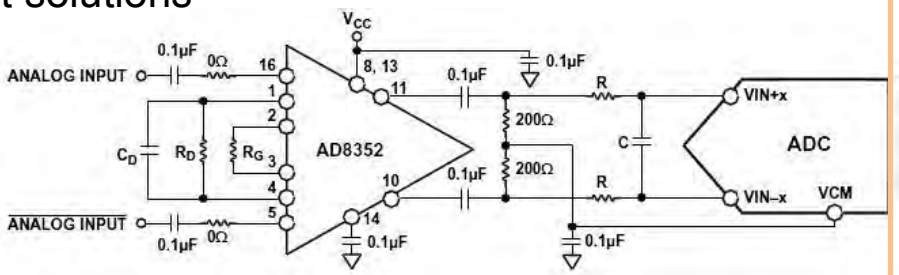




Offset problems and common mode voltage

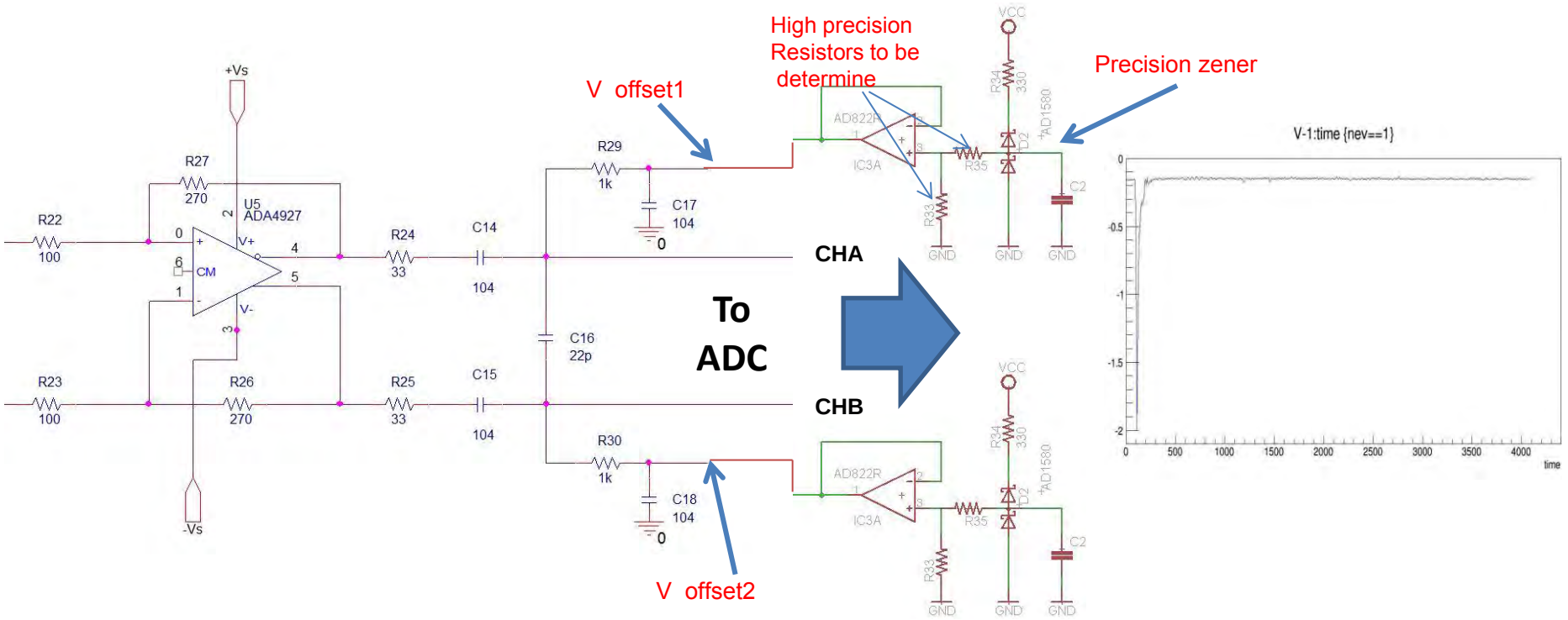
Data sheet solutions





Our solution to insert offset

We need to add to the signal a differential dc voltage component to move the reference line to obtain the maximum input dynamic

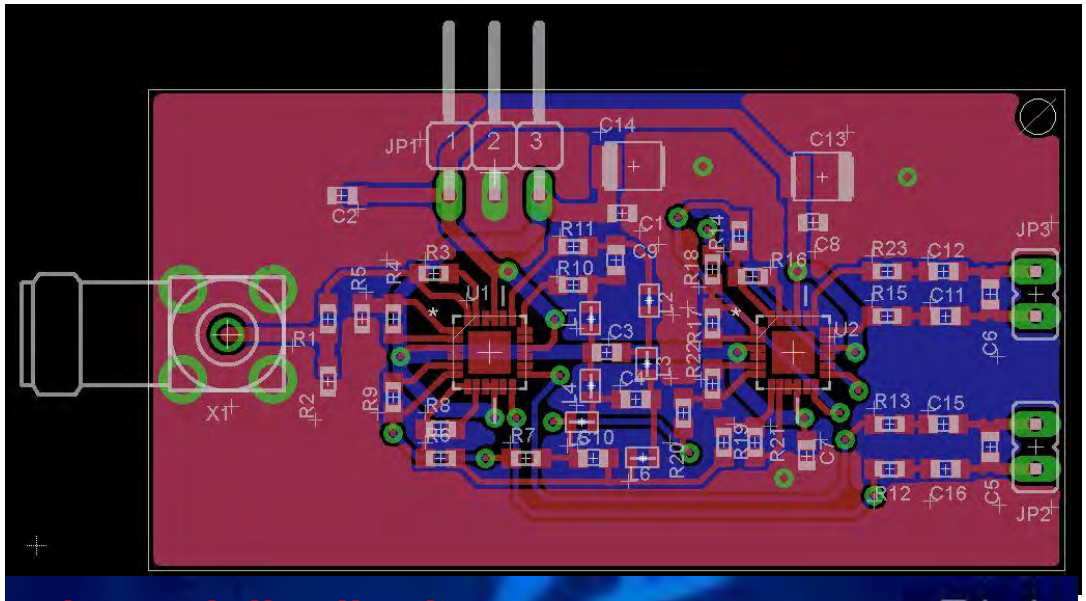


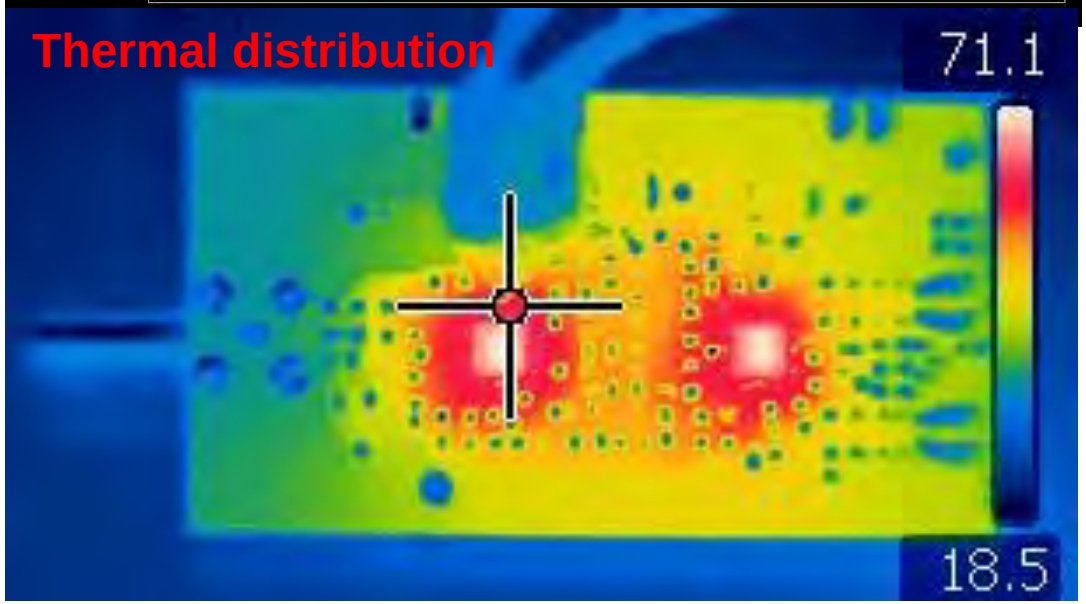
Front-end interface features

Power supply +5V -5V
Power consuption 800 mW

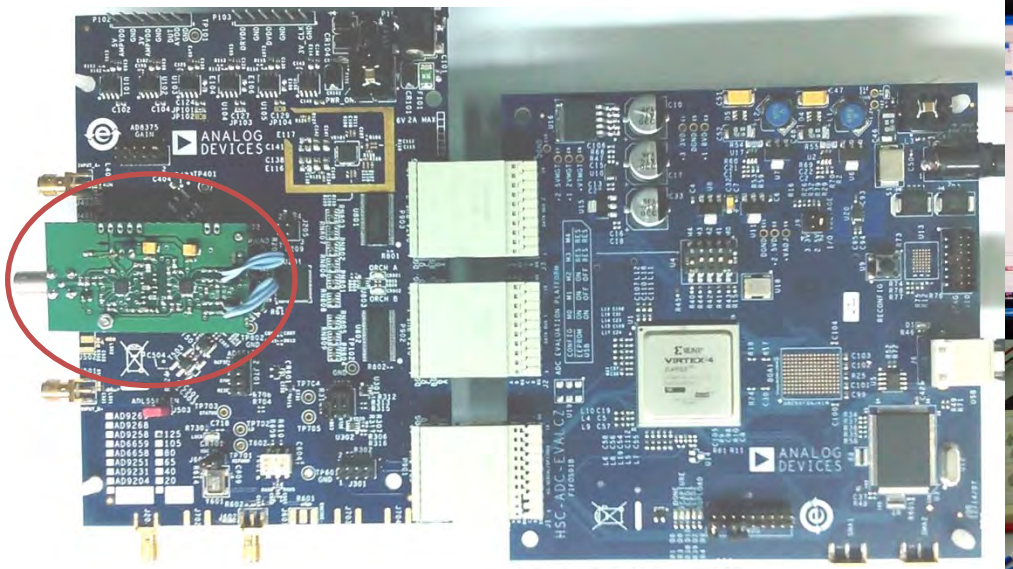
Bill of material

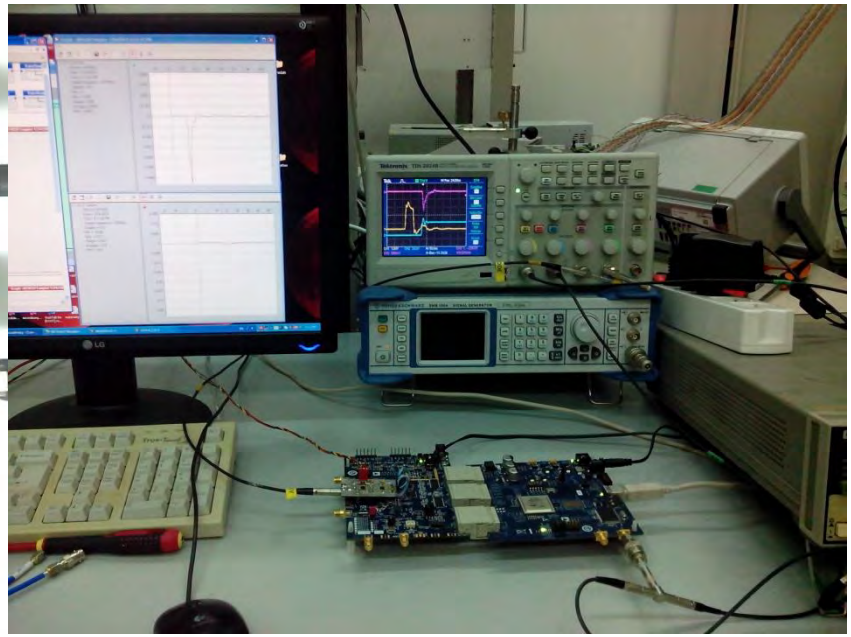
Qty	Value	Device	Parts
4		C-EUC0603	C1, C2, C7, C8
2		CPOL-EUSMCB	C13, C14
2		JP1E	JP2, JP3
1		JP2W	JP1
4		R-US_R0603	R19, R20, R21, R22
1	3p	C-EUC0603	C9
1	15p	C-EUC0603	C3
2	22	C-EUC0603	C5, C6
1	22p	C-EUC0603	C4
4	33	R-US_R0603	R12, R13, R15, R23
2	47nH	WE-KIHC_0603	L1, L2
2	50	R-US_R0603	R10, R11
1	51p	C-EUC0603	C10
1	56	R-US_R0603	R2
2	100	R-US_R0603	R6, R7
2	100nH	WE-KIHC_0603	L3, L4
4	104	C-EUC0603	C11, C12, C15, C16
2	150nH	WE-KIHC_0603	L5, L6
2	200	R-US_R0603	R8, R9
2	330	R-US_R0603	R1, R18
5	360	R-US_R0603	R3, R4, R5, R16, R17
1	380	R-US_R0603	R14
2	ADA4927-2YCPZ		U1, U2
1	BU-SMA-H	BU-SMA-H	X1

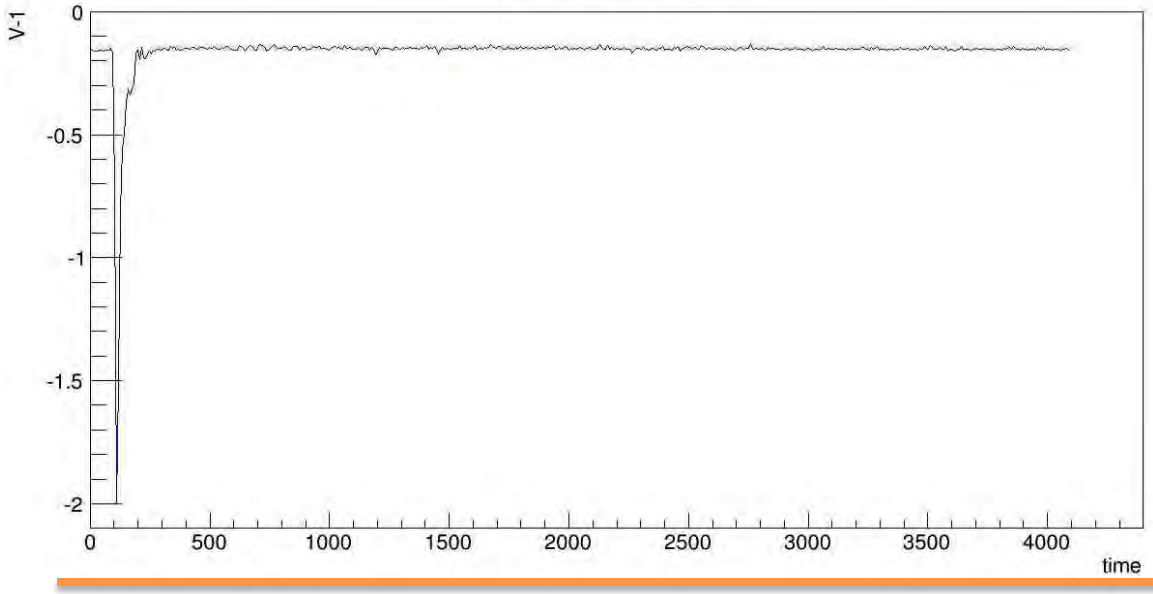




Front-end application on Analog Device evaluation board







Typical graphical rappresentation of acquired signal from PMT by analog device evaluation board

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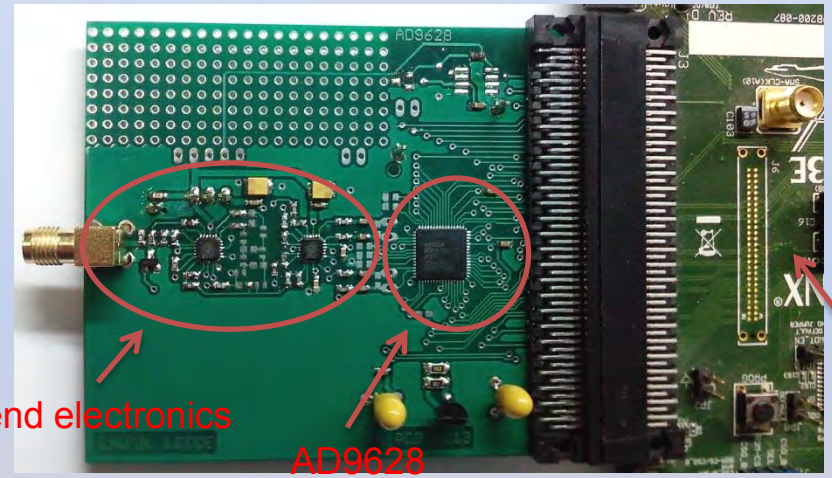
Next Step

Work in progress for prototyping of the board with analog front-end connected with fast ADC and xilinx spartan 3



More information about the status of the works to:
http://elettronica.le.infn.it/?page_id=216

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