Auger SDEU WP1 Meeting, January 2014 - Grenoble

SDE Upgrade

WP5 – STATUS REPORT

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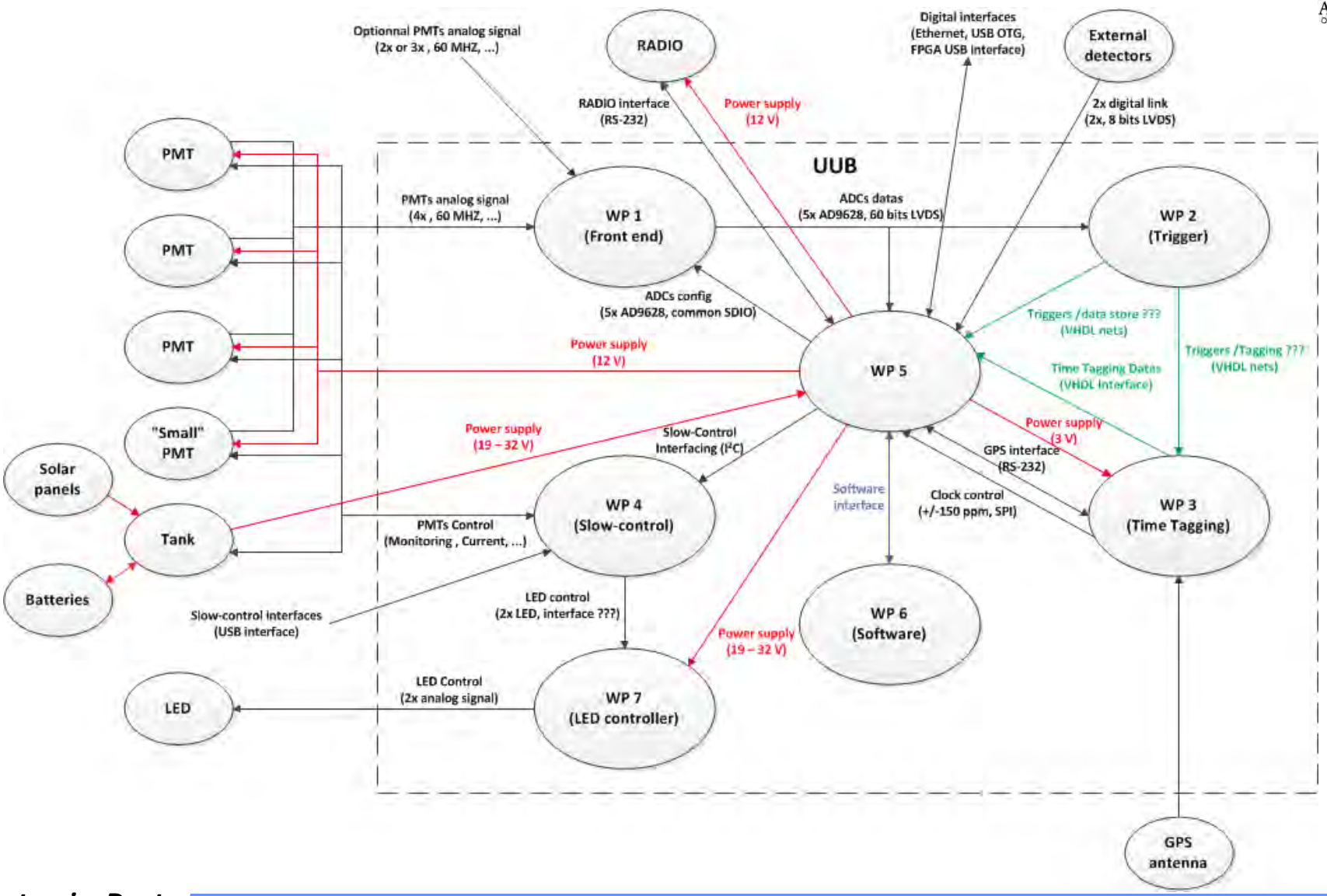
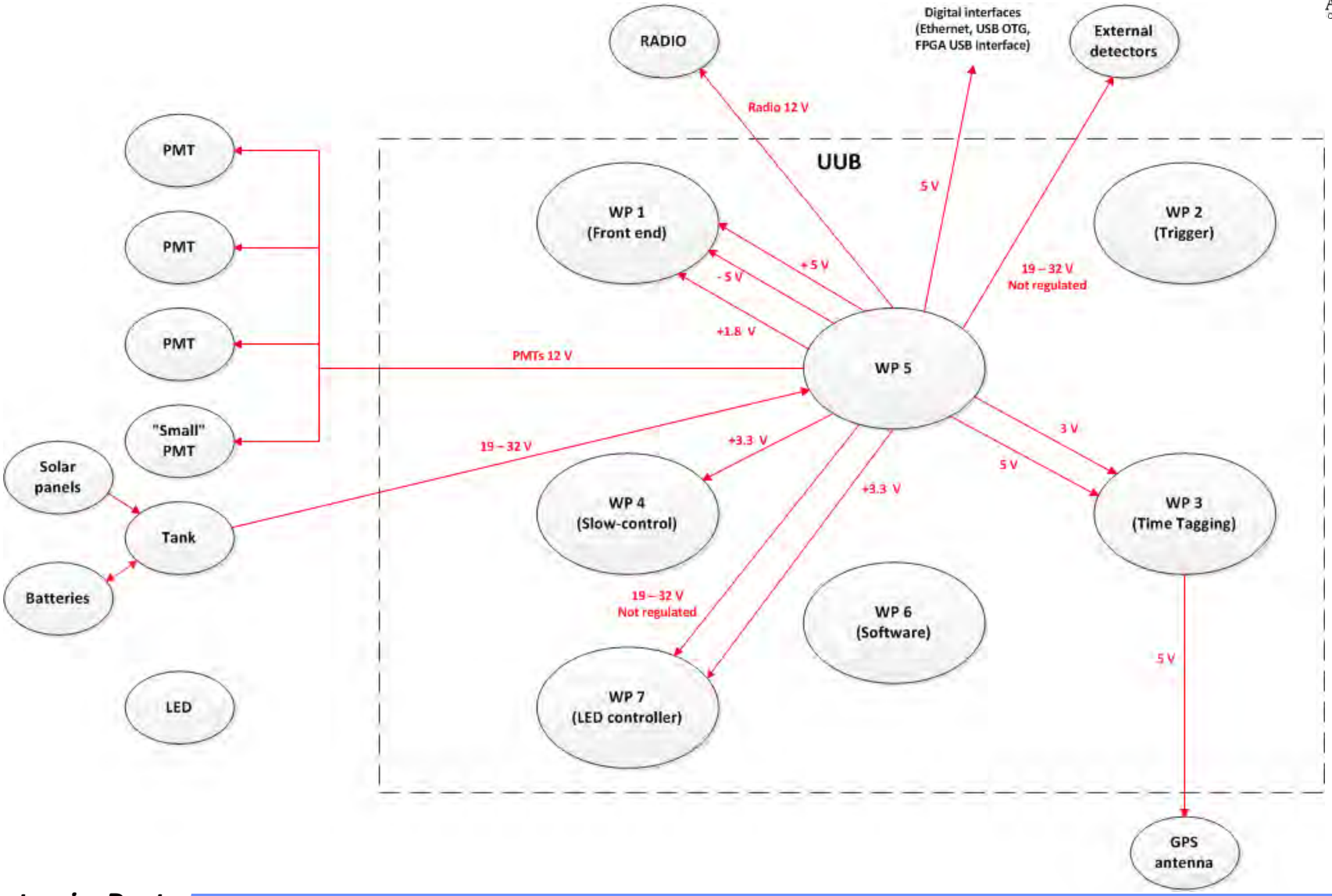
SDEU specifications

10x ADCs 12 bits 120 MS/s
Dual µ-processor ARM Cortex A9 333 Mhz
4 Gbits LP-DDR2 memory (Low Power DDR2)
1 Gbits Flash memory (storage memory)
i-LOTUS GPS (**TBC**)
LINUX
Online VHDL & software updatable
Industrial power supply connector (IP67)
Ethernet (Front panel)
OTG USB (to add an external electronic)
Slow-control and system USB control interface

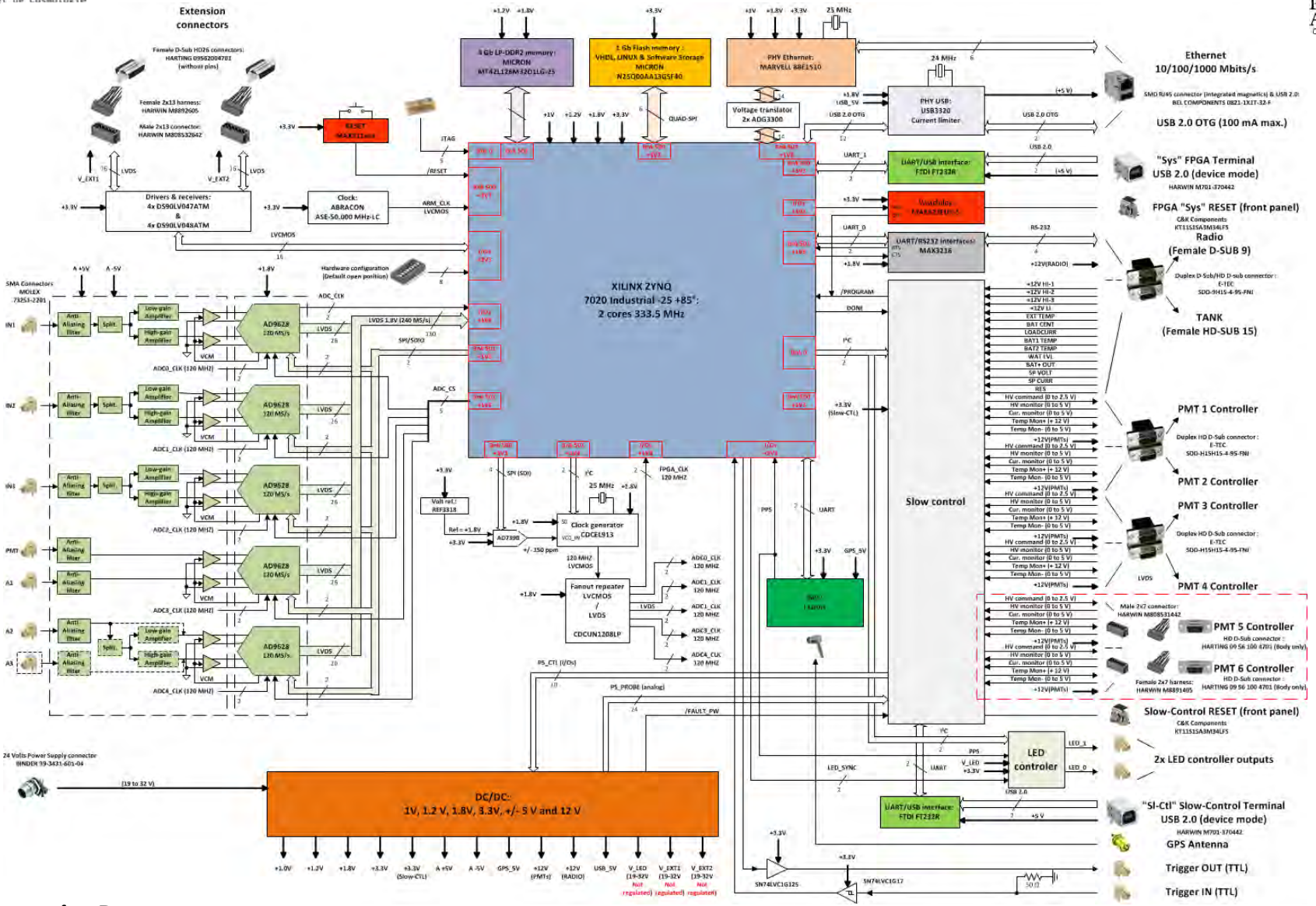
Global WP design interfaces



Power WP design interfaces



Global UUB Schematic



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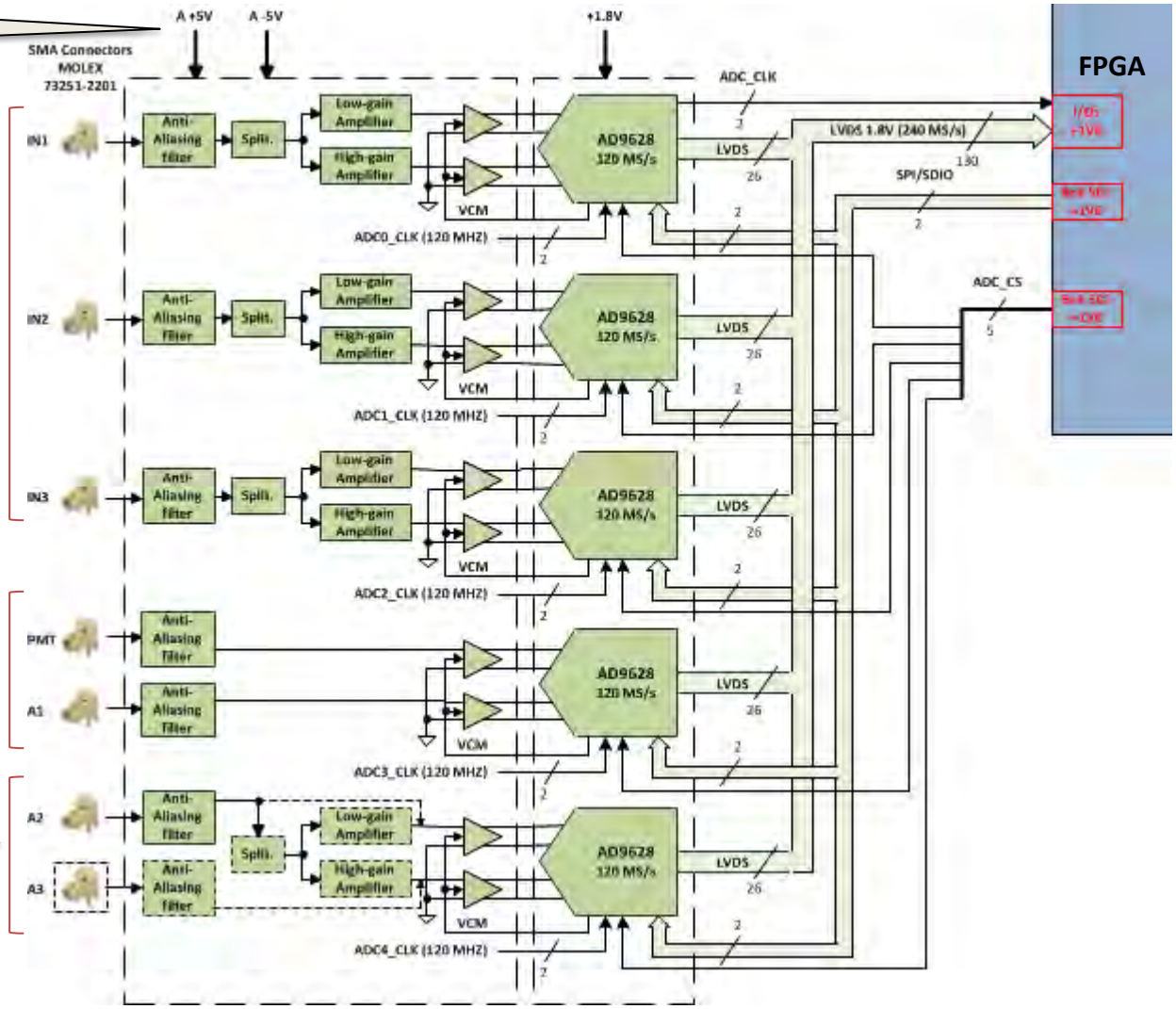
Front-end interface

Dedicated Power supplies: +/- 5 V



Type 1

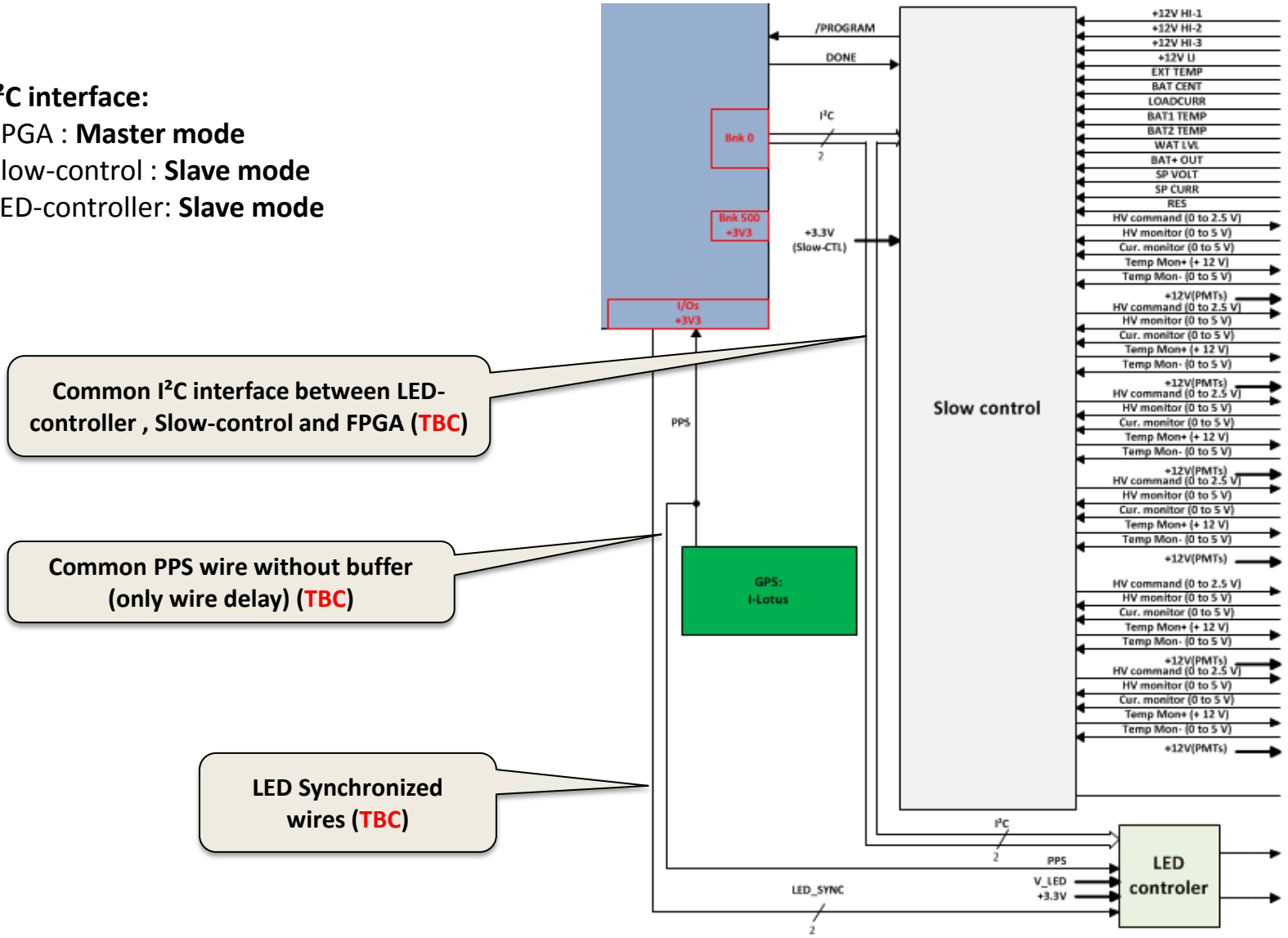
Type 2

Estimate power:
ADCs: **1400 mW**
Diff. Amplifiers: **1000 mW**
Gain Amplifiers: **168 mW (TBC)**
Anti-Aliasing filters: **??? (TBD)**

Design could provide type 1 or 2(TBC)

LED-Controller interface

I²C interface:
FPGA : **Master mode**
Slow-control : **Slave mode**
LED-controller: **Slave mode**



Common I²C interface between LED-controller , Slow-control and FPGA (TBC)

Common PPS wire without buffer (only wire delay) (TBC)

LED Synchronized wires (TBC)

Absolute peak power estimate

MUST BE UPDATED

Work Package	Functions	Devices	Maximum current (mA) / power supply (V) / Devices										Max Power / Devices	Nb.	Powers	Powers / WP
			FPGA				Slow C	Analog		GPS	USB	Radio	PMT				
			1	1,2	1,8	3,3	3,3	5	-5	5	5	12	12				
WP1	Front-End	Anti aliasing filter (TBD)						0						0	3	0,00	
		Low-gain path filter proposal						2,8	2,8					28	3	84,00	
		High-gain path filter proposal						2,8	2,8					28	3	84,00	2567,50
		Differential amplifier (ADA4938-2)						20	20					200	5	1000,00	
		12 bits ADC 120MS/s (Twin AD9628) proposa			155,5									279,9	5	1399,50	
WP2	Trigger	IN Digital Triggers (SN74LVC1G17)				0,5								1,65	1	1,65	
		OUT Digital Triggers (SN74LVC1G125)				0,5								1,65	1	1,65	56,10
		Test connector (32 signal,) (2x 74LCX16245)				8								26,4	2	52,80	
WP3	Time Tagging	GPS (I-LOTUS: ref ???)				52								171,6	1	171,60	301,60
		Antenna (Type II ref ???)								26				130	1	130,00	
WP4	Slow Control	µ-controller (MPS430F2618)					9,5							31,35	1	31,35	
		LED flasher controller (DAC 4 outputs : AD5624)					0,85							2,805	1	2,81	
		DAC (LTC2637-12)					1,3							4,29	1	4,29	67,55
		Ampliers (LT1112)					0,88							2,904	10	29,04	
		MUX (ADG608)					,01							0,0165	4	0,07	
WP5	VCO/ fanout/ Clock_ADC	**Clock generator (with VCO control) & DAC :**															
		Clock generator with external VCO control (CDCEL913)			11,7									21,06	1	21,06	
		LVDS double fanout repeater (CDCUN1208LP)			85									153	1	153,00	
		DAC VCO control (AD7390 & REF3318: Rail to Rail)				1,5								4,95	1	4,95	
	FPGA (and µP)	Xilinx ZYNQ 7020 Industrial : 2 cores 333.5Mhz BRA	1864,8	150,15	432,6									2823,66	1	2823,66	
	Extention connector	**interface used an external electronic:**															
		Driver (2x DS90LV047ATM)				15								49,5	4	198,00	
		Receiver differential (DS90LV048ATM)				37								122,1	4	488,40	
	Watchdog/ RESET/ Clock CPU	WATCHDOG : MAX823EUK-S				0,012								0,0396	1	0,04	4785,86
		RESET : MAX811EUS-S				0,01								0,033	1	0,03	
		ABRACON ASE-50,000MHz-LC				19								62,7	1	62,70	
	Control	Switches												0	2	0,00	
	System Memory	LP-DDR2 Low Power4 Gb: MICRON MT42L128M32D1-25		210	10									270	1	270,00	
	Flash Memory	1 Gb : µ N25Q00AA13GSF40 @ 3.3 V (Wr cycle)				20								66	1	66,00	
	Interfaces	Radio RS232 (MAX3218)			3									5,4	1	5,40	
		Terminal USB interface (FT232R, powered by USB link)												0	2	0,00	
		Ethernet phy (MARVELL 88E1018 en mode EEE+2x ADG3300)	14		40	7								109,1	1	109,10	
		USB (USB3320)			46,4									83,52	1	83,52	
		External Slave USB Power									100			500	1	500,00	
WP?	PMT 1,2 & 3 PMT	Main PMT											44,44	533,28	3	1599,84	
		Small PMT (ESTIMATE POWER)											44,44	533,28	1	533,28	5632,32
WP?	RADIO											291,6		3499,2	1	3499,20	
		Total Current / power supply (mA):	1878,8	360,15	1406,2	324,522	20,47	116,8	116,8	26	100	291,6	177,76	**Total power (mW):**		**13410,93**	
		Power supplies efficiency (%):	93,00	89,10	93,50	94,00	87,00	93,30	82,20	90,90	94,10						
		Power under 7V power supply (mW) :	2020,22	485,051	2707,12	1139,28	77,6448	625,938	710,462	143,014	531,35						
		Power supplies efficiency (%):	97,10%									97,50%	97,00%				
		power supply (mW) :	8692,15									3588,92	2199,09				
		Internal Total Power supplies :	**14 480,16 mW**														

***without 6,4 Watts for the 2 external connectors**

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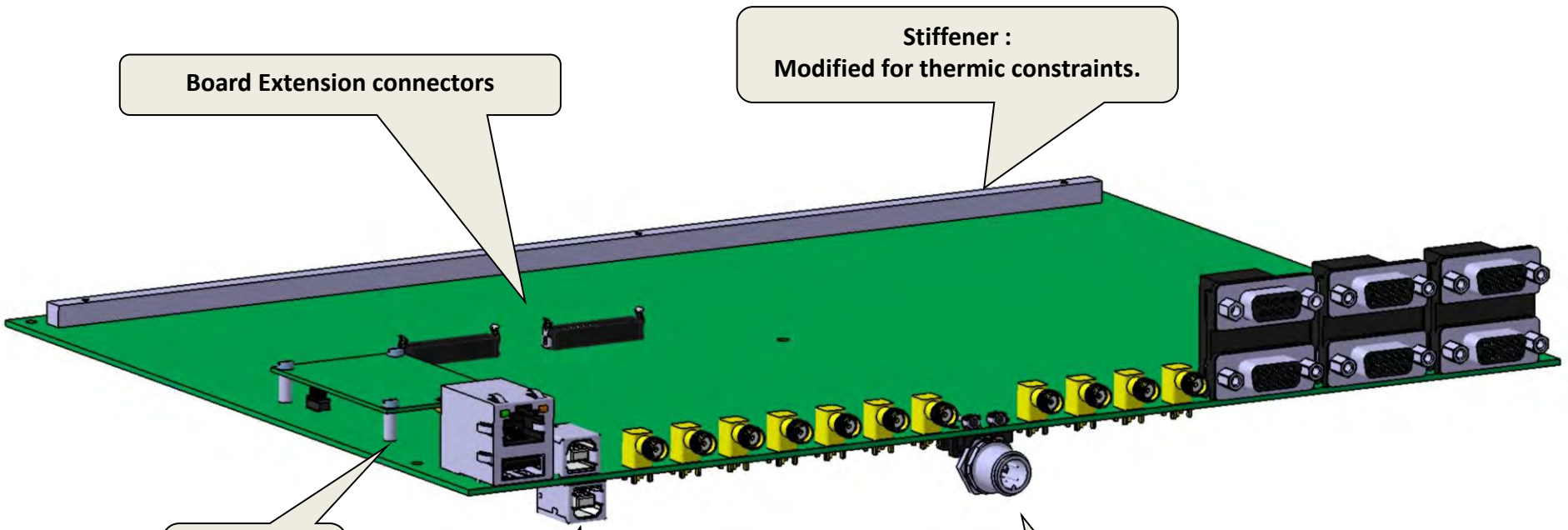
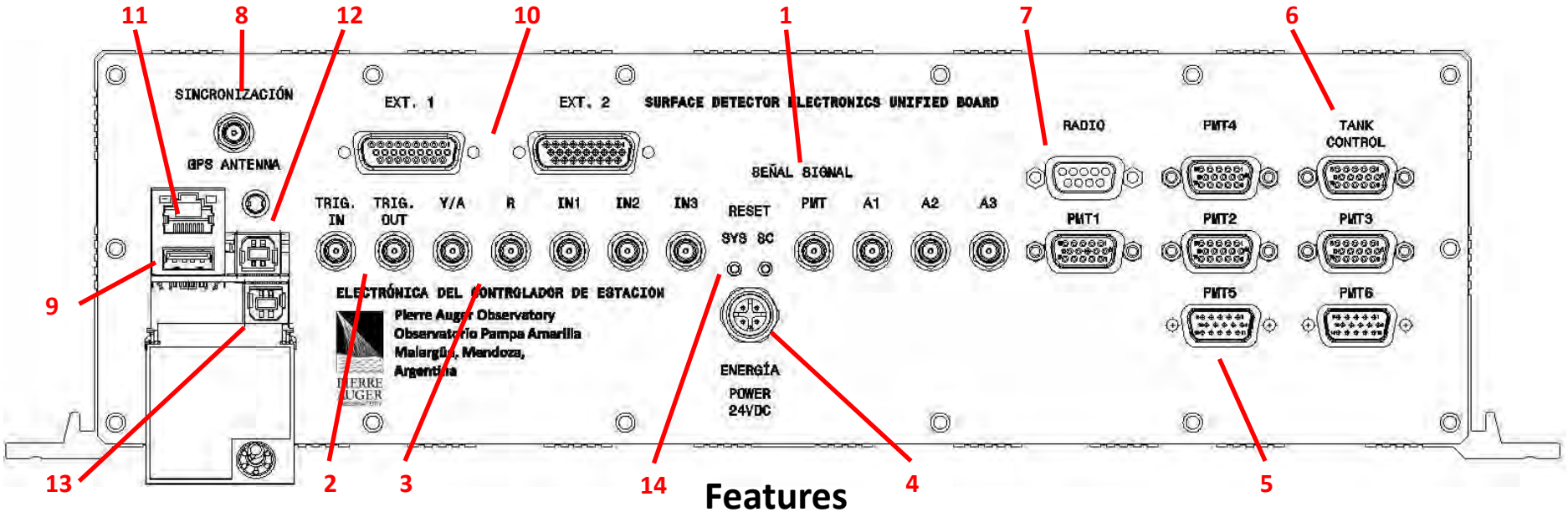
UB preview


Board Extension connectors
Stiffener :
Modified for thermic constraints.
GPS:
i-LOTUS
Ethernet, USB (OTG) (in same connector), Slow-control USB & System USB connectors
New 24 Volts power supply connector

SDE input/output connectors

Existing UB	Upgraded UB
6 analog inputs	**6 or 7** analog inputs
3 PMT control	4 PMT control
Ext control	Ext control
Trigger out signal	Trigger out signal
-	Trigger in signal
Power supply	Power supply (new connector)
2 switches	2 switches
2 LED-flasher control	2 LED-flasher control
"TEST" connector	-
"Console" connector	"Sys" connector with USB interface
	"Slow-Control" connector with USB interface
"Radio" connector	"Radio" connector
-	Ethernet 10/100/1000 Bits/s(Front panel)
-	USB OTG(Front panel)
	2x D-SUB 26 External extension connector

Front panel description



Features

1	7x Analogs inputs 12 bits@120MS/s and 3 of them 2x ADCs per input.
2	Digital input trigger and output trigger.
3	2x LED Flasher control
4	24 Volts Power supply .
5	**6X** PMT control.
6	Tank control.
7	RS-232 Radio connector.
8	GPS antenna connector.
9	USB 2,0 OTG, for external devices (0.5 Watts max.).
10	External extension connector. Works with an external electronic (19-32 Volts no regulated). 8 bits LVDS
11	Ethernet 10/100/1000 MBits.
12	System Terminal (UART to USB interface inside).
13	Slow-Control Terminal (UART to USB interface inside).
14	2x RESET switches, System and Slow-control.

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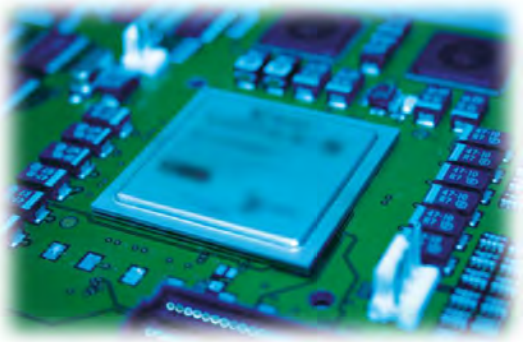
Design layout requirements proposal



Layout design:

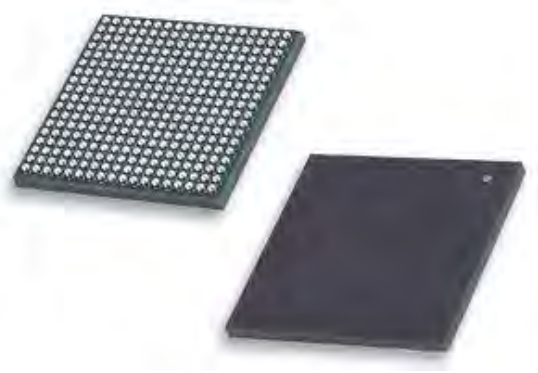
- LVDS: wire adapted 100 Ohms .
- Analog : 50 Ohms adapted.
- LP-DDR2 : 50 Ohms adapted.
- Same wire length between each ADC Clock and between each ADC data.

Electronic board:

- Class: 6
- 10 layers (symmetric)
- Size: 340 x 240 x 1,8 mm (maybe smaller)
- Tropical coating (not for the first prototypes).

Top	Signal (adapted)
GND 1	Gnd plan
Int 1	Signal (partial adapted)
Power 1	Power plans
Int 2	Signal
Int 3	Signal
Power 4	Power plans
Int 4	Signal (partial adapted)
GND 2	Gnd plan
Bottom	Signal (adapted)

Component specifications proposal



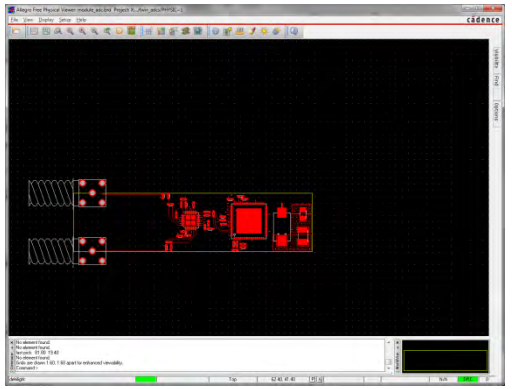
Global specifications:

- Available components for production up to 2016.
- Operating Temperature range: -20° to +70° C.
- RoHS compliant.
- No pending obsolescence components (warning: Obsolete components could be available).
- Standard Resistor: 1% tolerance.

Package:

- SMD packages privileged. Connector could have through-hole.
- Passive components (standard resistors & capacitors): 0603 package (down to 0402 for WP1 & WP5).
- Preferred PQFP, SSOP, SO, … instead of QFN & BGA packages.

Design integration proposal



SDEU will be designed with CADENCE 16.6 CAD software.
2 integration cases:

WPs don't use CADENCE:

- Schematics (PDF & CAD files).
- Layout specifications.
- Bill of Material (use template provided by WP5).

WPs use CADENCE:

- Used a common component CADENCE library (provided by LPSC).
- Used same WP5 layout specifications (wire width,…).
- CADENCE project files (Schematics, layout,…)

Eval. board (WP5) design description

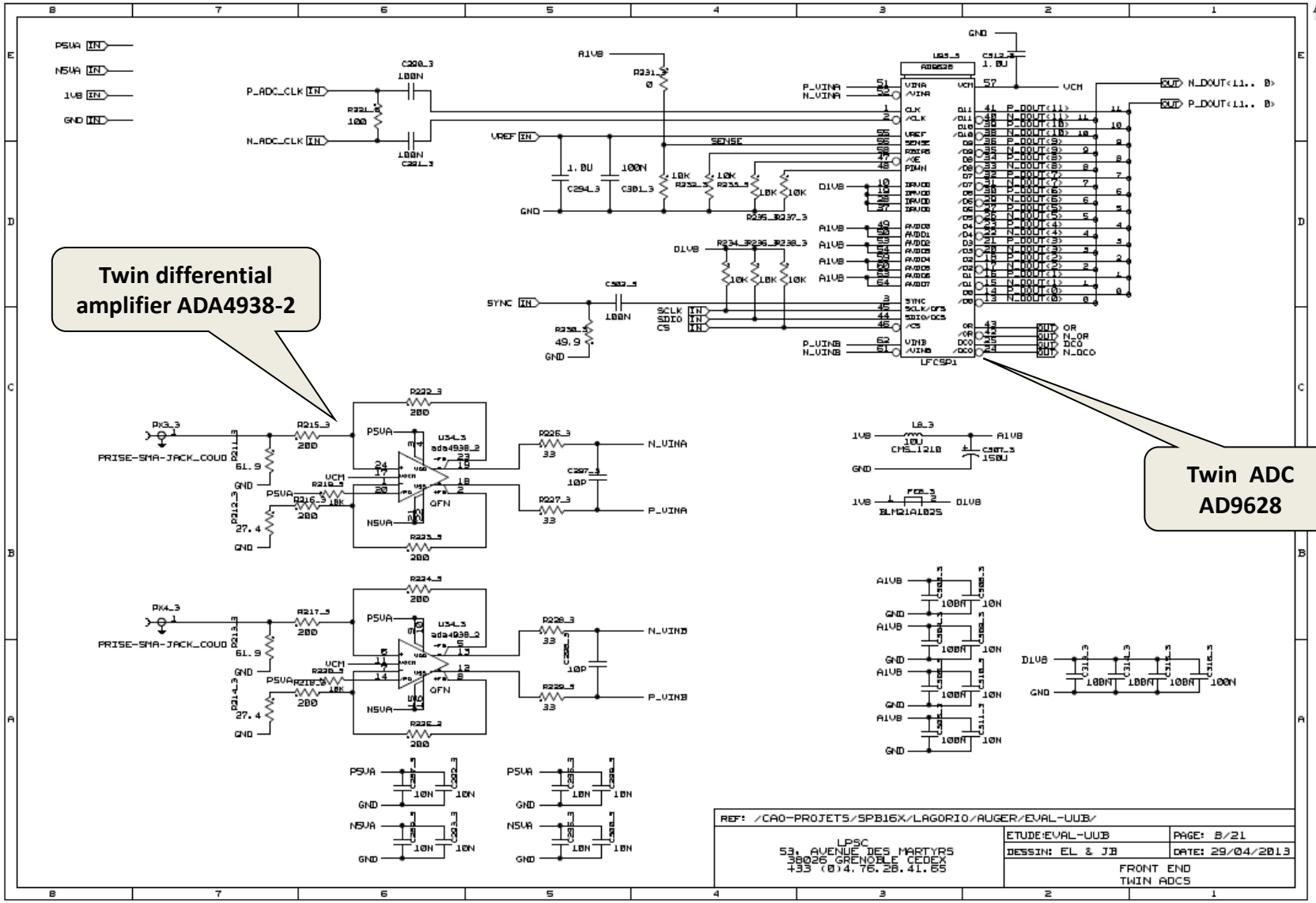
Must be validated:

- FPGA/LP-DDR2 sub-design functionality.
- Power supplies efficiency.
- Sub-designs layouts ready for prototype design.
- Mechanical: Sizes, front panel, connectors, GPS, …
- Slow-control power supplies start.

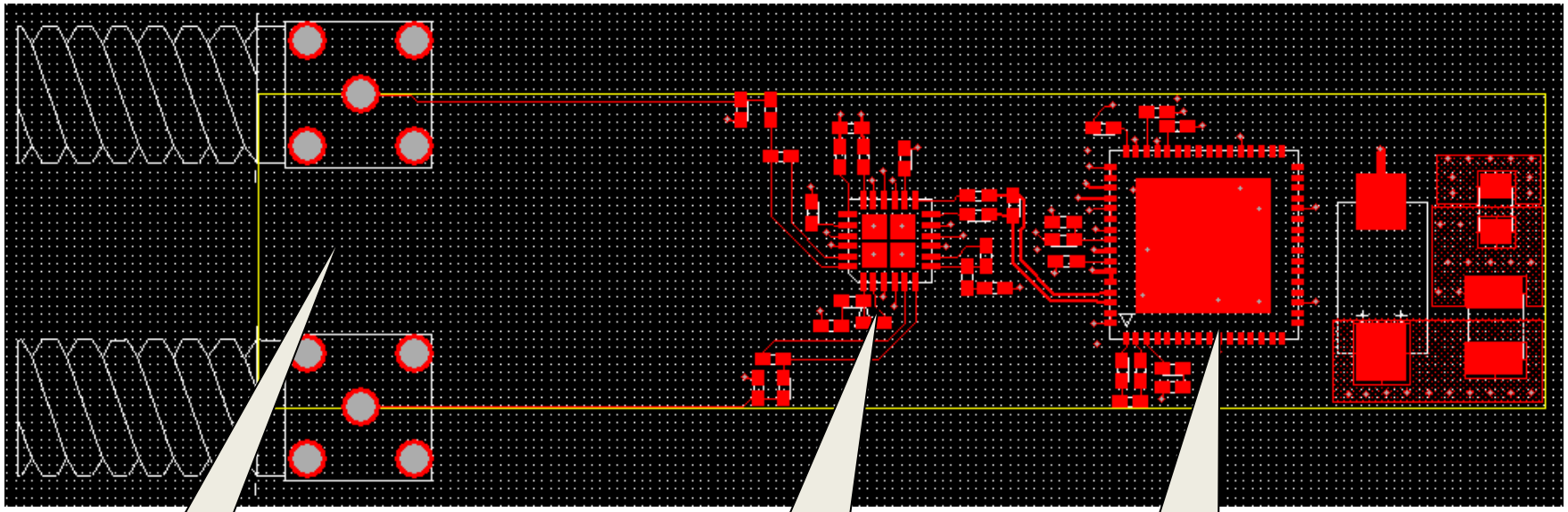
Devices:

1x ADC AD9628 **12 bits 120 MS/s**
Xilinx Zynq 7020 C: Dual µ-processor **ARM Cortex A9 333 Mhz**
4 Gbits LP-DDR2 memory (Low Power DDR2)
1 Gbits Flash memory (storage memory)
i-LOTUS GPS
LINUX
Online VHDL & software updatable
Industrial power supply connector (IP67)
Ethernet **& OTG USB**
Specific Slow-control and system USB control interface

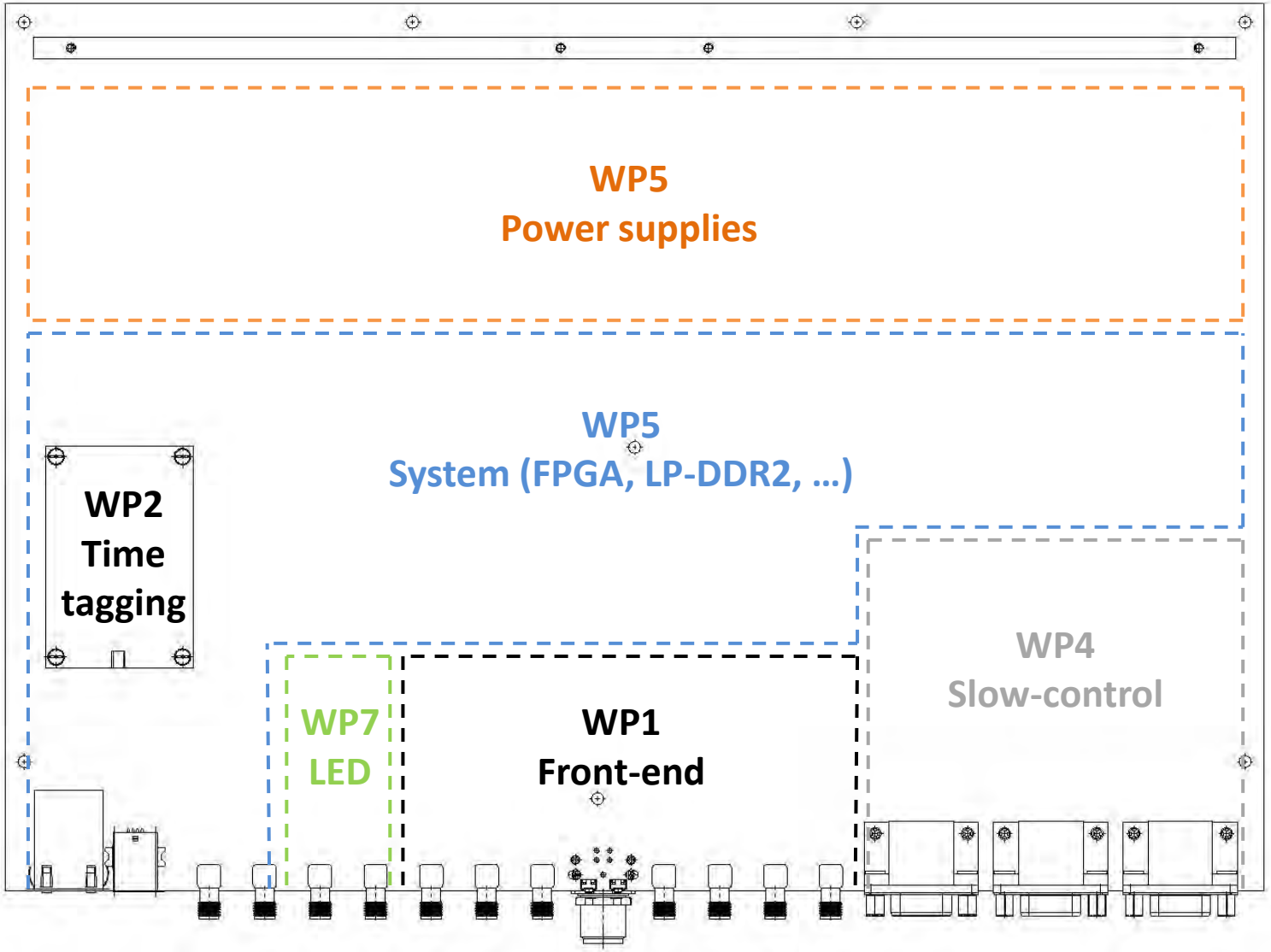
"Basic" Front-end Sub-design schematic



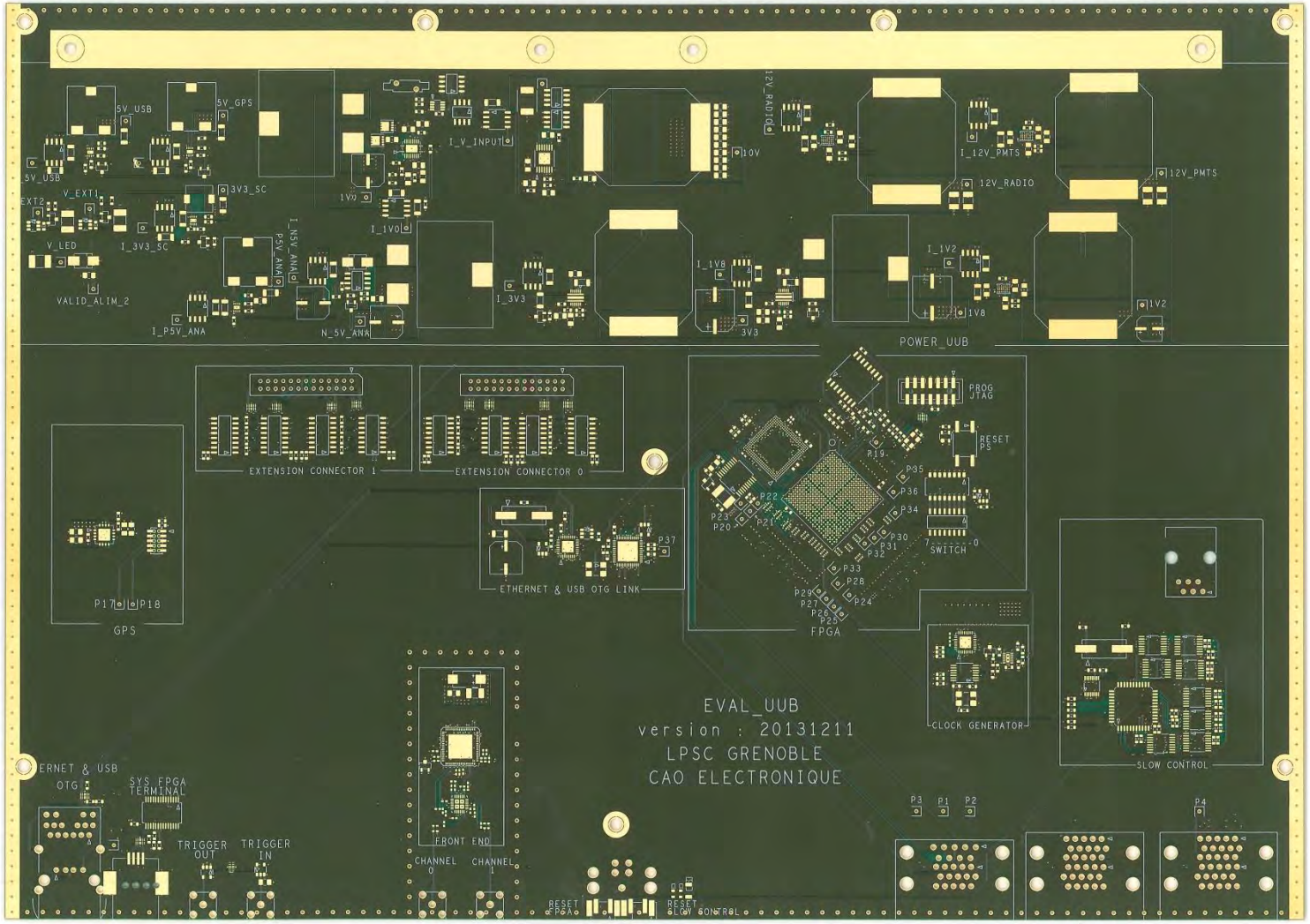
"Basic" Front-end Sub-design layout



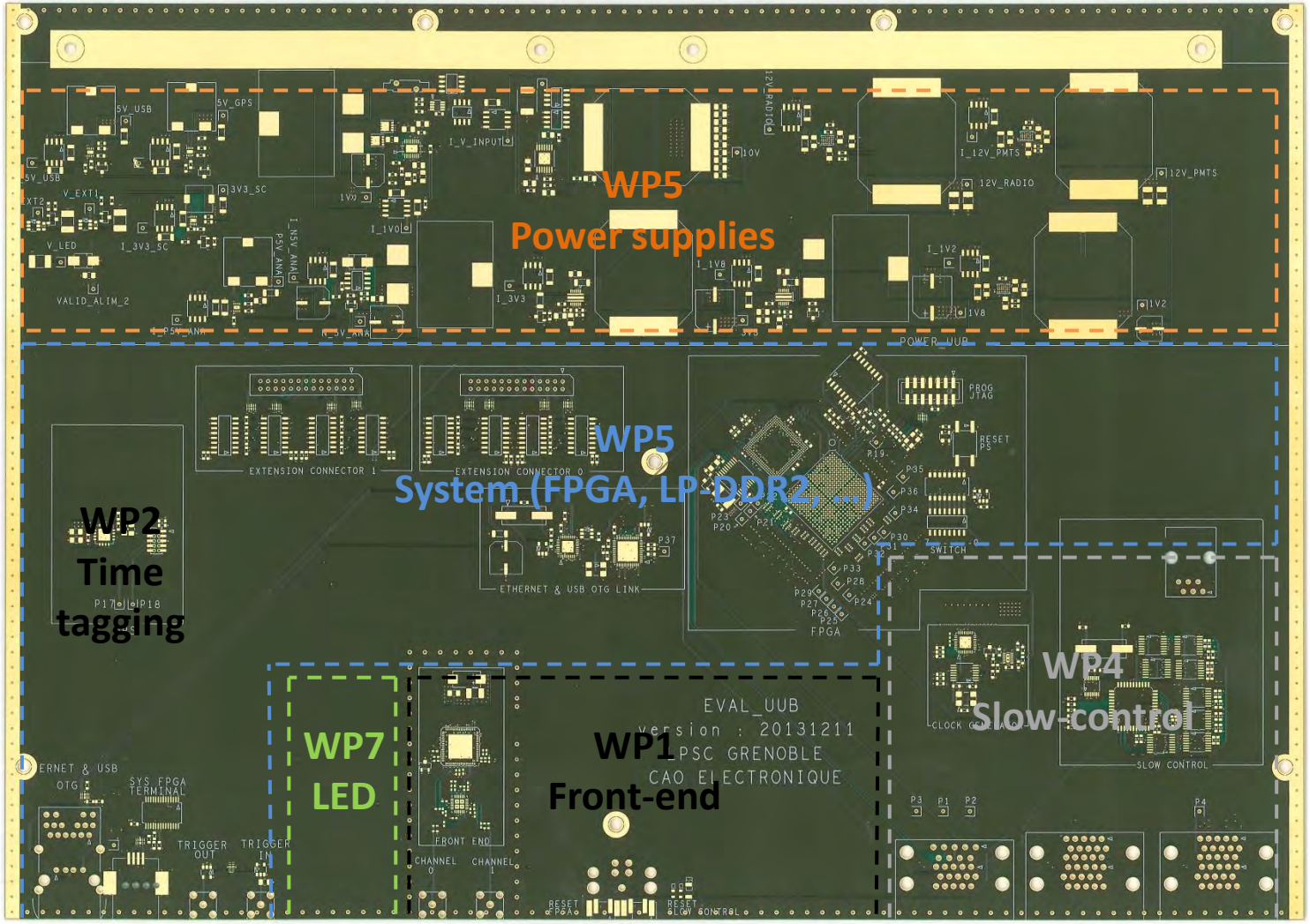
Hardware WP on SDE board



Evaluation board



Evaluation board



Works in progress & expects

Studies:

- Test and validation evaluation board (hardware, VHDL, software).
- Optimize power supplies (size and cost).
- Start evaluation board test : end January

Status:

- FPGA, only **16 I/Os available as 8% total IOs (above 90% used IOs, very difficult VHDL integration),** multi-voltage (**14x** 1,8V and **4x** 3,3 V)
- **POWER CONSUMPTION CRITICAL**.

Preview SDEU